

PATENT ASSIGNMENT

Electronic Version v1.1
 Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
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NATURE OF CONVEYANCE:	ASSIGNMENT
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CONVEYING PARTY DATA	
Name	Execution Date
On-Chip Technologies, Inc.	03/13/2008

RECEIVING PARTY DATA	
Name:	OC Applications Research LLC
Street Address:	1209 Orange Street
City:	Wilmington
State/Country:	DELAWARE
Postal Code:	19801

PROPERTY NUMBERS Total: 19	
Property Type	Number
Patent Number:	6687865
Patent Number:	6964001
Patent Number:	7080301
Application Number:	11424610
Patent Number:	7234092
Patent Number:	7197681
Patent Number:	7188286
Patent Number:	7200784
Application Number:	11182809
Application Number:	11208882
Application Number:	11208883
Application Number:	11680684
Application Number:	12046336
Application Number:	12047408
Application Number:	60079316

CH \$760.00 6687865

Application Number:	60387683
PCT Number:	US0318287
Application Number:	10922830
Application Number:	60651993

CORRESPONDENCE DATA

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ATTORNEY DOCKET NUMBER:	27592-01026
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NAME OF SUBMITTER:	Jeffrey W. Gluck
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Total Attachments: 8
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ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, On-Chip Technologies, Inc., a California corporation, with an office at 495 Sleeper Avenue, Mountain View, CA 94040 ("*Assignor*"), does hereby sell, assign, transfer, and convey unto OC Applications Research LLC, a Delaware limited liability company, with an address at 1209 Orange Street, Wilmington, DE 19801 ("*Assignee*"), or its designees, all right, title, and interest that exist today and may exist in the future in and to any and all of the following (collectively, the "*Patent Rights*"):

(a) the provisional patent applications, patent applications and patents listed in the table below (the "*Patents*");

(b) all patents and patent applications (i) that are Related Assets (as defined below), and/or (ii) that were co-owned applications that incorporate by reference, or are incorporated by reference into, the Patents;

(c) all reissues, reexaminations, extensions, continuations, continuations in part, continuing prosecution applications, requests for continuing examinations, divisions, registrations of any item in any of the foregoing categories (a) and (b);

(d) all foreign patents, patent applications, and counterparts relating to any item in any of the foregoing categories (a) through (c), including, without limitation, certificates of invention, utility models, industrial design protection, design patent protection, and other governmental grants or issuances;

(e) all items in any of the foregoing in categories (b) through (d), whether or not expressly listed as Patents below and whether or not claims in any of the foregoing have been rejected, withdrawn, cancelled, or the like;

(f) all inventions, invention disclosures, and discoveries described in any item in any of the foregoing categories (a) through (e);

(g) all rights to apply in any or all countries of the world for patents, certificates of invention, utility models, industrial design protections, design patent protections, or other governmental grants or issuances of any type related to any item in any of the foregoing categories (a) through (f), including, without limitation, under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement, or understanding;

(h) all causes of action (whether known or unknown or whether currently pending, filed, or otherwise) and other enforcement rights under, or on account of, any of the Patents and/or any item in any of the foregoing categories (b) through (g), including, without limitation, all causes of action and other enforcement rights for

- (i) damages,
- (ii) injunctive relief, and
- (iii) any other remedies of any kind

for past, current, and future infringement; and

- (i) all rights to collect royalties and other payments under or on account of any of the Patents and/or any item in any of the foregoing categories (b) through (h).

For purposes of this Assignment of Patent Rights, "**Related Assets**" means, with respect to a specified Patent, (a) those patents and patent applications (i) that directly claim priority to such Patent or to any other Related Asset of such Patent, and/or (ii) from which such Patent or any other Related Asset of such Patent directly claims priority, together with (b) those patents and patent applications (1) that directly claim priority to any patents or patent applications described in the foregoing subparagraph (a), and/or (2) from which any of the patents or patent applications described in the foregoing subparagraph (a) directly claims priority.

Patent or Application No.	Country	Filing Date	<u>Title of Patent and First Named Inventor</u>
6,687,865	USA	Mar. 24, 1999	On-chip service processor for test and debug of integrated circuits (Bulent Dervisoglu)
6,964,001	USA	Jan. 20, 2004	On-chip service processor (Bulent Dervisoglu)
7,080,301	USA	Oct. 31, 2005	On-chip service processor (Bulent Dervisoglu)
App. 11/424,610	USA	June 16, 2007	On-chip service processor (Bulent Dervisoglu)
7,234,092	USA	Jan. 24, 2003	Variable clock scan test circuitry and method (Laurence Cooke)
GB 2403811	United Kingdom	Nov. 11, 2004	Variable clock scan test circuitry and method (Laurence Cooke)
GB 2415789	United Kingdom	Nov. 11, 2004	Variable clock scan test circuitry and method

<u>Patent or Application No.</u>	<u>Country</u>	<u>Filing Date</u>	<u>Title of Patent and First Named Inventor</u>
			(Laurence Cooke)
7,197,681	USA	Jan. 5, 2004	Accelerated scan circuitry and method for reducing scan test data volume and execution time (Bulent Dervisoglu)
7,188,286	USA	Sept. 1, 2004	Accelerated scan circuitry and method for reducing scan test data and execution time (Bulent Dervisoglu)
7,200,784	USA	Sept. 1, 2004	Accelerated scan circuitry and method for reducing scan test data volume and execution time (Bulent Dervisoglu)
US20060195746 (11/182,809)	USA	Aug. 31, 2006	Variable clocked scan test improvements (Laurence Cooke)
US20070050596 (11/208,882)	USA	Aug. 23, 2005	Hashing and serial decoding techniques (Laurence Cooke)
US20070168798 (11/208,883)	USA	Aug.23, 2005	Scan string segmentation for digital test compression (Laurence Cooke)
US20070162803 (11/680,684)	USA	Mar. 1, 2007	Accelerated scan circuitry and method for reducing scan test data volume and execution time (Bulent Dervisoglu)
12/046,336	USA	Mar. 11, 2007	Variable Clock Scan Test Improvements (Laurence Cooke)
12/047,408	USA	Mar. 13, 2007	Variable Clock Scan Test Circuitry and Method (Laurence Cooke)

Assignor represents, warrants and covenants that:

(1) Assignor has the full power and authority, and has obtained all third party consents, approvals and/or other authorizations required to enter into this Agreement and to carry out its obligations hereunder, including the assignment of the Patent Rights to Assignee; and

(2) Assignor owns, and by this document assigns to Assignee, all right, title, and interest to the Patent Rights, including, without limitation, all right, title, and interest to sue for infringement of the Patent Rights. Assignor has obtained and properly recorded previously executed assignments for the Patent Rights as necessary to fully perfect its rights and title therein in accordance with governing law and regulations in each respective jurisdiction. The Patent Rights are free and clear of all liens, claims, mortgages, security interests or other encumbrances, and restrictions.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.


Assignor will, at the reasonable request of Assignee do all things necessary, proper, or advisable, including without limitation, the execution, acknowledgment, and recordation of specific assignments, oaths, declarations, and other documents on a country-by-country basis, to assist Assignee in obtaining, perfecting, sustaining, and/or enforcing the Patent Rights. Such assistance will include providing, and obtaining from the respective inventors, prompt production of pertinent facts and documents, giving of testimony, execution of petitions, oaths, powers of attorney, specifications, declarations or other papers, and other assistance reasonably necessary for filing patent applications, complying with any duty of disclosure, and conducting prosecution, reexamination, reissue, interference or other priority proceedings, opposition proceedings, cancellation proceedings, public use proceedings, infringement or other court actions and the like with respect to the Patent Rights. Assignor shall provide such assistance relating to conveying and perfecting the right, title, and interest in the Patent Rights unto Assignee without demanding any further compensation. For all other assistance specified in this paragraph or otherwise, Assignee shall pay Assignor and/or the inventors a reasonable hourly professional fee for time spent providing such assistance and shall reimburse Assignor and/or the inventors for their reasonable expenses, including attorneys' fees, incurred in providing such assistance.

The terms and conditions of this Assignment of Patent Rights will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed at Moua fa
View on 3/13/2008

ASSIGNOR:

On-Chip Technologies, Inc.

By: 
 Name: Balent Dervisoglu
 Title: Chief Executive Officer
 (Signature MUST be notarized)

STATE OF _____)
) ss.
 COUNTY OF _____)

On _____, before me, _____,
 Notary Public in and for said State, personally appeared _____,
 personally known to me (or proved to me on the basis of satisfactory evidence) to be the
 person whose name is subscribed to the within instrument and acknowledged to me that
 he/she executed the same in his/her authorized capacity, and that by his/her signature on the
 instrument the person, or the entity upon behalf of which the person acted, executed the
 instrument.

WITNESS my hand and official seal.

Signature _____
 K. L. DUBAL, NOTARY PUBLIC (Seal)

See attached

ACKNOWLEDGMENT

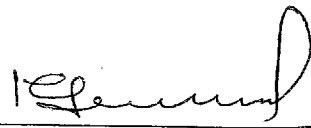
State of California
County of Santa Clara

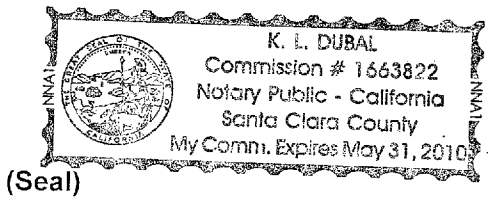
On March 13, 2008 before me, K. L. DUBAL, NOTARY PUBLIC
(insert name and title of the officer)

personally appeared Bulent Dervisoylu
who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is are
subscribed to the within instrument and acknowledged to me that he she/they executed the same in
his/her/their authorized capacity(ies), and that by his/her/their signature(s) on the instrument the
person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing
paragraph is true and correct.

WITNESS my hand and official seal.

Signature 



ASSIGNMENT OF RIGHTS IN CERTAIN ASSETS

For good and valuable consideration, the receipt of which is hereby acknowledged, On-Chip Technologies, Inc., a California corporation, with an office at 495 Sleeper Avenue, Mountain View, CA 94040 (“*Assignor*”), does hereby sell, assign, transfer, and convey unto OC Applications Research LLC, a Delaware limited liability company, with an address at 1209 Orange Street, Wilmington, DE 19801 (“*Assignee*”), or its designees, the right, title, and interest in and to any and all of the following provisional patent applications, patent applications, patents, and other governmental grants or issuances of any kind (the “*Certain Assets*”):

<u>Patent or Application No.</u>	<u>Country</u>	<u>Filing Date</u>	<u>Title of Patent and First Named Inventor</u>
60/079,316 (Provisional)	USA	Mar. 25, 1998	On-chip service processor for test and debug of integrated circuits (Bulent Dervisoglu)
60/387,683 (Provisional)	USA	June 22, 2003	Variable clocked scan test method (Laurence Cooke)
PCT/US03/18287 (WO/03/104828)	WO	June 11, 2003	Variable Clock Scan Test Circuitry and Method (Laurence Cooke)
10/922,830 (US20060041798)	USA	Aug. 23, 2004	Design Techniques to Increase Testing Efficiency (Laurence Cooke)
60/651,993 (Provisional)	USA	Feb. 14, 2005	Variable clocked scan test improvements (Laurence Cooke)

Assignor assigns to Assignee all rights to the inventions, invention disclosures, and discoveries in the assets listed above, together, with the rights, if any, to revive prosecution of claims under such assets and to sue or otherwise enforce any claims under such assets for past, present or future infringement.


Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to make available to Assignee all records regarding the Certain Assets.

The terms and conditions of this Assignment of Rights in Certain Assets will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

DATED this 13 day of March 2008

ASSIGNOR:

On-Chip Technologies, Inc.

By: 
Name: Bulent Dervisoglu
Title: Chief Executive Officer