

PATENT ASSIGNMENT

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SUBMISSION TYPE:

NEW ASSIGNMENT

NATURE OF CONVEYANCE:

ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
MOSAID Technologies Incorporated	04/30/2008

RECEIVING PARTY DATA

Name:	SAtech Group A.B. Limited Liability Company
Street Address:	2711 Centerville Rd., Suite 400
City:	Wilmington
State/Country:	DELAWARE
Postal Code:	19808

PROPERTY NUMBERS Total: 35

Property Type	Number
Patent Number:	5469401
Patent Number:	5708619
Patent Number:	5546343
Patent Number:	5956274
Patent Number:	6279088
Patent Number:	6560684
Patent Number:	7155581
Patent Number:	5570381
Patent Number:	5822333
Patent Number:	6691218
Application Number:	09733629
Patent Number:	6539369
Patent Number:	6839825
Patent Number:	6880064
Patent Number:	7106732

PATENT

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REEL: 021040 FRAME: 0648

CH \$1400.00 5469401

Patent Number:	6917954
Patent Number:	6836771
Application Number:	11099724
Application Number:	11502587
Patent Number:	6775281
Patent Number:	6862287
Application Number:	11069635
Patent Number:	6990001
Patent Number:	7095640
Patent Number:	7298637
Patent Number:	7003625
Patent Number:	7194574
Patent Number:	7010741
Patent Number:	7350137
Patent Number:	7017064
Application Number:	11327725
Patent Number:	7136961
Application Number:	11548766
Application Number:	09886659
Application Number:	12111138

CORRESPONDENCE DATA

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ATTORNEY DOCKET NUMBER:	MOSAID
NAME OF SUBMITTER:	Robert J. Irvine III

Total Attachments: 8
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ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, MOSAID Technologies Incorporated, a Canadian company, with an office at 11 Hines Road, Kanata, Ontario, Canada, K2K 2X1 ("**Assignor**"), does hereby sell, assign, transfer, and convey unto SAtech Group A.B. Limited Liability Company, a Delaware limited liability company, with an address at 2711 Centerville Rd, Suite 400, Wilmington, DE 19808 ("**Assignee**"), or its designees, all right, title, and interest that exist today and may exist in the future in and to any and all of the following (collectively, the "**Patent Rights**"):

(a) the provisional patent applications, patent applications and patents listed in the table below (the "**Patents**");

(b) all patents and patent applications (i) to which any of the Patents directly or indirectly claims priority, and/or (ii) for which any of the Patents directly or indirectly forms a basis for priority;

(c) all reissues, reexaminations, extensions, continuations, continuations in part, continuing prosecution applications, requests for continuing examinations, divisions, registrations of any item in any of the foregoing categories (a) and (b);

(d) all foreign patents, patent applications, and counterparts relating to any item in any of the foregoing categories (a) through (c), including, without limitation, certificates of invention, utility models, industrial design protection, design patent protection, and other governmental grants or issuances;

(e) all items in any of the foregoing in categories (b) through (d), whether or not expressly listed as Patents below and whether or not claims in any of the foregoing have been rejected, withdrawn, cancelled, or the like;

(f) inventions, invention disclosures, and discoveries described in any of the Patents and/or any item in the foregoing categories (b) through (e) that (i) are included in any claim in the Patents and/or any item in the foregoing categories (b) through (e), (ii) are subject matter capable of being reduced to a patent claim in a reissue or reexamination proceedings brought on any of the Patents and/or any item in the foregoing categories (b) through (e), and/or (iii) could have been included as a claim in any of the Patents and/or any item in the foregoing categories (b) through (e);

(g) all rights to apply in any or all countries of the world for patents, certificates of invention, utility models, industrial design protections, design patent protections, or other governmental grants or issuances of any type related to any item in any of the foregoing categories (a) through (f), including, without limitation, under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement, or understanding;

(h) all causes of action (whether known or unknown or whether currently pending, filed, or otherwise) and other enforcement rights under, or on account of, any of the Patents and/or any item in any of the foregoing categories (b) through (g), including, without limitation, all causes of action and other enforcement rights for

- (1) damages,
- (2) injunctive relief, and
- (3) any other remedies of any kind

for past, current, and future infringement except to the extent any of the foregoing in this subparagraph (h) are precluded by the Prior Licenses (as defined in the Patent Purchase Agreement dated April 28, 2008 between Assignor and Assignee (the "PPA")); and

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(i) all rights to collect royalties and other payments under or on account of any of the Patents and/or any item in any of the foregoing categories (b) through (h), except for such monetary rights included under the Prior Licenses (as defined in the PPA).

<u>Patent or Application No.</u>	<u>Country</u>	<u>Filing Date</u>	<u>Title of Patent and First Named Inventor</u>
5,469,401 (07/913,183)	US	11/21/1995 (7/14/1992)	Column redundancy scheme for DRAM using normal and redundant column decoders programmed with defective array address and defective column address Gillingham, Peter B.
5,708,619 (08/560,547)	US	1/16/1998 (11/17/1995)	Column redundancy scheme for DRAM using normal and redundant column decoders programmed with defective array address and defective column address Gillingham, Peter B.
5,546,343 (08/224,998)	US	8/13/1996 (4/7/1997)	Method and apparatus for a single instruction operating multiple processors on a memory chip Elliott, Duncan G
5,956,274 (08/686,504)	US	9/21/1999 (7/24/1996)	Memory device with multiple processors having parallel access to the same memory area Elliott, Duncan G.
6,279,088 (09/275,972)	US	8/21/2001 (3/25/1999)	Memory device with multiple processors having parallel access to the same memory area Elliott, Duncan G.
6,560,684 (09/907,825)	US	5/6/2003 (7/19/2001)	Method and apparatus for an energy efficient operation of multiple processors in a memory Elliott, Duncan G.
7,155,581 (10/429,690)	US	12/26/2006 (5/6/2003)	Method and apparatus for an energy efficient operation of multiple processors in a memory Elliott, Duncan G.
5,570,381 (08/430,230)	US	10/29/1996 (4/28/1995)	Synchronous DRAM tester Schofield, Paul

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
5,822,333 (08/624,213)	US	10/13/1998 (3/29/1996)	Digital memory testing method Foss, Richard C.
CA2393760 (CA2393760)	CA	(12/8/2000)	Method and apparatus for longest match address lookup Brown David A.
CN00818946.3	CN	12/8/2000	Method and apparatus for longest match address lookup Brown David A.
DE10085388.9	DE	12/8/2000	Method and apparatus for longest match address lookup Brown David A.
JP2001-0542955	JP	12/8/2000	Method and apparatus for longest match address lookup Brown David A.
GB2374174 (GB0213390.8)	GB	2/3/2004 (12/8/2000)	Method and apparatus for longest match address lookup Brown David A.
CA2395151	CA	12/8/2000	Method and apparatus for longest match address lookup Brown David A.
CN00818947.1	CN	12/8/2000	Method and apparatus for longest match address lookup Brown David A.
DE10085390.0	DE	12/8/2000	Method and apparatus for longest match address lookup Brown David A.
GB2373083 (GB0213389.0)	GB	(12/8/2000)	Method and apparatus for longest match address lookup Brown David A.
JP2001-0542932	JP	12/8/2000	Method and apparatus for longest match address lookup Brown David A.
CA2397608	CA	12/8/2000	Method and apparatus for longest match address lookup Brown David A.
DE10085389.7	DE	12/8/2000	Method and apparatus for longest match address lookup Brown David A.
JP20010542933T	JP	12/8/2000	Method and apparatus for longest match address lookup

<u>Patent or Application No.</u>	<u>Country</u>	<u>Filing Date</u>	<u>Title of Patent and First Named Inventor</u>
			Brown David A.
GB2373082 (GB0213387.4)	GB	2/17/2004 (12/8/2000)	Method and apparatus for longest match address lookup Brown David A.
CN00818944.7	CN	12/8/2000	Method and apparatus for longest match address lookup Brown David A.
6,691,218 (09/733,627)	US	2/10/2004 (12/8/2000)	Method and apparatus for longest match address lookup Brown David A.
09/733,629	US	12/8/2000	Method and apparatus for an incremental update of a longest prefix match lookup table David Brown
6,539,369 (09/733,761)	US	3/25/2003 (12/8/2000)	Method and apparatus for storing sparse and dense subtrees in a longest prefix match lookup table Brown, David A.
6,839,825 (09/886,649)	US	1/4/2005 (6/21/2001)	Method and apparatus for logically expanding the width of memory Brown, David A.
6,880,064 (09/886,650)	US	4/12/2005 (6/21/2001)	Method and apparatus for physical width expansion of a longest prefix match lookup table Brown, David A.
7,106,732 (10/004,280)	US	9/12/2006 (10/31/2001)	Default route coding Brown, David A.
CA2365395	CA	12/17/2001	Default route coding Brown, David A.
6,917,954 (10/132,675)	US	7/12/2005 (4/24/2002)	Load balancing in IP address lookup Ahmad, Imtiaz
6,836,771 (10/336,055)	US	12/28/2004 (1/2/2003)	Method and apparatus for storing sparse and dense subtrees in a longest prefix match lookup table Brown, David A.
11/099,724	US	4/6/2005	Method and apparatus for physical width expansion of longest prefix match lookup table Brown, David A.
11/502,587	US	8/10/2006	Default route coding David Brown
6,775,281 (09/409,184)	US	8/10/2004 (9/30/1999)	Method and apparatus for a four-way hash table Brown, David A.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
CA2385331	CA	9/18/2000	Method and apparatus for a four-way hash table Brown, David A.
CN1377543 (CN00813708)	CN	12/8/2004 (9/18/2000)	Method and apparatus for a four-way hash table Brown, David A.
GB2370187 (GB0207003.5)	GB	11/11/2003 (9/18/2000)	Method and apparatus for a four-way hash table Brown, David A.
JP2001-0527500	JP	9/18/2000	Method and apparatus for a four-way hash table Brown, David A.
6,862,287 (10/187,472)	US	3/1/2005 (6/28/2002)	Method and apparatus for a four-way hash table Brown, David A.
11/069,635	US	7/7/2005	Method and apparatus for a four-way hash table Brown, David A.
CA2310295	CA	5/31/2000	Multiple match detection circuit and method Ma Stanley Jeh-Chun
CN018133770 (CN01813377)	CN	1/24/2007 (5/31/2001)	Multiple match detection circuit and method Ma Stanley Jeh-Chun
DE10196292.4	DE	5/31/2001	Multiple match detection circuit and method Ma Stanley Jeh-Chun
GB2379545 (229175.5)	GB	05/31/2001	Multiple match detection circuit and method Ma Stanley Jeh-Chun
KR10-0810778 (KR10-2002-7016289)	KR	2/28/2008 (11/29/2002)	Multiple match detection circuit and method Ma Stanley Jeh-Chun
6,990,001 (10/296,884)	US	1/24/2006 (5/31/2001)	Multiple match detection circuit and method Ma Stanley Jeh-Chun
7,095,640 (11/285,197)	US	8/22/2006 (11/23/2005)	Multiple match detection circuit and method Ma Stanley Jeh-Chun
7,298,637 (11/459,420)	US	11/20/2007 (7/24/2006)	Multiple match detection circuit and method Ma Stanley Jeh-Chun
7,003,625 (10/386,378)	US	2/21/2006 (3/10/2003)	Searching small entities in a wide CAM King, Lawrence
7,194,574 (11/291,673)	US	3/20/2007 (11/30/2005)	Multiple match detection circuit and method Ma Stanley Jeh-Chun
7,010,741 (10/306,732)	US	3/7/2006 (11/29/2002)	Method and circuit for error correction in CAM cells Foss, Richard
7,350,137 (11/313,616)	US	3/25/2008 (12/22/2005)	Method and circuit for error correction in CAM cells

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
7,017,064 (09/851,169)	US	3/21/2006 (5/9/2001)	Foss, Richard Calculating apparatus having a plurality of stages Thomas, Terence Neil
CN02119138.7	CN	5/9/2002	Multi-stage counting device Thomas, Terence N.
11/327,725	US	1/6/2006	Calculating apparatus having a plurality of stages Thomas, Terence N.
229,998 (91109550)	TW	05/08/02	Calculating apparatus having a plurality of stages Thomas, Terence N.
7,136,961 (10/357,270)	US	11/14/2006 (1/31/2003)	Method and apparatus for wide word deletion in content addressable memories Roth, Alan
EP03776686.2	EP	11/12/2003	Method and apparatus for wide word deletion in content addressable memories Roth, Alan
(92131747)	TW	11/13/2003	Method and apparatus for wide word deletion in content addressable memories Roth, Alan
CN200380108681	CN	11/12/2003	Method and apparatus for wide word deletion in content addressable memories Roth, Alan
11/548,766	US	10/12/2006	Method and apparatus for wide word deletion in content addressable memories Roth, Alan
09/886,659	US	06/21/2001	Method and Apparatus for Logically Expanding the Length of A Search Key Brown, David A.
12/111,138	US	04/28/2008	Calculating apparatus having a plurality of stages Terence N. Thomas

Assignor represents, warrants and covenants that:

(1) Assignor has the full power and authority, and has obtained all third party consents, approvals and/or other authorizations required to enter into this Agreement and to carry out its obligations hereunder, including the assignment of the Patent Rights to Assignee; and

(2) Assignor owns, and by this document assigns to Assignee, all right, title, and interest to the Patent Rights, including, without limitation, all right, title, and interest to sue for infringement of the Patent Rights. Assignor has obtained and properly recorded

previously executed assignments for the Patent Rights as necessary to fully perfect its rights and title therein in accordance with governing law and regulations in each respective jurisdiction. Except for the certain prior granted non-exclusive licenses under the Patent Rights (identified in Exhibit H of the PPA), the Patent Rights are free and clear of all liens, claims, mortgages, security interests or other encumbrances, and restrictions. There are no actions, suits, investigations, claims or proceedings threatened, pending or in progress relating in any way to the Patent Rights. There are no existing contracts, agreements, options, commitments, proposals, bids, offers, or rights with, to, or in any person to acquire any of the Patent Rights.

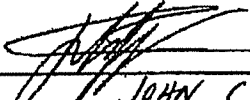
Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

Assignor will, at the reasonable request of Assignee and without demanding any further consideration therefore, do all things necessary, proper, or advisable, including without limitation, the execution, acknowledgment, and recordation of specific assignments, oaths, declarations, and other documents on a country-by-country basis, to assist Assignee in obtaining, perfecting, sustaining, and/or enforcing the Patent Rights. The terms and conditions of this Assignment of Patent Rights will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

ON April 30, 2008 IN WITNESS WHEREOF this Assignment of Patent Rights is executed at Kanta.

ASSIGNOR:

MOSAID Technologies Incorporated

By: 
Name: JOHN C. LINDGREN
Title: President + CEO
(Signature MUST be attested)

ATTESTATION

The undersigned witnessed the signature of John Lindgren to the above Assignment of Patent Rights on behalf of MOSAID Technologies Incorporated and makes the following statements:

1. I am over the age of 18 and competent to testify as to the facts in this Attestation block if called upon to do so.

2. John Lindgren is personally known to me (or proved to me on the basis of satisfactory evidence) and appeared before me on April 30 2008 to execute the above Assignment of Patent Rights on behalf of MOSAID Technologies Incorporated.

3. John Lindgren subscribed to the above Assignment of Patent Rights on behalf of MOSAID Technologies Incorporated.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

EXECUTED on April 30, 2008 (date)

Vinod Kumar
Print Name: VINOD KUMAR