

PATENT ASSIGNMENT

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OP \$40.00 11074808

ASSIGNMENT

We, Toshiba America Electronic Components, Inc., a corporation organized under the laws of California, located at 19900 MacArthur Boulevard, Suite 400, Irvine, CA 92612, U.S.A., the assignee of the following U.S. Patent Application:

<u>SERIAL NO.</u>	<u>DATE FILED</u>	<u>INVENTORS</u>
11/074,808	3/8/2005	Kenji Iwamura

TITLE OF INVENTION

Systems and Methods for Design Verification Using Selectively Enabled Checkers

hereby assign the entirety of our right, title and interest in said U.S. Patent Application, including all divisions, reissues, continuations, substitutions and extensions thereof and all rights arising under or pursuant to any and all international agreements, treaties or laws relating to the protection of industrial property, including rights of priority, resulting from the filing of any said application to KABUSHIKI KAISHA TOSHIBA, a Japanese corporation, located at 1-1 Shibaura 1-chome, Minato-ku, Tokyo, Japan, their successors, assigns, or other legal representatives.

The undersigned is authorized to sign this document on behalf of the corporation.

TOSHIBA AMERICA ELECTRONIC
COMPONENTS, INC.

By: 
Name: Mr. Hideya Sakaida
Title: President and CEO

Date: 4/28/08

Approved
TAEC Legal Department