PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Mr. Jin-Ki KIM	06/23/2008

RECEIVING PARTY DATA

Name:	MOSAID Technologies Incorporated
Street Address:	11 Hines Road
City:	Kanata, Ontario
State/Country:	CANADA
Postal Code:	K2K 2X1

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	11613563

CH $40.00 11613563

CORRESPONDENCE DATA

Fax Number: (613)591-8148
Correspondence will be sent via US Mail when the fax attempt is unsuccessful.
Phone: 613-599-9539
Email: ipadmin@mosaid.com
Correspondent Name: Victoria Donnelly
Address Line 1: 11 Hines Road
Address Line 4: Kanata, Ontario, CANADA K2K 2X1

ATTORNEY DOCKET NUMBER:	1232-01US-000-25
NAME OF SUBMITTER:	Victoria Donnelly

Total Attachments: 7
source=Confirmatory Assignment Jin-Ki Kim#page1.tif
source=Confirmatory Assignment Jin-Ki Kim#page2.tif
source=Confirmatory Assignment Jin-Ki Kim#page3.tif
source=Confirmatory Assignment Jin-Ki Kim#page4.tif
source=Confirmatory Assignment Jin-Ki Kim#page5.tif

source=Confirmatory Assignment Jin-Ki Kim#page6.tif
source=Confirmatory Assignment Jin-Ki Kim#page7.tif

CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS

For and in consideration of agreement(s) duly entered into with my employer, MOSAID Technologies Incorporated ("Assignee"), an Ontario corporation, and/or other good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, on this 23rd day of June, 2008, Jin-Ki Kim, ("Assignor"), hereby confirms, selling, assigning, and transferring to Assignee, the full extent of all right, title, and interest in and to any and all of the following (collectively, the "Rights"):

1. The provisional patent applications, patent applications and/or patents listed in the attached Exhibit 'A' (the "Patents");

2. All inventions claimed or described in any or all of the Patents (collectively, the "Inventions");

3. All rights with respect to the Inventions, including all U.S. patents or other governmental grants or issuances that may be granted with respect to the Inventions or from any direct or indirect divisionals, continuations, continuations-in-part, or other patent applications claiming priority rights from the Patents ("Potential Patents");

4. All reissues, reexaminations, extensions, or registrations of the Patents or Potential Patents;

5. All non-United States patents, patent applications, and counterparts relating to any or all of the Inventions, the Patents, or Potential Patents, including, without limitation, certificates of invention, utility models, industrial design protection, design patent protection, and other governmental grants or issuances ("Foreign Rights"), and including the right to file foreign applications directly in the name of Assignee, its successors and assigns;

6. The right to claim priority rights deriving from the Patents;

7. All causes of action and remedies related to any or all of the Patents, the Inventions, Potential Patents, or Foreign Rights (including, without limitation, the right to sue for past, present, or future infringement, misappropriation or violation of rights related to any of the foregoing and the right to collect royalties and other payments under or on account of any of the foregoing); and

8. Any and all other rights and interests arising out of, in connection with, or in relation to the Patents, the Inventions, Potential Patents, or Foreign Rights.

9. Assignor will not sign any writing or do any act conflicting with this Assignment, and, will sign all documents and do such additional acts as Assignee, their successors, legal representatives, and assigns deem necessary or desirable to perfect enjoyment of the Rights, conduct proceedings regarding the Rights (including any litigation or interference proceedings), or perfect or defend title to the Rights. Assignee shall compensate Assignor for any reasonable, documented disbursements provided that Assignor shall have furnished Assignee an advance, written estimate of the fees and costs for such assistance and Assignee shall have agreed in writing to pay such fees and costs. Assignor requests the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention,

utility models, or other governmental grants or issuances that may be granted upon any of the Rights in the name of the Assignee, as the assignee to the entire interest therein.

10. Assignor authorizes the firm, where applicable, MOSAID Technologies Incorporated and its agents to insert any further identification necessary to make this assignment suitable for recordation in the Patent Offices of any country as may be required.

11. The terms and conditions of this Assignment will inure to the benefit of Assignee, its successors, legal representatives, and assigns and will be binding upon Assignor, his successors, legal representatives and assigns.

By: _____
Jin-Ki Kim
Mosaid Technologies Incorporated

ATTESTATION

The undersigned witnessed the signature of Jin-Ki Kim to this document and makes the following statements:

1. Jin-Ki Kim is personally known to me (or proved to me on the basis of satisfactory evidence) and appeared before me on June 23, 2008, to execute this document.

2. Jin-Ki Kim subscribed to this document.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

By: Tammy Kelley
Print Name: Tammy Kelly

EXHIBIT 'A'

Serial #	Country ID	Filed Date	Title
2384039.00	CA	4/30/2002	Low Power Content Addressable Memory Architecture
2541046.00	CA	3/27/2006	Power Supply Testing Architecture
2627663.00	CA	9/29/2006	Daisy Chain Cascading Devices
PCT/CA2006/001606	CA	9/29/2006	Multiple Independent Serial Link Memory
2781031.60	DE	12/5/2002	Low Power Content Addressable Memory Architecture
2828188.80	CN	12/5/2002	Low Power Content Addressable Memory Architecture
200680036462.20	CN	9/29/2006	Multiple Independent Serial Link Memory
200680036482.X	CN	9/29/2006	Daisy Chain Cascading Devices
6790770.90	EP	9/29/2006	Multiple Independent Serial Link Memory
6790771.70	EP	9/29/2006	Daisy Chain Cascading Devices
6790773.30	EP	9/29/2006	Memory With Output Control
8006223.50	EP	9/29/2006	Daisy Chain Cascading Devices
8006224.30	EP	9/29/2006	Daisy Chain Cascading Devices
8006225.00	EP	9/29/2006	Daisy Chain Cascading Devices
2781031.60	EP	12/5/2002	Low Power Content Addressable Memory Architecture
91137612.00	TW	12/27/2002	Low Power Content Addressable Memory Architecture
95136434.00	TW	9/29/2006	Daisy Chain Cascading Devices
95136448.00	TW	9/29/2006	Memory With Output Control
95136449.00	TW	9/29/2006	Multiple Independent Serial Link Memory
96102363.00	TW	1/22/2007	Power Supply Testing Architecture
96108972.00	TW	3/15/2007	Nonvolatile Memory System
96109567.00	TW	3/20/2007	Non-Volatile Semiconductor Memory With Page Erase
96111391.00	TW	3/30/2007	Flash Memory System Control Scheme
96112915.00	TW	4/12/2007	Dynamic Random Access Memory With Fully Independent Partial Array Refresh Function
96118202.00	TW	5/22/2007	Apparatus And Method For Establishing Device Identifiers For Serially Interconnected Devices
96130974.00	TW	8/21/2007	Modular Command Structure For Memory And Memory System
96131131.00	TW	8/22/2007	Scalable Memory System
96134279.00	TW	9/13/2007	Flash Multi-Level Threshold Distribution Scheme
96144786.00	TW	11/26/2007	New Architecture And Circuit Details In Flash Memory
96145695.00	TW	11/30/2007	Flash Memory Program Inhibit Scheme
96145941.00	TW	12/3/2007	Apparatus And Method For Producing Device Identifiers For Serially Interconnected Devices Of Mixed Type
96146276.00	TW	12/5/2007	Apparatus And Method For Producing Device Identifiers For Serially Interconnected Devices Of Mixed Type
96146278.00	TW	12/5/2007	Apparatus And Method For Producing Identifiers Regardless Of Mixed Device Type In A Serial Interconnection

96146482.00	TW	12/6/2007	Address Assignment And Type Recognition Of Serially Interconnected Memory Devices Of Mixed Type
96146483.00	TW	12/6/2007	System And Method Of Operating Memory Devices Of Mixed Typed
96147300.00	TW	12/11/2007	Memory System And Method With Serial And Parallel Modes
96148758.00	TW	12/19/2007	Hybrid Solid-State Memory System Having Volatile And Non-Volatile Memory
96148760.00	TW	12/19/2007	ID Generation Apparatus And Method For Serially Interconnected Devices
96149587.00	TW	12/21/2007	Independent Link And Bank Selection
97102393.00	TW	1/22/2008	Non-Volatile Semiconductor Memory Having Multiple External Power Supplies
97103130.00	TW	1/28/2008	Semiconductor Device And Method For Reducing Power Consumption In A System Having Interconnected Devices
97104918.00	TW	2/12/2008	Source Side Asymmetrical Precharge Programming Scheme
97105439.00	TW	2/15/2008	Apparatus And Method For Using A Page Buffer Of A Memory Device As A Temporary Cache
97105440.00	TW	2/15/2008	Apparatus And Method Of Page Program Operation For Memory Devices With Mirror Back-Up Of Data
97105441.00	TW	2/15/2008	Non-Volatile Memory With Dynamic Multi-Mode Operation
97106128.00	TW	2/21/2008	System And Method Of Page Buffer Operation For Memory Devices
97107920.00	TW	3/6/2008	Partial Block Erase Architecture For Flash Memory
N/A	TW	11/21/2007	Apparatus And Method For Processing Data In Serial Interconnection Configuration Of Memory Devices
10-2008-7010546	KR	9/29/2006	Multiple Independent Serial Link Memory
10-2008-7010548	KR	9/29/2006	Daisy Chain Cascading Devices
10-2008-7010560	KR	9/29/2006	Memory With Output Control
10/134,753	US	4/30/2002	Low Power Content Addressable Memory Architecture
11/565,170	US	11/30/2006	Flash Memory Program Inhibit Scheme
11/613,325	US	12/20/2006	Hybrid Solid-State Memory System Having Volatile And Non-Volatile Memory
11/613,563	US	12/20/2006	ID Generation Apparatus And Method For Serially Interconnected Devices
11/622,828	US	1/12/2007	Apparatus And Method For Producing Ids For Interconnected Devices Of Mixed Type
11/624,929	US	1/19/2007	Apparatus And Method For Producing Device Identifiers For Serially Interconnected Devices Of Mixed Type
11/637,175	US	12/12/2006	Memory System And Method With Serial And Parallel Modes
11/692,446	US	3/28/2007	Apparatus And Method For Producing Identifiers Regardless Of Mixed Device Type In A Serial Interconnection

11/692,452	US	3/28/2007	Apparatus And Method For Producing Device Identifiers For Serially Interconnected Devices Of Mixed Type
11/771,023	US	6/29/2007	Address Assignment And Type Recognition Of Serially Interconnected Memory Devices Of Mixed Type
11/771,241	US	6/29/2007	System And Method Of Operating Memory Devices Of Mixed Type
11/779,685	US	7/18/2007	Partial Block Erase Architecture For Flash Memory
11/822,496	US	7/6/2007	System And Method Of Page Buffer Operation For Memory Devices
11/829,410	US	7/27/2007	Non-Volatile Memory With Dynamic Multi-Mode Operation
11/873,475	US	10/17/2007	Single-Strobe Operation Of Memory Devices
11/942,173	US	11/19/2007	Apparatus And Method For Processing Data In Serial Interconnection Configuration Of Memory Devices
11/955,754	US	12/13/2007	Non-Volatile Semiconductor Memory Having Multiple External Power Supplies
12/018,272	US	1/23/2008	Semiconductor Device And Method For Reducing Power Consumption In A System Having Interconnected Devices
12/026,825	US	2/6/2008	Nonvolatile Semiconductor Memory
12/029,634	US	2/12/2008	Apparatus And Method For Using A Page Buffer Of A Memory Device As A Temporary Cache
12/030,235	US	2/13/2008	Apparatus And Method Of Page Program Operation For Memory Devices With Mirror Back-Up Of Data
12/042,551	US	3/5/2008	Nonvolatile Memory Having Non-Power Of Two Memory Capacity
12/115,784	US	5/6/2008	Power Supplies In Flash Memory Devices And Systems
60/949,993	US	7/16/2007	Non-Volatile Semiconductor Memory Having Multiple External Power Supplies
61/015,366	US	12/20/2007	Nonvolatile Semiconductor Memory Device Capable Of Multiple Mode Operations And Multiple Connection-Mode Operations
61/015,909	US	12/21/2007	Hierarchical Csl (Common Source Line) Structure In Nand Flash Memory
61/019,415	US	1/7/2008	Nand Flash Memory Having Multiple Cell Substrates
61/021,662	US	1/17/2008	Nonvolatile Memory Having Non-Power Of Two Memory Capacity
61/022,656	US	1/22/2008	Prefetched Input And Output Data In A Nonvolatile Memory
61/025,003	US	1/31/2008	Power Supply Configuration For Nand Flash Memory
61/025,920	US	2/4/2008	Nonvolatile Memory Having Configurable Device Organization
61/032,203	US	2/28/2008	Packaging Method For Serially Interconnected Memory Chips

61/035,791	US	3/12/2008	Flexible Multiple-Bank Operations In Nand Flash Nonvolatile Semiconductor Memory
10/809,421	US	3/26/2004	Hybrid Content Addressable Memory
11/324,023	US	12/30/2005	Multiple Independent Serial Link Memory
11/412,783	US	4/28/2006	Dynamic Random Access Memory With Fully Independent Partial Array Refresh Function
11/496,278	US	7/31/2006	Daisy Chain Cascading Device
11/583,354	US	10/19/2006	Memory With Output Control
11/594,564	US	11/8/2006	Daisy Chain Cascading Devices
11/639,375	US	12/14/2006	Nonvolatile Memory System
11/643,850	US	12/22/2006	Independent Link And Bank Selection
11/693,027	US	3/29/2007	Flash Memory System Control Scheme
11/715,838	US	3/8/2007	Non-Volatile Semiconductor Memory With Page Erase
11/750,649	US	5/18/2007	Apparatus And Method For Establishing Device Identifiers For Serially Interconnected Devices
11/762,330	US	6/13/2007	Flash Multi-Level Threshold Distribution Scheme
11/840,692	US	8/17/2007	Modular Command Structure For Memory And Memory System
11/843,440	US	8/22/2007	Scalable Memory System
11/944,535	US	11/23/2007	New Architecture And Circuit Details In Flash Memory
PCT/CA2006/001606	JP	9/29/2006	Multiple Independent Serial Link Memory
PCT/CA2006/001607	JP	9/29/2006	Daisy Chain Cascading Devices
PCT/CA2006/001609	JP	9/29/2006	Memory With Output Control
CA2007/000382	WO	3/8/2007	Power Supply Testing Architecture
PCT/CA2007/000478	WO	3/26/2007	Non-Volatile Semiconductor Memory With Page Erase
PCT/CA2007/000488	WO	3/26/2007	Non-Volatile Memory System
PCT/CA2007/000499	WO	3/28/2007	Dynamic Random Access Memory With Fully Independent Partial Array Refresh Function
PCT/CA2007/000501	WO	3/29/2007	Flash Memory System Control Scheme
PCT/CA2007/000891	WO	5/18/2007	Apparatus And Method For Establishing Device Identifiers For Serially Interconnected Devices
PCT/CA2007/001428	WO	8/20/2007	Modular Command Structure For Memory And Memory System
PCT/CA2007/001469	WO	8/22/2007	Scalable Memory System
PCT/CA2007/001621	WO	9/12/2007	Flash Multi-Level Threshold Distribution Scheme
PCT/CA2007/002092	WO	11/20/2007	Apparatus And Method For Processing Data In Serial Interconnection Configuration Of Memory Devices
PCT/CA2007/002125	WO	11/26/2007	New Architecture And Circuit Details In Flash Memory
PCT/CA2007/002147	WO	11/29/2007	Apparatus And Method For Producing Device Identifiers For Serially Interconnected Devices Of Mixed Type
PCT/CA2007/002149	WO	11/29/2007	Flash Memory Program Inhibit Scheme
PCT/CA2007/002167	WO	12/3/2007	ID Generation Apparatus And Method For Serially Interconnected Devices
PCT/CA2007/002171	WO	12/4/2007	Apparatus And Method For Producing Device Identifiers For Serially Interconnected Devices Of Mixed Type

PCT/CA2007/002173	WO	12/4/2007	Address Assignment And Type Recognition Of Serially Interconnected Memory Devices Of Mixed Type
PCT/CA2007/002182	WO	12/4/2007	System And Method Of Operating Memory Devices Of Mixed Typed
PCT/CA2007/002193	WO	12/4/2007	Apparatus And Method For Producing Identifiers Regardless Of Mixed Device Type In A Serial Interconnection
PCT/CA2007/002222	WO	12/10/2007	Memory System And Method With Serial And Parallel Modes
PCT/CA2007/002304	WO	12/18/2007	Hybrid Solid-State Memory System Having Volatile And Non-Volatile Memory
PCT/CA2007/002320	WO	12/21/2007	Independent Link And Bank Selection
PCT/CA2008/000120	WO	1/23/2008	Semiconductor Device And Method For Reducing Power Consumption In A System Having Interconnected Devices
PCT/CA2008/000232	WO	2/6/2008	Source Side Asymmetrical Precharge Programming Scheme
PCT/CA2008/000250	WO	2/12/2008	Apparatus And Method For Using A Page Buffer Of A Memory Device As A Temporary Cache
PCT/CA2008/000256	WO	2/12/2008	Non-Volatile Semiconductor Memory Having Multiple External Power Supplies
PCT/CA2008/000273	WO	2/13/2008	Apparatus And Method Of Page Program Operation For Memory Devices With Mirror Back-Up Of Data
PCT/CA2008/000285	WO	2/14/2008	Non-Volatile Memory With Dynamic Multi-Mode Operation
PCT/CA2008/000287	WO	2/15/2008	System And Method Of Page Buffer Operation For Memory Devices
N/A	WO	3/4/2008	Partial Block Erase Architecture For Flash Memory