PATENT ASSIGNMENT

Electronic Version v1.1
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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Mr. Peter Gillingham	06/18/2008

RECEIVING PARTY DATA

Name:	MOSAID Technologies Incorporated
Street Address:	11 Hines Road
City:	Kanata, Ontario
State/Country:	CANADA
Postal Code:	K2K 2X1

PROPERTY NUMBERS Total: 1

Property Type	Number
Patent Number:	5546350

CH $40.00 5546350

CORRESPONDENCE DATA

Fax Number: (613)591-8148
Correspondence will be sent via US Mail when the fax attempt is unsuccessful.
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Address Line 4: Kanata, Ontario, CANADA K2K 2X1

ATTORNEY DOCKET NUMBER:	1028-01US-000-20
NAME OF SUBMITTER:	Victoria Donnelly

Total Attachments: 5
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CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS

For and in consideration of agreement(s) duly entered into with my employer, MOSAID Technologies Incorporated ("Assignee"), an Ontario corporation, and/or other good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, on this 18th day of June, 2008, Peter Gillingham ("Assignor"), hereby confirms, selling, assigning, and transferring to Assignee, the full extent of all right, title, and interest in and to any and all of the following (collectively, the "Rights"):

1. The provisional patent applications, patent applications and/or patents listed in the attached Exhibit 'A' (the "Patents");

2. All inventions claimed or described in any or all of the Patents (collectively, the "Inventions");

3. All rights with respect to the Inventions, including all U.S. patents or other governmental grants or issuances that may be granted with respect to the Inventions or from any direct or indirect divisionals, continuations, continuations-in-part, or other patent applications claiming priority rights from the Patents ("Potential Patents");

4. All reissues, reexaminations, extensions, or registrations of the Patents or Potential Patents;

5. All non-United States patents, patent applications, and counterparts relating to any or all of the Inventions, the Patents, or Potential Patents, including, without limitation, certificates of invention, utility models, industrial design protection, design patent protection, and other governmental grants or issuances ("Foreign Rights"), and including the right to file foreign applications directly in the name of Assignee, its successors and assigns;

6. The right to claim priority rights deriving from the Patents;

7. All causes of action and remedies related to any or all of the Patents, the Inventions, Potential Patents, or Foreign Rights (including, without limitation, the right to sue for past, present, or future infringement, misappropriation or violation of rights related to any of the foregoing and the right to collect royalties and other payments under or on account of any of the foregoing); and

8. Any and all other rights and interests arising out of, in connection with, or in relation to the Patents, the Inventions, Potential Patents, or Foreign Rights.

9. Assignor will not sign any writing or do any act conflicting with this Assignment, and, will sign all documents and do such additional acts as Assignee, their successors, legal representatives, and assigns deem necessary or desirable to perfect enjoyment of the Rights, conduct proceedings regarding the Rights (including any litigation or interference proceedings), or perfect or defend title to the Rights. Assignee shall compensate Assignor for any reasonable, documented disbursements provided that Assignor shall have furnished Assignee an advance, written estimate of the fees and costs for such assistance and Assignee shall have agreed in

writing to pay such fees and costs. Assignor requests the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention, utility models, or other governmental grants or issuances that may be granted upon any of the Rights in the name of the Assignee, as the assignee to the entire interest therein.

10. Assignor authorizes the firm, where applicable, MOSAID Technologies Inccorporate and its agents to insert any further identification necessary to make this assignment suitable for recordation in the Patent Offices of any country as may be required.

11. The terms and conditions of this Assignment will inure to the benefit of Assignee, its successors, legal representatives, and assigns and will be binding upon Assignor, his successors, legal representatives and assigns.

By: _____
Peter Gillingham
Mosaid Technologies Incorporated

ATTESTATION

The undersigned witnessed the signature of Peter Gillingham to this document and makes the following statements:

1. Peter Gillingham is personally known to me (or proved to me on the basis of satisfactory evidence) and appeared before me on June 18, 2008 to execute this document.

2. Peter Gillingham subscribed to this document.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

By: Tammy Kelly
Print Name: Tammy Kelly

EXHIBIT "A"

Serial #	Country ID	Filed Date	Title
680,994	US	4/5/1991	High Voltage Boosted Wordline Supply Charge Pump And Regulator For DRAM
134,621	US	10/12/1993	High Voltage Boosted Wordline Supply Charge Pump And Regulator For DRAM
684,252	US	7/19/1996	High Voltage Boosted Wordline Supply Charge Pump And Regulator For DRAM
921,579	US	9/2/1997	High Voltage Boosted Wordline Supply Charge Pump And Regulator For DRAM
09/178,977	US	10/26/1998	High Voltage Boosted Wordline Supply Charge Pump And Regulator For DRAM
09/483,626	US	1/14/2000	High Voltage Boosted Word Line Supply Charge Pump And Regulator For DRAM
09/819,488	US	3/28/2001	High Voltage Boosted Word Line Supply Charge Pump And Regulator For DRAM
10/056,837	US	1/24/2002	High Voltage Boosted Word Line Supply Charge Pump And Regulator For DRAM
10/463,218	US	6/17/2003	Boosted Voltage Supply
10/032,431	US	12/21/2001	Dynamic Random Access Memory Using Imperfect Isolating Transistors
667,880	US	3/12/1991	Bandgap Voltage Generator
08/595,020	US	1/31/1996	REISSUE Of Patent 5,283,761 Method For Multi-Level DRAM Sense And Restore
09/654,367	US	9/1/2000	Method Of Multi-Level Storage In Dram And Apparatus Thereof
226,035	US	4/11/1994	Ram Variable Size Block Write
08/253,271	US	6/2/1994	Single Chip Frame Buffer And Graphics Accelerator
09/434,331	US	11/5/1999	Single Chip Frame Buffer And Graphics Accelerator - RE-ISSUE APPLICATION
10/264,013	US	10/4/2002	Single Chip Frame Buffer And Graphics Accelerator
11/872,353	US	11/29/1995	Single Chip Display Controller Frame Buffer And Output Pixel Logic System - Assigned To Accelerix
08/319,042	US	10/6/1994	Delay Locked Loop Implementation In A Synchronous Dynamic Random Access Memory
09/392,088	US	9/8/1999	Delay Locked Loop Implementation In A Synchronous Dynamic Random Access Memory
10/348,062	US	1/17/2003	Delay Locked Loop Implementation In A Synchronous Dynamic Random Access Memory
355,957	US	12/14/1994	Flexible Dram Array
597,510	US	2/2/1996	Flexible Dram Array
366,921	US	12/30/1994	Method For Multi-Level DRAM Sense And Restore
584,887	US	1/11/1996	Method For Multi-Level DRAM Sense And Restore MOS95-03A
09/000,968	US	12/30/1997	Bist Memory Test System

11/906,756	US	10/3/2007	High Bandwidth Memory Interface
11/978,988	US	10/30/2007	High Bandwidth Memory Interface
11/978,896	US	10/30/2007	Apparatuses For Synchronous Transfer Of Information
09/182,494	US	10/30/1998	High Bandwidth Memory Interface
10/247,821	US	9/20/2002	High Bandwidth Memory Interface
10/919,491	US	8/17/2004	High Bandwidth Memory Interface
09/533,128	US	3/23/2000	Dynamic Content Addressable Memory Cell
09/977,982	US	10/17/2001	Dynamic Content Addressable Memory Cell
10/258,580	US	3/10/2003	Matchline Sense Circuit And Method
11/269,659	US	11/9/2005	Matchline Sense Circuit And Method
10/357,394	US	2/4/2003	Searchline Control Circuit And Power Reduction Method
10/134,753	US	4/30/2002	Low Power Content Addressable Memory Architecture
10/262,643	US	9/30/2002	Dense Mode Coding Scheme
11/969,521	US	1/4/2008	Dense Mode Coding Scheme
226,033	US	4/11/1994	Dram Page Copy Method
09/750,068	US	12/29/2000	Memory-Logic Semiconductor Device
10/856,783	US	6/1/2004	Ternary Cam Cell For Reduced Matchline Capacitance
11/534,873	US	9/25/2006	Compare Circuit For A Content Addressable Memory Cell
11/925,208	US	10/26/2007	Compare Circuit For A Content Addressable Memory Cell
60/949,993	US	7/16/2007	Non-Volatile Semiconductor Memory Having Multiple External Power Supplies
11/955,754	US	12/13/2007	Non-Volatile Semiconductor Memory Having Multiple External Power Supplies
11/477,659	US	6/30/2006	Synchronous Memory Read Data Capture
12/032,249	US	2/15/2008	Clock Mode Determination In A Memory System
11/843,024	US	8/22/2007	Reduced Pin Count Interface
61/019,907	US	1/9/2008	Timing And Clocking Method In A System Having A Plurality Of Devices
2781031.6	FR	12/5/2002	Low Power Content Addressable Memory Architecture
95105181.2	FR	4/6/1995	Dram Page Copy Method
95105180.4	FR	4/6/1995	Ram Variable Size Block Write
95309490	GB	12/28/1995	Method For Multi-Level DRAM Sense And Restore MOS95-03A
1255244.4	GB	3/30/2000	Dynamic Content Addressable Memory Cell
225063.7	GB	5/1/2001	Matchline Sense Circuit And Method
95105181.2	GB	4/6/1995	Dram Page Copy Method
95105180.4	GB	4/6/1995	Ram Variable Size Block Write
2781031.6	EP	12/5/2002	Low Power Content Addressable Memory Architecture
95309490.1	EP	12/28/1995	Method For Multi-Level DRAM Sense And Restore MOS95-03A
1401381.7	EP	5/25/2001	Memory-Logic Semiconductor Device
95105180.4	EP	4/6/1995	Ram Variable Size Block Write
95105181.2	EP	4/6/1995	Dram Page Copy Method
2007-513634	JP	12/1/2006	Ternary Cam Cell For Reduced Matchline Capacitance
2002-300220	JP	6/1/1995	Single Chip Frame Buffer And Graphic Accelerator

135297/1995	JP	6/1/1995	Single Chip Frame Buffer And Graphics Accelerator
2008-023690	JP	6/1/1995	Single Chip Frame Buffer And Graphic Accelerator
2000-610011	JP	3/30/2000	Dynamic Content Addressable Memory Cell
352932/1995	JP	12/29/1995	Method For Multi-Level DRAM Sense And Restore
2000-155585	JP	5/26/2000	Memory-Logic Semiconductor Device
073380/1991	JP	4/6/1991	High Voltage Boosted Wordline Supply Charge Pump And Regulator For DRAM
95105181.2	IT	4/6/1995	Dram Page Copy Method
95105180.4	IT	4/6/1995	Ram Variable Size Block Write
2781031.6	DE	12/5/2002	Low Power Content Addressable Memory Architecture
10196141.3	DE	5/1/2001	Matchline Sense Circuit And Method
95309401.1	DE	12/28/1995	Method For Multi-Level DRAM Sense And Restore MOS95-03A
10084440.5	DE	3/30/2000	Dynamic Content Addressable Memory Cell
2,212,089	CA	7/31/1997	Bist Memory Test System
2,266,062	CA	3/31/1999	Dynamic Content Addressable Memory Cell
2,307,240	CA	5/1/2000	Matchline Sense Circuit And Method
2,313,275	CA	6/30/2000	Searchline Control And Power Reduction Method
10-2006-70279091	KR	12/29/2006	Improved Ternary CAM Cell For Reduced ML Capacitance
2001-209	KR	1/3/2001	Memory-Logic Semiconductor Device
2001-7012599	KR	3/30/2000	Dynamic Content Addressable Memory Cell
1811709	CN	5/1/2001	Matchline Sense Circuit And Method
200580025684.X	CN	1/29/2007	Ternary Cam Cell For Reduced Matchline Capacitance
2828188.8	CN	12/5/2002	Low Power Content Addressable Memory Architecture
2781031.6	NL	12/5/2002	Low Power Content Addressable Memory Architecture
97105559	TW	2/18/2008	Clock Mode Determination In A Memory System
90110312	TW	4/30/2001	Memory-Logic Semiconductor Device
97102393	TW	1/22/2008	Non-Volatile Semiconductor Memory Having Multiple External Power Supplies
91137612	TW	12/27/2002	Low Power Content Addressable Memory Architecture
96118239	TW	5/22/2007	Synchronous Memory Read Data Capture
PCT/CA2007/000787	WO	5/7/2007	Synchronous Memory Read Data Capture
PCT/CA2008/000256	WO	2/12/2008	Non-Volatile Semiconductor Memory Having Multiple External Power Supplies
PCT/CA2008/000292	WO	2/15/2008	Clock Mode Determination In A Memory System
PCT/CA2007/001789	WO	10/10/2007	Reduced Pin Count Interface