PATENT ASSIGNMENT

Electronic Version v1.1 Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY AGREEMENT

CONVEYING PARTY DATA

Name	Execution Date
Daniel E. Leckrone	12/14/2007
ChipScale, Inc.	12/14/2007
Technology Properties Limited	12/14/2007

RECEIVING PARTY DATA

Name:	Phil P. Marcoux
Street Address:	335 Chatham Way
City:	Mountain View
State/Country:	CALIFORNIA
Postal Code:	94040

PROPERTY NUMBERS Total: 18

Property Type	Number
Patent Number:	5280194
Patent Number:	5403729
Patent Number:	5441898
Patent Number:	5444009
Patent Number:	5521420
Patent Number:	5592022
Patent Number:	5455187
Patent Number:	5557149
Patent Number:	5656547
Patent Number:	5789817
Patent Number:	5904496
Patent Number:	6051489
Patent Number:	6121119
	DATENT

PATENT "
REEL: 021243 FRAME: 0894

500595389

Patent Number:	6355981	
Patent Number:	6414585	
Patent Number:	6954130	
Patent Number:	6833986	
Patent Number:	6946734	

CORRESPONDENCE DATA

Fax Number: (408)850-3280

Correspondence will be sent via US Mail when the fax attempt is unsuccessful.

Phone: 650-274-7762
Email: oneppm@aol.com
Correspondent Name: Phil Marcoux
Address Line 1: 335 Chatham Way

Address Line 4: Mountain View, CALIFORNIA 94040

NAME OF SUBMITTER: Phil P. Marcoux

Total Attachments: 10

source=ChipScale Security Agreement.2007-12-14#page1.tif source=ChipScale Security Agreement.2007-12-14#page2.tif source=ChipScale Security Agreement.2007-12-14#page3.tif source=ChipScale Security Agreement.2007-12-14#page4.tif source=ChipScale Security Agreement.2007-12-14#page5.tif source=ChipScale Security Agreement.2007-12-14#page6.tif source=ChipScale Security Agreement.2007-12-14#page7.tif source=ChipScale Security Agreement.2007-12-14#page8.tif source=ChipScale Security Agreement.2007-12-14#page9.tif

source=ChipScale Security Agreement.2007-12-14#page10.tif

SECURITY AGREEMENT

This SECURITY AGREEMENT, dated as of <u>Parabola</u>, 2007 (this "Security Agreement"), is executed by Chipscale, Inc., a California corporation ("Company") and Daniel Leckrone ("Purchaser"), in favor of Phil Marcoux as the sellers' representative (the "Sellers' Representative") for the benefit of and on behalf of each of the individuals set forth on Schedule 1 (each a "Seller" and collectively, the "Sellers"). Capitalized terms used but not defined herein have the meanings ascribed to them in the Purchase Agreement (as defined below).

RECITALS

- A. The parties hereto have entered into that certain Amended and Restated Purchase Agreement date as of the date hereof (the "Purchase Agreement"), with Technology Properties Limited and each of the Sellers pursuant to which the Sellers have agreed to sell all of the outstanding capital stock of the Company (the "Company Stock") to Purchaser.
- B. Pursuant to the terms of the Purchase Agreement, the Purchaser has agreed to pay Purchase Price over a period of time as more fully set forth in Article I of the Purchase Agreement. In order to induce the Sellers to accept such deferred payments, the Purchaser has agreed (i) to pledge the Company Stock as collateral for the unpaid portion of the Purchase Price and (ii) to cause the Company to grant a security interest in all of its assets as collateral for the unpaid portion of the Purchase Price, in each case, pursuant to the terms of this Security Agreement.
- C. Pursuant to the Purchase Agreement, the Sellers have appointed the Seller's Representative as their agent with respect to the Security Agreement.

AGREEMENT

NOW, THEREFORE, in consideration of the above recitals and for other good and valuable consideration, the receipt and adequacy of which are hereby acknowledged, the Purchaser and the Company hereby agree with the Sellers' Representative as follows:

- 1. <u>Definitions and Interpretation</u>. Unless otherwise defined herein, all terms defined in the California Uniform Commercial Code (the "UCC") shall have the respective meanings given to those terms in the UCC.
- 2. <u>The Pledge</u>. To secure the Obligations as defined in Section 4 hereof, Purchaser hereby pledges to Sellers' Representative for the benefit of the Sellers, a security interest in all of the Purchaser's right, title and interest, whether now owned or hereafter acquired, in all of the following (the "Pledged Collateral"): the securities of the Company, together with any additional securities of the Company hereafter acquired by the Purchaser (collectively, the "Pledged Securities").
- 3. <u>The Security Interest</u>. To secure the Obligations as defined in Section 4 hereof, the Company hereby grants to Sellers' Representative for the benefit of the Sellers, a security interest in, all of the Company's right, title and interest, whether now owned or hereafter acquired, in all of the property or assets of the Company (collectively, the "Collateral"), including the patents listed on the Schedule 2 hereto.

Chipscale Security Agreement FINAL REV 1 2007-08-27.doc

- 4. <u>Security for Obligations</u>. The obligations secured by this Security Agreement (the "Obligations") shall mean the payment of the unpaid portion of the Purchase Price.
- 5. <u>Further Assurances</u>. The Purchaser and the Company each hereby agree that at any time and from time to time, such parties will promptly execute and deliver all further instruments and documents, including without limitation all additional Pledged Securities, and take all further action that the Sellers' Representative may reasonably request, in order to perfect and protect any security interest granted hereby. Seller's Representative shall promptly take all action necessary or the Company reasonably deems necessary with respect to any Pledged Collateral or Collateral upon full payment of the Purchase Price.
- 6. <u>Sellers' Representative Appointed Attorney-in-Fact</u>. The Purchaser and the Company each hereby appoint Sellers' Representative as their attorney-in-fact, with full authority in the place and stead of such parties and in the name of such parties, from time to time in Sellers' Representative's reasonable discretion and to the full extent permitted by law to take any action and to execute any instrument which is necessary to accomplish the purposes of this Security Agreement in accordance with the terms and provisions hereof. The powers conferred on Sellers' Representative hereunder are solely to protect its interests in the Pledged Collateral and the Collateral and shall not impose any duty upon Sellers' Representative to exercise any such powers.

7. Miscellaneous.

- (a) <u>Event of Default</u>. Any breach of Purchaser's payment obligation under the Purchase Agreement shall constitute a default hereunder and Seller's Representative, for and on behalf of the Sellers, shall have all of the rights of a secured party hereunder and under applicable law.
- (b) <u>Notices</u>. All notices shall be made in the manner provided in the Purchase Agreement.
- (c) <u>Nonwaiver</u>. No failure or delay on Sellers' Representative's part in exercising any right hereunder shall operate as a waiver thereof or of any other right nor shall any single or partial exercise of any such right preclude any other further exercise thereof or of any other right.
- (d) <u>Amendments and Waivers</u>. This Security Agreement may not be amended or modified, nor may any of its terms be waived, except by written instruments signed by Sellers' Representative, the Purchaser and the Company. Each waiver or consent under any provision hereof shall be effective only in the specific instances for the purpose for which given.
- (e) <u>Assignments</u>. This Security Agreement shall be binding upon and inure to the benefit of Sellers' Representative for the benefit of the Sellers, the Purchaser and the Company and their respective successors and assigns; provided, however, that the Purchaser and the Company may not assign its rights and duties hereunder without the prior written consent of Sellers' Representative.
- (f) <u>Cumulative Rights, etc.</u> The rights, powers and remedies of Sellers' Representative under this Security Agreement shall be in addition to all rights, powers and remedies given to Sellers' Representative virtue of any applicable law, rule or regulation of any governmental authority, or any other agreement, all of which rights, powers, and remedies shall be cumulative and

may be exercised successively or concurrently without impairing Sellers' Representative's rights hereunder.

- (g) <u>Governing Law</u>. This Security Agreement shall be governed by and construed in accordance with the laws of the State of California without reference to conflicts of law rules (except to the extent governed by the UCC).
- (h) <u>Counterparts</u>. This Security Agreement may be executed in multiple counterparts, each of which shall be deemed an original, and all of such counterparts shall constitute but one instrument.

[Signature Page Follows]

IN WITNESS WHEREOF, Debtor	r has caused this Security Agreement to be executed as of
the day and year first above written.	DANIEL LECKRONE
	CHIPSCALE, INC., a California corporation
	By:
	Name:
	Title:
ACKNOWLEDGED AND AGREED:	
PHIL MARCOUX, as Sellers' Representation for the benefit of and on behalf of the Selle	

IN WITNESS	WHEREOF,	Debtor has	caused	this Se	ecurity.	Agreement	to be	executed	as :	οĚ
the day and year first a	above written	•			•	~				

DANIEL LECKRONE

CHIPSCALE, INC., a California corporation

By: <u>(2//</u>

Name: Billy L. LONG

Title: //(CS/) E/V T

ACKNOWLEDGED AND AGREED:

PHIL MARCOUX, as Sellers' Representative

for the benefit of and on behalf of the Sellers

SCHEDULE 1

TO SECURITY AGREEMENT

<u>SELLERS</u>

1520 Partners

Allan Johnson

Annette Severiens, J.C. Severiens Trust

Chuck Harwood

Don Bolton

Don Richmond

Doug Peltzer

Groom and Cave

James Young

Lida Urbanek

Michael Lancaster

Mpulse Microwave, Inc.

Paul Franklin

Phil Marcoux

Richard H. Vaccarello

Jennifer DeGolia

Rick DeGolia

Wendell Sander

WS Investment Company 96A

SCHEDULE 2

TO SECURITY AGREEMENT

SCHEUDLE OF PATENTS

(see attached)

Chipscale Security Agreement FINAL REV 1 2007-08-27.doc

Schedule of Chipscale Patents

	<u>EXPIRES</u> 1/18/2011	4/4/2012	8/15/2012 8/22/2012	5/28/2013	1/7/2014	10/3/2012	9/17/2013	8/12/2014	8/4/2018		cidillo Del 🖟
0	ISSUED 1/18/1994	4/4/1995	8/22/1995	9/28/1996	1/1/1997	10/3/1995	9/17/1996	8/12/1997	8/4/1998		COC
0 ~ SO	<u>FILED</u> 9/04/1992	5/27/1992	12/23/1994	7/5/1994	7/5/1994	11/1/1994	3/24/1995	5/11/1994	11/15/1996		
Allowed: In Process:	PRIORIT Y	æ ,	= =	æ	e.	****		*	77] <u>t</u>	
Pending: US - 0 Non US - 2 (P005FRG, P005JP)	Electrical apparatus with a metallic layer coupled to a lower region of a substrate and metallic layer coupled to a lower region of a semiconductor device.	Fabricating a semiconductor with an insulative coating	rapricating a semiconductor with an insulative coating Fabricating a semiconductor with an	insulative coating Fabricating a semiconductor with an	insulative coating Fabricating a semiconductor with an	insutative coatring Method of making a semiconductor device with a metallic layer coupled	to a lower region of a substrate and metallic layer coupled to a lower region of a semiconductor device Semiconductor fabrication with	contact processing for wrap-around flange interface Method for making a leadless surface	flange interface contacts Electrical apparatus with a metallic layer coupled to a lower region of a	device	
US - 20 Non US - 14	<u>PAT NO</u> 5,280,194	5,403,729	5,441,898	5,521,420	5,592,022	5,455,187	5,557,149	5,656,547	5,789,817		Schedule
Issued:	PAT IUR FAM US	US	s sa	SO	SA	Sn	Si	SO	Sn		Chipscale Patent Schedule

No.	Š.	, L	Area of the second
		€ DEL	-
	22	ë T	Ť

EXPIRES	5/18/2019	6/8/2019	4/18/2020	9/19/2070	4/24/2023	3/12/2022	7/2/2022	10/11/2025	12/21/2024	9/20/2025	6/23/2017	6/23/2020	3/20/2015	11/16/2015 9/16/2015	11/18/2015 11/18/2018 1/16/2022
ISSUED	5/18/1999	6661/8/9	4/18/2000	9/19/2000	4/24/2001	3/12/2002	7/2//2002	10/11/2005	12/21/2004	9/20/2005	6/23/2000	6/23/2000	3/20/1998	9/16/1998	11/18/1998 11/18/1998 1/16/2002
	1/24/1997	1/24/1997	5/13/1997	5/29/1997	6/26/1998	1/21/1999	5/13/1997	2/7/2002	2/20/2004	2/20/2004	4/27/1995	11/30/1998	4/27/1995	6/1/1995 4/27/1995	6/1/1995 11/7/1997 1/26/1998
DESCRIPTION PRIORITY V	Wafer fabrication of inside-wrapped	Contacts for electronic devices. Wafer fabrication of die-bottom	contacts for electronic devices Electronic component package with	substrate Resistor fabrication	Wafer fabrication of die-bottom	contacts for electronic devices Wafer fabrication of inside-wrapped	contacts for electronic devices Integrated passive components and	package with posts Integrated passive components and	package with posts Integrated passive components and	package with posts Integrated passive components and	package with posts Semiconductor fabrication with	contact processing for wrap-around flange interface Resistor fabrication	Semiconductor fabrication with contact processing for wrap-around	nange interface Resistor fabrication Semiconductor fabrication with contact processing for wrap-around	flange interface Resistor fabrication Resistor fabrication Wafer fabrication of inside-wrapped contacts for electronic devices
PATNO	5,904,496	5,910,687	6,051,489	6,121,119	6,221,751	6,355,981	6,414,585	6,954,130	6,833,986	6,946,734	HK1012776	HK1011454	34858 (WO95/31829)	34853 GB2302210	GB2302452 GB2316541 GB2337636
PAT JUR FAM	SA	SA	US	ŝû	SI	Sú	Š	Ŝ	Sn	Sin	Ħ	HK	Singapore	Singapore UK	ď

Chipscale Patent Schedule

EXPIRES	12/19/2021	4/3/2022	8/21/2022	12/24/2014	6/21/2019	10/14/2019	2/20/2026	9750/507/2
ISSUED	12/19/2001	4/3/2002	8/21/2002	12/24/1997	6/21/2002	10/14/2002	2/20/2006	2/20/2006
<u>ETLED</u>	1/26/1998	2/13/1998	5/13/1998	11/20/1989	4/27/1.995	\$661/1/9	8/13/1998	5/13/1998
DESCRIPTION PRIORIT	Wafer fabrication of die-bottom contacts for electronic devices	Integrated passive components and nackage with nosts	electronic component package with osts on the active side of the	substrate An Improved Beam Leads for Schottky-barrier diodes	emiconductor fabrication with ontact processing for wrap-around ange interface	esistor fabrication	Electronic component package with posts on the active side of the	substrate Integrated passive components and package with posts
<u>PAT NO</u>	GB2336034	GB2341003	GB2341277		343030	358446	10-0555241	10-0555237
PAT JUR FAM	K	¥	Ä	South Korea	South Korea	South Korea	South Korea	South Korea

and all additions, changes, amendments, modifications, actions, counterparts, continuations, continuations-in-part, extensions, reissues, divisionals This Schedule of Patents shall be deemed to include the items listed above, as well as all progenitors, progeny and enhancements thereof, and/or renewals of such progenitors, progeny and enhancements.

Chipscale Patent Schedule

50