PATENT ASSIGNMENT

Electronic Version v1.1
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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Mr. HakJune Oh	06/23/2008

RECEIVING PARTY DATA

Name:	MOSAID Technologies Incorporated
Street Address:	11 Hines Road
City:	Kanata, Ontario
State/Country:	CANADA
Postal Code:	K2K 2X1

PROPERTY NUMBERS Total: 3

Property Type	Number
Application Number:	11959996
Application Number:	11843440
Application Number:	11637175

CH $120.00 11959996

CORRESPONDENCE DATA

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ATTORNEY DOCKET NUMBER:	1251-02 1271-01 1228-01US
NAME OF SUBMITTER:	Victoria Donnelly

Total Attachments: 7
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CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS

For and in consideration of agreement(s) duly entered into with my employer, MOSAID Technologies Incorporated ("Assignee"), an Ontario corporation, and/or other good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, on this 23 day of June, 2008, HakJune Oh, ("Assignor"), hereby confirms, selling, assigning, and transferring to Assignee, the full extent of all right, title, and interest in and to any and all of the following (collectively, the "Rights"):

1. The provisional patent applications, patent applications and/or patents listed in the attached Exhibit 'A' (the "Patents");

2. All inventions claimed or described in any or all of the Patents (collectively, the "Inventions");

3. All rights with respect to the Inventions, including all U.S. patents or other governmental grants or issuances that may be granted with respect to the Inventions or from any direct or indirect divisionals, continuations, continuations-in-part, or other patent applications claiming priority rights from the Patents ("Potential Patents");

4. All reissues, reexaminations, extensions, or registrations of the Patents or Potential Patents;

5. All non-United States patents, patent applications, and counterparts relating to any or all of the Inventions, the Patents, or Potential Patents, including, without limitation, certificates of invention, utility models, industrial design protection, design patent protection, and other governmental grants or issuances ("Foreign Rights"), and including the right to file foreign applications directly in the name of Assignee, its successors and assigns;

6. The right to claim priority rights deriving from the Patents;

7. All causes of action and remedies related to any or all of the Patents, the Inventions, Potential Patents, or Foreign Rights (including, without limitation, the right to sue for past, present, or future infringement, misappropriation or violation of rights related to any of the foregoing and the right to collect royalties and other payments under or on account of any of the foregoing); and

8. Any and all other rights and interests arising out of, in connection with, or in relation to the Patents, the Inventions, Potential Patents, or Foreign Rights.

9. Assignor will not sign any writing or do any act conflicting with this Assignment, and, will sign all documents and do such additional acts as Assignee, their successors, legal representatives, and assigns deem necessary or desirable to perfect enjoyment of the Rights, conduct proceedings regarding the Rights (including any litigation or interference proceedings), or perfect or defend title to the Rights. Assignee shall compensate Assignor for any reasonable, documented disbursements provided that Assignor shall have furnished Assignee an advance, written estimate of the fees and costs for such assistance and Assignee shall have agreed in writing to pay such fees and costs. Assignor requests the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention,

utility models, or other governmental grants or issuances that may be granted upon any of the Rights in the name of the Assignee, as the assignee to the entire interest therein.

10. Assignor authorizes the firm, where applicable, MOSAID Technologies Incorporated and its agents to insert any further identification necessary to make this assignment suitable for recordation in the Patent Offices of any country as may be required.

11. The terms and conditions of this Assignment will inure to the benefit of Assignee, its successors, legal representatives, and assigns and will be binding upon Assignor, his successors, legal representatives and assigns.

By: _____
HakJune Oh
Mosaid Technologies Incorporated

ATTESTATION

The undersigned witnessed the signature of HakJune Oh to this document and makes the following statements:

1. HakJune Oh is personally known to me (or proved to me on the basis of satisfactory evidence) and appeared before me on June 23, 2008, to execute this document.

2. HakJune Oh subscribed to this document.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

By: _____
Print Name: Tammy Kelly

EXHIBIT "A"

Serial #	Country ID	Filed Date	Title
6790596.8	EP	8/29/2006	Semiconductor Integrated Circuit Having Current Leakage Reduction Scheme
6790773.3	EP	9/29/2006	Memory With Output Control
6790843.4	EP	10/12/2006	Dynamic Random Access Memory Device And Method For Self-Refreshing Memory Cells
8006223.5	EP	9/29/2006	Daisy Chain Cascading Devices
8006224.3	EP	9/29/2006	Daisy Chain Cascading Devices
8006225	EP	9/29/2006	Daisy Chain Cascading Devices
PCT/CA2006/001953	EP	11/30/2006	Semiconductor Integrated Circuit Having Low Power Consumption With Self-Refresh
95129818	TW	8/14/2006	Semiconductor Integrated Circuit Having Current Leakage Reduction Scheme
95136448	TW	9/29/2006	Memory With Output Control
95138232	TW	10/17/2006	Dynamic Random Access Memory Device And Method For Self-Refreshing Memory Cells
95141969	TW	11/13/2006	Semiconductor Integrated Circuit Having Low Power Consumption With Self-Refresh
95144215	TW	11/29/2006	Apparatus And Method For Self-Refreshing Dynamic Random Access Memory Cells
96112915	TW	4/12/2007	Dynamic Random Access Memory With Fully Independent Partial Array Refresh Function
96118202	TW	5/22/2007	Apparatus And Method For Establishing Device Identifiers For Serially Interconnected Devices
96123864	TW	6/29/2007	Method Of Configuring Non-Volatile Memory For A Hybrid Disk Drive
96130974	TW	8/21/2007	Modular Command Structure For Memory And Memory System
96131131	TW	8/22/2007	Scalable Memory System
96134886	TW	9/18/2007	Packet Based Id Generation For Serially Interconnected Devices
96145941	TW	12/3/2007	Apparatus And Method For Producing Device Identifiers For Serially Interconnected Devices Of Mixed Type
96146276	TW	12/5/2007	Apparatus And Method For Producing Device Identifiers For Serially Interconnected Devices Of Mixed Type
96146278	TW	12/5/2007	Apparatus And Method For Producing Identifiers Regardless Of Mixed Device Type In A Serial Interconnection
96146482	TW	12/6/2007	Address Assignment And Type Recognition Of Serially Interconnected Memory Devices Of Mixed Type
96146483	TW	12/6/2007	System And Method Of Operating Memory Devices Of Mixed Typed
96146527	TW	12/6/2007	Apparatus And Method For Capturing Serial Input Data

96147300	TW	12/11/2007	Memory System And Method With Serial And Parallel Modes
96148760	TW	12/19/2007	ID Generation Apparatus And Method For Serially Interconnected Devices
96149587	TW	12/21/2007	Independent Link And Bank Selection
97103130	TW	1/28/2008	Semiconductor Device And Method For Reducing Power Consumption In A System Having Interconnected Devices
97105439	TW	2/15/2008	Apparatus And Method For Using A Page Buffer Of A Memory Device As A Temporary Cache
97105440	TW	2/15/2008	Apparatus And Method Of Page Program Operation For Memory Devices With Mirror Back-Up Of Data
97105557	TW	2/18/2008	System Having One Or More Memory Devices
97106128	TW	2/21/2008	System And Method Of Page Buffer Operation For Memory Devices
N/A	TW	11/21/2007	Apparatus And Method For Processing Data In Serial Interconnection Configuration Of Memory Devices
N/A	TW	2/8/2008	Methods And Apparatus For Clock Synchronization In A Configuration Of Series-Connected Semiconductor Devices
200680036477.90	CN	8/29/2006	Semiconductor Integrated Circuit Having Current Leakage Reduction Scheme
200680040549.70	CN	10/12/2006	Dynamic Random Access Memory Device And Method For Self-Refreshing Memory Cells
PCT/CA2006/001953	CN	11/30/2006	Semiconductor Integrated Circuit Having Low Power Consumption With Self-Refresh
10-2008-7009975	KR	8/29/2006	Semiconductor Integrated Circuit Having Current Leakage Reduction Scheme
10-2008-7010548	KR	9/29/2006	Daisy Chain Cascading Devices
10-2008-7010560	KR	9/29/2006	Memory With Output Control
N/A	KR	11/30/2006	Semiconductor Integrated Circuit Having Low Power Consumption With Self-Refresh
PCT/CA2006/001688	KR	10/12/2006	Dynamic Random Access Memory Device And Method For Self-Refreshing Memory Cells
11/238,975	US	9/30/2005	Semiconductor Integrated Circuit Having Current Leakage Reduction Scheme
11/866,035	US	10/2/2007	Semiconductor Integrated Circuit Having Current Leakage Reduction Scheme
11/289,428	US	11/30/2005	Semiconductor Integrated Circuit Having Low Power Consumption With Self-Refresh
11/261,493	US	10/31/2005	Dynamic Random Access Memory Device And Method For Self-Refreshing Memory Cells
12/038,855	US	2/28/2008	Dynamic Random Access Memory Device And Method For Self-Refreshing Memory Cells
11/319,451	US	12/29/2005	Apparatus And Method For Self-Refreshing Dynamic Random Access Memory Cells
11/930,292	US	10/31/2007	Apparatus And Method For Self-Refreshing Dynamic Random Access Memory Cells
11/412,783	US	4/28/2006	Dynamic Random Access Memory With Fully Independent Partial Array Refresh Function

11/428,050	US	6/30/2006	Method Of Configuring Non-Volatile Memory For A Hybrid Disk Drive
11/750,649	US	5/18/2007	Apparatus And Method For Establishing Device Identifiers For Serially Interconnected Devices
11/622,828	US	1/12/2007	Apparatus And Method For Producing Ids For Interconnected Devices Of Mixed Type
11/594,564	US	11/8/2006	Daisy Chain Cascading Devices
11/643,850	US	12/22/2006	Independent Link And Bank Selection
11/583,354	US	10/19/2006	Memory With Output Control
11/529,293	US	9/29/2006	Packet Based Id Generation For Serially Interconnected Devices
11/771,023	US	6/29/2007	Address Assignment And Type Recognition Of Serially Interconnected Memory Devices Of Mixed Type
11/771,241	US	6/29/2007	System And Method Of Operating Memory Devices Of Mixed Type
11/567,551	US	12/6/2006	Apparatus And Method For Capturing Serial Input Data
11/613,563	US	12/20/2006	ID Generation Apparatus And Method For Serially Interconnected Devices
11/822,496	US	7/6/2007	System And Method Of Page Buffer Operation For Memory Devices
12/030,235	US	2/13/2008	Apparatus And Method Of Page Program Operation For Memory Devices With Mirror Back-Up Of Data
11/624,929	US	1/19/2007	Apparatus And Method For Producing Device Identifiers For Serially Interconnected Devices Of Mixed Type
11/692,452	US	3/28/2007	Apparatus And Method For Producing Device Identifiers For Serially Interconnected Devices Of Mixed Type
12/018,272	US	1/23/2008	Semiconductor Device And Method For Reducing Power Consumption In A System Having Interconnected Devices
11/692,446	US	3/28/2007	Apparatus And Method For Producing Identifiers Regardless Of Mixed Device Type In A Serial Interconnection
11/942,173	US	11/19/2007	Apparatus And Method For Processing Data In Serial Interconnection Configuration Of Memory Devices
11/840,692	US	8/17/2007	Modular Command Structure For Memory And Memory System
11/959,996	US	12/19/2007	Methods And Apparatus For Clock Synchronization In A Configuration Of Series-Connected Semiconductor Devices
11/843,440	US	8/22/2007	Scalable Memory System
11/637,175	US	12/12/2006	Memory System And Method With Serial And Parallel Modes
61/013,036	US	12/12/2007	Memory System With Point-To-Point Ring Topology
11/779,587	US	7/18/2007	Memory With Data Control
11/897,105	US	8/29/2007	Daisy-Chain Memory Configuration And Usage

12/029,634	US	2/12/2008	Apparatus And Method For Using A Page Buffer Of A Memory Device As A Temporary Cache
61/015,724	US	12/21/2007	Method And Apparatus For Power Saving In Memory Device With Dll
61/048,737	US	4/29/2008	Non-Volatile Semiconductor Memory Device With Power Saving Feature
12/033,577	US	2/19/2008	System Having One Or More Memory Devices
61/032,203	US	2/28/2008	Packaging Method For Serially Interconnected Memory Chips
61/032,672	US	2/29/2008	Bit Line Precharge Voltage Control In Low Power Consumption Mode
PCT/CA2006/001417	JP	8/29/2006	Semiconductor Integrated Circuit Having Current Leakage Reduction Scheme
PCT/CA2006/001607	JP	9/29/2006	Daisy Chain Cascading Devices
PCT/CA2006/001609	JP	9/29/2006	Memory With Output Control
PCT/CA2006/001688	JP	10/12/2006	Dynamic Random Access Memory Device And Method For Self-Refreshing Memory Cells
PCT/CA2006/001953	JP	11/30/2006	Semiconductor Integrated Circuit Having Low Power Consumption With Self-Refresh
PCT/CA2007/000499	WO	3/28/2007	Dynamic Random Access Memory With Fully Independent Partial Array Refresh Function
PCT/CA2007/000891	WO	5/18/2007	Apparatus And Method For Establishing Device Identifiers For Serially Interconnected Devices
PCT/CA2007/001167	WO	6/29/2007	Method Of Configuring Non-Volatile Memory For A Hybrid Disk Drive
PCT/CA2007/001428	WO	8/20/2007	Modular Command Structure For Memory And Memory System
PCT/CA2007/001469	WO	8/22/2007	Scalable Memory System
PCT/CA2007/001661	WO	9/18/2007	Packet Based Id Generation For Serially Interconnected Devices
PCT/CA2007/002092	WO	11/20/2007	Apparatus And Method For Processing Data In Serial Interconnection Configuration Of Memory Devices
PCT/CA2007/002147	WO	11/29/2007	Apparatus And Method For Producing Device Identifiers For Serially Interconnected Devices Of Mixed Type
PCT/CA2007/002167	WO	12/3/2007	ID Generation Apparatus And Method For Serially Interconnected Devices
PCT/CA2007/002171	WO	12/4/2007	Apparatus And Method For Producing Device Identifiers For Serially Interconnected Devices Of Mixed Type
PCT/CA2007/002173	WO	12/4/2007	Address Assignment And Type Recognition Of Serially Interconnected Memory Devices Of Mixed Type
PCT/CA2007/002182	WO	12/4/2007	System And Method Of Operating Memory Devices Of Mixed Typed
PCT/CA2007/002183	WO	12/4/2007	Apparatus And Method For Capturing Serial Input Data
PCT/CA2007/002193	WO	12/4/2007	Apparatus And Method For Producing Identifiers Regardless Of Mixed Device Type In A Serial Interconnection

PCT/CA2007/002222	WO	12/10/2007	Memory System And Method With Serial And Parallel Modes
PCT/CA2007/002320	WO	12/21/2007	Independent Link And Bank Selection
PCT/CA2008/000120	WO	1/23/2008	Semiconductor Device And Method For Reducing Power Consumption In A System Having Interconnected Devices
PCT/CA2008/000237	WO	2/5/2008	Methods And Apparatus For Clock Synchronization In A Configuration Of Series-Connected Semiconductor Devices
PCT/CA2008/000250	WO	2/12/2008	Apparatus And Method For Using A Page Buffer Of A Memory Device As A Temporary Cache
PCT/CA2008/000273	WO	2/13/2008	Apparatus And Method Of Page Program Operation For Memory Devices With Mirror Back-Up Of Data
PCT/CA2008/000287	WO	2/15/2008	System And Method Of Page Buffer Operation For Memory Devices
PCT/US2008/054307	WO	2/19/2008	System Having One Or More Memory Devices