PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Mr. Hong-Boem Pyeon	06/23/2008

RECEIVING PARTY DATA

Name:	MOSAID Technologies Incorporated
Street Address:	11 Hines Road
City:	Kanata, Ontario
State/Country:	CANADA
Postal Code:	K2K 2X1

PROPERTY NUMBERS Total: 3

Property Type	Number
Application Number:	11942173
Application Number:	11966152
Application Number:	12018272

CH $120.00 11942173

CORRESPONDENCE DATA

Fax Number: (613)591-8148
Correspondence will be sent via US Mail when the fax attempt is unsuccessful.
Phone: 613-599-9539
Email: ipadmin@mosaid.com
Correspondent Name: Victoria Donnelly
Address Line 1: 11 HInes Road
Address Line 4: Kanata, Ontario, CANADA K2K 2X1

ATTORNEY DOCKET NUMBER:	1247-02 1260-02 1239-03US
NAME OF SUBMITTER:	Victoria Donnelly

Total Attachments: 8
source=Confirmatory Assignment Hong-Beom Pyeon#page1.tif
source=Confirmatory Assignment Hong-Beom Pyeon#page2.tif

source=Confirmatory Assignment Hong-Beom Pyeon#page3.tif
source=Confirmatory Assignment Hong-Beom Pyeon#page4.tif
source=Confirmatory Assignment Hong-Beom Pyeon#page5.tif
source=Confirmatory Assignment Hong-Beom Pyeon#page6.tif
source=Confirmatory Assignment Hong-Beom Pyeon#page7.tif
source=Confirmatory Assignment Hong-Beom Pyeon#page8.tif

CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS

For and in consideration of agreement(s) duly entered into with my employer, MOSAID Technologies Incorporated ("Assignee"), an Ontario corporation, and/or other good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, on this 23rd day of June, 2008, Hong-Boem Pyeon, ("Assignor"), hereby confirms, selling, assigning, and transferring to Assignee, the full extent of all right, title, and interest in and to any and all of the following (collectively, the "Rights"):

1. The provisional patent applications, patent applications and/or patents listed in the attached Exhibit 'A' (the "Patents");

2. All inventions claimed or described in any or all of the Patents (collectively, the "Inventions");

3. All rights with respect to the Inventions, including all U.S. patents or other governmental grants or issuances that may be granted with respect to the Inventions or from any direct or indirect divisionals, continuations, continuations-in-part, or other patent applications claiming priority rights from the Patents ("Potential Patents");

4. All reissues, reexaminations, extensions, or registrations of the Patents or Potential Patents;

5. All non-United States patents, patent applications, and counterparts relating to any or all of the Inventions, the Patents, or Potential Patents, including, without limitation, certificates of invention, utility models, industrial design protection, design patent protection, and other governmental grants or issuances ("Foreign Rights"), and including the right to file foreign applications directly in the name of Assignee, its successors and assigns;

6. The right to claim priority rights deriving from the Patents;

7. All causes of action and remedies related to any or all of the Patents, the Inventions, Potential Patents, or Foreign Rights (including, without limitation, the right to sue for past, present, or future infringement, misappropriation or violation of rights related to any of the foregoing and the right to collect royalties and other payments under or on account of any of the foregoing); and

8. Any and all other rights and interests arising out of, in connection with, or in relation to the Patents, the Inventions, Potential Patents, or Foreign Rights.

9. Assignor will not sign any writing or do any act conflicting with this Assignment, and, will sign all documents and do such additional acts as Assignee, their successors, legal representatives, and assigns deem necessary or desirable to perfect enjoyment of the Rights, conduct proceedings regarding the Rights (including any litigation or interference proceedings), or perfect or defend title to the Rights. Assignee shall compensate Assignor for any reasonable, documented disbursements provided that Assignor shall have furnished Assignee an advance, written estimate of the fees and costs for such assistance and Assignee shall have agreed in writing to pay such fees and costs. Assignor requests the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention,

utility models, or other governmental grants or issuances that may be granted upon any of the Rights in the name of the Assignee, as the assignee to the entire interest therein.

10. Assignor authorizes the firm, where applicable, MOSAID Technologies Incorporated and its agents to insert any further identification necessary to make this assignment suitable for recordation in the Patent Offices of any country as may be required.

11. The terms and conditions of this Assignment will inure to the benefit of Assignee, its successors, legal representatives, and assigns and will be binding upon Assignor, his successors, legal representatives and assigns.

By: _____
Hong-Boem Pyeon
Mosaid Technologies Incorporated

ATTESTATION

The undersigned witnessed the signature of Hong-Boem Pyeon to this document and makes the following statements:

1. Hong-Boem Pyeon is personally known to me (or proved to me on the basis of satisfactory evidence) and appeared before me on June 24, 2008, to execute this document.

2. Hong-Boem Pyeon subscribed to this document.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

By: _____
Print Name: Roland Schuetz

Exhibit 'A'

Serial #	Country ID	Filed Date	Title
2,627,663	CA	9/29/2006	Daisy Chain Cascading Devices
PCT/CA2006/001606	CA	9/29/2006	Multiple Independent Serial Link Memory
2.0068E+11	CN	9/29/2006	Multiple Independent Serial Link Memory
200680036482.X	CN	9/29/2006	Daisy Chain Cascading Devices
PCT/CA2006/001364	CN	8/18/2006	Power Up Circuit With Low Power Sleep Mode Operation
6775132.1	EP	8/18/2006	Power Up Circuit With Low Power Sleep Mode Operation
6790773.3	EP	9/29/2006	Memory With Output Control
8006223.5	EP	9/29/2006	Daisy Chain Cascading Devices
8006224.3	EP	9/29/2006	Daisy Chain Cascading Devices
8006225	EP	9/29/2006	Daisy Chain Cascading Devices
6761198.8	EP	7/31/2006	Voltage Down Converter For High Speed Memory
6790770.9	EP	9/29/2006	Multiple Independent Serial Link Memory
6790771.7	EP	9/29/2006	Daisy Chain Cascading Devices
751/MUMNP/2008	IN	9/29/2006	Daisy Chain Cascading Devices
PCT/CA2006/001606	IN	9/29/2006	Multiple Independent Serial Link Memory
PCT/CA2006/001252	JP	7/31/2006	Voltage Down Converter For High Speed Memory
PCT/CA2006/001364	JP	8/18/2006	Power Up Circuit With Low Power Sleep Mode Operation
PCT/CA2006/001606	JP	9/29/2006	Multiple Independent Serial Link Memory
PCT/CA2006/001607	JP	9/29/2006	Daisy Chain Cascading Devices
PCT/CA2006/001609	JP	9/29/2006	Memory With Output Control
10-2008-7009811	KR	8/18/2006	Power Up Circuit With Low Power Sleep Mode Operation
10-2008-7010546	KR	9/29/2006	Multiple Independent Serial Link Memory
10-2008-7010548	KR	9/29/2006	Daisy Chain Cascading Devices
10-2008-7010560	KR	9/29/2006	Memory With Output Control
10-2008-7005295	KR	7/31/2006	Voltage Down Converter For High Speed Memory
95128339	TW	8/2/2006	Voltage Down Converter For High Speed Memory
95136434	TW	9/29/2006	Daisy Chain Cascading Devices
95136449	TW	9/29/2006	Multiple Independent Serial Link Memory
96118202	TW	5/22/2007	Apparatus And Method For Establishing Device Identifiers For Serially Interconnected Devices
96125723	TW	7/13/2007	Pulse Counter With Clock Edge Recover
96130974	TW	8/21/2007	Modular Command Structure For Memory And Memory System
96131131	TW	8/22/2007	Scalable Memory System
96134886	TW	9/18/2007	Packet Based Id Generation For Serially Interconnected Devices

	TW	11/29/2007	Circuit And Method For Testing Multi-Device Systems
	TW	12/3/2007	Apparatus And Method For Producing Device Identifiers For Serially Interconnected Devices Of Mixed Type
	TW	12/5/2007	Apparatus And Method For Producing Device Identifiers For Serially Interconnected Devices Of Mixed Type
	TW	12/5/2007	Apparatus And Method For Producing Identifiers Regardless Of Mixed Device Type In A Serial Interconnection
	TW	12/6/2007	Address Assignment And Type Recognition Of Serially Interconnected Memory Devices Of Mixed Type
	TW	12/6/2007	System And Method Of Operating Memory Devices Of Mixed Typed
	TW	12/6/2007	Apparatus And Method For Capturing Serial Input Data
	TW	12/11/2007	Memory System And Method With Serial And Parallel Modes
	TW	12/19/2007	ID Generation Apparatus And Method For Serially Interconnected Devices
	TW	12/21/2007	Independent Link And Bank Selection
	TW	1/28/2008	Semiconductor Device And Method For Reducing Power Consumption In A System Having Interconnected Devices
	TW	2/13/2008	Semiconductor Device And Method For Selection And De-Selection Of Memory Devices Interconnected In Series
	TW	2/15/2008	Apparatus And Method For Using A Page Buffer Of A Memory Device As A Temporary Cache
	TW	2/15/2008	Apparatus And Method Of Page Program Operation For Memory Devices With Mirror Back-Up Of Data
	TW TW	2/18/2008	System Having One Or More Memory Devices
	TW	2/21/2008	System And Method Of Page Buffer Operation For Memory Devices
N/A		11/21/2007	Apparatus And Method For Processing Data In Serial Interconnection Configuration Of Memory Devices
	TW TW	5/1/2008	Mlc (Multi-Level Cell) Page Buffer With Dual Functions
N/A		2/19/2008	Decoding Control With Address Transition Detection In Page Erase Function
	TW	8/21/2006	Power Up Circuit With Low Power Sleep Mode Operation
95136448	TW	9/29/2006	Memory With Output Control

6 2 9 6 1 2 7 9 1 07 87	TW	2/13/2007	Dynamic Random Access Memory Device And Method For Self-Refreshing Memory Cells With Temperature Compensated Self-Refresh
6 107 3	TW	3/2/2007	Asynchronous Id Generation
9 6 4	TW	3/2/2007	Daisy Chain Cascade Configuration Recognition Technique
23 5 11 9 8 0	TW	6/29/2007	Method Of Configuring Non-Volatile Memory For A Hybrid Disk Drive
4 2 1 6	US	8/3/2005	Voltage Down Converter For High Speed Memory
11 5 55	US	4/28/2006	Dynamic Random Access Memory Device And Method For Self-Refreshing Memory Cells With Temperature Compensated Self-Refresh
11 6 56	US	12/6/2006	Apparatus And Method For Capturing Serial Input Data
1 13 8 2 8	US	12/20/2006	ID Generation Apparatus And Method For Serially Interconnected Devices
1 624 9 2	US	1/12/2007	Apparatus And Method For Producing Ids For Interconnected Devices Of Mixed Type
637 5	US	1/19/2007	Apparatus And Method For Producing Device Identifiers For Serially Interconnected Devices Of Mixed Type
11 17 44	US	12/12/2006	Memory System And Method With Serial And Parallel Modes
692 6 11 452	US	3/28/2007	Apparatus And Method For Producing Identifiers Regardless Of Mixed Device Type In A Serial Interconnection
692 7 11 043	US	3/28/2007	Apparatus And Method For Producing Device Identifiers For Serially Interconnected Devices Of Mixed Type
11 771	US	2/27/2007	Decoding Control With Address Transition Detection In Page Erase Function
11 023 1 4 1 2	US	6/29/2007	Address Assignment And Type Recognition Of Serially Interconnected Memory Devices Of Mixed Type
771 1 1 81 1 5	US	6/29/2007	System And Method Of Operating Memory Devices Of Mixed Type
781 1 822 1 96 1 4	US	7/23/2007	Voltage Down Converter For High Speed Memory
855 1 96 1 4	US	7/6/2007	System And Method Of Page Buffer Operation For Memory Devices
1/942 1 173	US	9/14/2007	Dynamic Random Access Memory And Boosted Voltage Producer Therefor
11/966,152	US	11/19/2007	Apparatus And Method For Processing Data In Serial Interconnection Configuration Of Memory Devices
	US	12/28/2007	Mlc (Multi-Level Cell) Page Buffer With Dual Functions

01 2 25 28 8 12/ 83 5	US	1 2 2008 4/2 008	Semiconductor Device And Method For Reducing Power Consumption In A System Having Interconnected Devices
/0 '3 9 12 02, 34	US	2 / 2 5/2 008	Apparatus And Method For Identifying Device Types Of Series-Connected Devices Of Mixed Type
1 / 2 66 6 12 0 0' 35	US	/ / 2 6/2 008	Semiconductor Device And Method For Selection And De-Selection Of Memory Devices Interconnected In Series
2 2 62 5		8/2	Nonvolatile Semiconductor Memory
12/ 0 3' 7	US	2 008 0	Data Channel Test Apparatus And Method Thereof
3 7 5 1 / 4 , 8 0	US	2 12 2 2/ 13 20 0 8	Apparatus And Method For Using A Page Buffer Of A Memory Device As A Temporary Cache
2 12/ 35 1 0 ,784	US	/ / 2/ 20 8	Apparatus And Method Of Page Program Operation For Memory Devices With Mirror Back-Up Of Data
12/ 39 ,79	US	19 0	System Having One Or More Memory Devices
1 6 6 62/9 3	US	2/21 2008 / 0	Serial Data Flow Control In Multiple Independent Serial Port
1 1 ,784 8 7		1 6 2 8 3 0 2 /2 7	Power Supplies In Flash Memory Devices And Systems
6/0 5 1 1 ,345 3	US	1/ / 12 4 0	Input/Output Buffer Path Test Circuit And Method Thereof
6 /0 15'	US	1 2 7 12/ /2 07	Memory Controller With Flexible Data Alignment To Clock
1 909 6 /0 9	US	20 0	Method For Stacking Serially-Connected Integrated Circuits And Multi-Chip Device Made From Same
1 01 ;907	U	/2 /20 12 1 07 /	Hierarchical Csl (Common Source Line) Structure In Nand Flash Memory
6 /2 1/01 2 ;92	US US	8 1/9 200 1/2 / 0 8	Timing And Clocking Method In A System Having A Plurality Of Devices
6 / 5 3 1/02 ,00	S US	3 2 0 3 2 0 8	Id (Identification) Number Based Sleep Mode Control In Serial Connected Memory
6 5 6 1/0 ,391	US	1/ 1/ 2 /4/2008	Power Supply Configuration For Nand Flash Memory
6 2 03	US	2 / 8 2 0	Selective-Broadcast Function For Serial-Connected Devices
1/03 ,6 1	US	2 0 8 3/2 / 0 8	Packaging Method For Serially Interconnected Memory Chips
6 9 05 11/238,973	US	6 2 0 9/30 2005	Memory Controller With Flexible Data Alignment To Clock
11/324,023	US		Power Up Circuit With Low Power Sleep Mode Operation
	US	12/30/2005	Multiple Independent Serial Link Memory
11/428,050	US	6/30/2006	Method Of Configuring Non-Volatile Memory For A Hybrid Disk Drive

11/495,609	US	7/31/2006	Pulse Counter With Clock Edge Recover
11/496,278	US	7/31/2006	Daisy Chain Cascading Device
11/521,734	US	9/15/2006	Asynchronous Id Generation
11/529,293	US	9/29/2006	Packet Based Id Generation For Serially Interconnected Devices
11/565,327	US	11/30/2006	Circuit And Method For Testing Multi-Device Systems
11/583,354	US	10/19/2006	Memory With Output Control
11/594,564	US	11/8/2006	Daisy Chain Cascading Devices
11/606,407	US	11/29/2006	Daisy Chain Cascade Configuration Recognition Technique
11/643,850	US	12/22/2006	Independent Link And Bank Selection
11/750,649	US	5/18/2007	Apparatus And Method For Establishing Device Identifiers For Serially Interconnected Devices
11/835,663	US	8/8/2007	Dynamic Random Access Memory Device And Method For Self-Refreshing Memory Cells With Temperature Compensated Self-Refresh
11/840,692	US	8/17/2007	Modular Command Structure For Memory And Memory System
11/843,440	US	8/22/2007	Scalable Memory System
PCT/CA2007/002092	WO	11/20/2007	Apparatus And Method For Processing Data In Serial Interconnection Configuration Of Memory Devices
PCT/CA2007/002147	WO	11/29/2007	Apparatus And Method For Producing Device Identifiers For Serially Interconnected Devices Of Mixed Type
PCT/CA2007/002148	WO	11/29/2007	Circuit And Method For Testing Multi-Device Systems
PCT/CA2007/002167	WO	12/3/2007	ID Generation Apparatus And Method For Serially Interconnected Devices
PCT/CA2007/002171	WO	12/4/2007	Apparatus And Method For Producing Device Identifiers For Serially Interconnected Devices Of Mixed Type
PCT/CA2007/002173	WO	12/4/2007	Address Assignment And Type Recognition Of Serially Interconnected Memory Devices Of Mixed Type
PCT/CA2007/002182	WO	12/4/2007	System And Method Of Operating Memory Devices Of Mixed Typed
PCT/CA2007/002183	WO	12/4/2007	Apparatus And Method For Capturing Serial Input Data
PCT/CA2007/002193	WO	12/4/2007	Apparatus And Method For Producing Identifiers Regardless Of Mixed Device Type In A Serial Interconnection
PCT/CA2007/002222	WO	12/10/2007	Memory System And Method With Serial And Parallel Modes
PCT/CA2007/002320	WO	12/21/2007	Independent Link And Bank Selection

			Semiconductor Device And Method For Reducing Power Consumption In A System Having Interconnected Devices
			Semiconductor Device And Method For Selection And De-Selection Of Memory Devices Interconnected In Series
			Apparatus And Method For Using A Page Buffer Of A Memory Device As A Temporary Cache
			Decoding Control With Address Transition Detection In Page Erase Function
			Apparatus And Method Of Page Program Operation For Memory Devices With Mirror Back-Up Of Data
			System And Method Of Page Buffer Operation For Memory Devices
			Multi-Level Cell Access Buffer With Dual Functions
			System Having One Or More Memory Devices
			Asynchronous Id Generation
			Daisy Chain Cascade Configuration Recognition Technique
			Dynamic Random Access Memory Device And Method For Self-Refreshing Memory Cells With Temperature Compensated Self-Refresh
			Apparatus And Method For Establishing Device Identifiers For Serially Interconnected Devices
			Method Of Configuring Non-Volatile Memory For A Hybrid Disk Drive
			Pulse Counter With Clock Edge Recover
			Modular Command Structure For Memory And Memory System
			Scalable Memory System
			Packet Based Id Generation For Serially Interconnected Devices