PATENT ASSIGNMENT

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Montalvo Systems, Inc.	04/17/2008

RECEIVING PARTY DATA

Name:	Sun Microsystems, Inc.
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PROPERTY NUMBERS Total: 96

Property Type	Number
Patent Number:	6542958
Patent Number:	6894534
Patent Number:	6348812
Patent Number:	6614258
Patent Number:	6433581
Patent Number:	6304102
Patent Number:	6502202
Patent Number:	6957323
Patent Number:	6848025
Application Number:	11781942
Application Number:	12030856
PCT Number:	US0852493
PCT Number:	US0852496
Application Number:	11277761
Application Number:	11277762

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Application Number:	11277763
Application Number:	11277764
Application Number:	11277765
Application Number:	11306000
Application Number:	11351059
Application Number:	11279880
Application Number:	11279882
Application Number:	11279883
Application Number:	11535971
Application Number:	11535972
Application Number:	11535977
Application Number:	11553453
Application Number:	11553455
Application Number:	11553458
Application Number:	11561270
Application Number:	11561274
Application Number:	11561281
Application Number:	11561284
Application Number:	11561287
Application Number:	11566206
Application Number:	11740892
Application Number:	11740901
Application Number:	11759216
Application Number:	11759217
Application Number:	11759218
Application Number:	11774581
Application Number:	11774583
Application Number:	11751949
Application Number:	11751973
Application Number:	11751985
Application Number:	11490778
Application Number:	11645901
Application Number:	11782140
Application Number:	11993199
Application Number:	60707070

Application Number:	60721385
Application Number:	60721817
Application Number:	60721818
Application Number:	60730550
Application Number:	60729558
Application Number:	60730810
Application Number:	60731784
Application Number:	60731785
Application Number:	60731962
Application Number:	60731967
Application Number:	60731968
Application Number:	60731969
Application Number:	60732438
Application Number:	60736632
Application Number:	60736736
Application Number:	60738225
Application Number:	60741724
Application Number:	60743560
Application Number:	60744010
Application Number:	60744592
Application Number:	60746049
Application Number:	60747200
Application Number:	60747818
Application Number:	60749962
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Application Number:	60757240
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Application Number:	60762817
Application Number:	60777015
Application Number:	60781772
Application Number:	60803367
Application Number:	60804085

Application Number:	60806786
Application Number:	60832822
Application Number:	60832823
Application Number:	60832848
Application Number:	60862609
Application Number:	60863125
Application Number:	60866203
Application Number:	60866205
Application Number:	60888006
Application Number:	60888011
Application Number:	60889547

CORRESPONDENCE DATA

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Total Attachments: 6
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ASSIGNMENT OF PATENT RIGHTS

This ASSIGNMENT OF PATENT RIGHTS, dated April 21, 2008 (this "**Agreement**"), is entered into by Montalvo Systems, Inc., a Delaware corporation ("**Assignor**"), for the benefit of Sun Microsystems, Inc., a Delaware corporation ("**Purchaser**"), and Sun Microsystems Technology Ltd., a company organized and existing under the laws of Bermuda and a wholly-owned subsidiary of Purchaser ("**Purchaser Sub**", and together with Purchaser, the "**Assignees**").

WHEREAS, Purchaser, Purchaser Sub, Assignor, Montalvo Computer Systems India Private Limited, a limited company organized under the laws of India, Montalvo Systems Cayman, Ltd., a company organized under the laws of the Cayman Islands, and U.S. Bank, National Association as Escrow Agent, have entered into that certain Asset Purchase Agreement dated as of April 9, 2008 (the "**Purchase Agreement**").

WHEREAS, Assignor has agreed to sell and assign, and the Assignees have agreed to buy and acquire all of Assignor's rights, title and interests in and to the letters patents and patent applications set forth in Attachment A attached hereto (the "**Assigned Patents and Patent Applications**").

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, Assignor hereby assigns and transfers to the Assignees any and all worldwide rights, title and interests Assignor holds, or may hold, in and to the Assigned Patents and Patent Applications, together with all rights derived therefrom, including but not limited to the right to sue for and collect damages for past, present and future infringement.

Assignor further agrees that, should additional or further documentation of the assignment be required for whatever reason, Assignor will, without further consideration, provide or execute such other information or documents as may be necessary upon the Assignees' reasonable request.

This Agreement shall be binding on and shall inure to the benefit of, the parties hereto and their respective successors and assigns. This Agreement will be governed by, and construed in accordance with, the internal laws of the State of California applicable to contracts executed and performed entirely therein, without regard to the principles of choice of law or conflicts or law of any jurisdiction. If any term or other provision of this Agreement is invalid, illegal or incapable of being enforced by any rule of law or public policy, all other conditions and provisions of this Agreement will nevertheless remain in full force and effect so long as the economic or legal substance of the transactions contemplated hereby is not affected in any manner materially adverse to any party. Upon such determination that any term or other provision is invalid, illegal or incapable of being enforced, the parties hereto will negotiate in good faith to modify this Agreement so as to effect the original intent of the parties as closely as possible in a mutually acceptable manner in order that the transactions contemplated hereby be consummated as originally contemplated to the greatest extent possible. This Agreement may be executed in one or more counterparts, and by the different parties hereto in separate counterparts, each of which when executed will be deemed to be an original but all of which taken together will constitute one and the same agreement.

[SIGNATURE PAGE FOLLOWS ON NEXT PAGE]

IN WITNESS WHEREOF, Assignor has caused this Assignment of Patent Rights to be executed by its duly authorized representatives effective as of the date first written above.

MONTALVO SYSTEMS, INC.

By: _____

Name: MATTHEW R. PERRY

Title: PRESIDENT & CEO

State of California

County of SANTA CLARA }

On 17 APRIL 2008 before me, WILLIAM F. BRONNER NOTARY PUBLIC

Date Here Insert Name and Title of the Officer

personally appeared MATTHEW R. PERRY

Name(s) of Signer(s)

who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is/~~are~~ subscribed to the within instrument and acknowledged to me that he/~~she/they~~ executed the same in his/~~her/their~~ authorized capacity(ies), and that by his/~~her/their~~ signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

Signature _____

Signature of Notary Public

WILLIAM F. BRONNER
COMM. # 1697638
NOTARY PUBLIC - CALIFORNIA
SANTA CLARA COUNTY
MY COMM. EXP. NOV. 1, 2010

Place Notary Seal Above

ATTACHMENT A

ASSIGNED PATENTS AND PATENT APPLICATIONS

Patents

Patent Number	Title	Country	Date Issued
6,542,958	Software Control of DRAM Refresh to Reduce Power Consumption In A Data Processing System	US	04/01/2003
182548	Software Control of DRAM Refresh To Reduce Power Consumption In A Data Processing System	Taiwan	11/21/2003
6,894,534	Dynamic Programmable Logic Array That Can Be Reprogrammed and A Method of Use	US	05/17/2005
6,348,812	Dynamic Programmable Logic Array That Can Be Reprogrammed and A Method of Use	US	02/19/2002
6,614,258	Field-Programmable Dynamic Logic Array	US	09/02/2003
6,433,581	Configurable Dynamic Programmable Logic Array	US	08/13/2002
171206	Configurable Dynamic Programmable Logic Array	Taiwan	05/29/2003
6,304,102	Repairable Dynamic Programmable Logic Array	US	10/16/2001
172035	Repairable Dynamic Programmable Logic Array	Taiwan	06/12/2003
6,502,202	Self-Adjusting Multi-Speed Pipeline	US	12/31/2002
6,957,323	Operand File Using Pointers and Reference Counters and a Method of Use	US	10/18/2005
6,848,025	Method and System for Programmable Replacement Mechanism for Caching Devices	US	01/25/2005

Patent Applications

Application Number	Application title	Utility filing date
11/781,937	Trace Unit with a Decoder, a Basic Block Builder, and a Multi-Block Builder	2007/07/23
11/781,942	Trace Unit with a Decoder, a Basic Block Cache, a Multi-Block Cache, and a Sequencer	2007/07/23
11/880,861	Trace Unit with a Trace Builder	2007/07/23
11/781,950	Trace Unit with a Decoder, a Basic Block Builder, and a Multi-Block Cache	2007/07/24
11/880,862	Trace Unit with a Decoder, a Basic Block Cache, a Multi-Block Cache, and Sequencer	2007/07/23
11/880,863	Trace Unit with an Op Path from a Decoder (bypass mode) and from a Basic-Block Builder	2007/07/23
11/880,864	Front End Processor Core Supporting Multiple Back End Execution Units Sharing a Basic Block Builder	2007/07/23
11/880,859	Concurrent vs. Low Power Branch Prediction	2007/07/23
11/880,875	Instruction Cache, Decoder Circuit, Basic Block Cache Circuit, and Multi-Block Cache Circuit	2007/07/23
11/880,882	Trace Unit	2007/07/23
11/923,638	Graceful Degradation in a Trace-Based Processor	2007/10/24
11/923,640	Abort Prioritization in a Trace-Based Processor	2007/10/24
11/941,900	Flag Optimization of a Trace	2007/11/16
11/941,908	Emit Vector Optimization of a Trace	2007/11/16
11/941,912	Symbolic Renaming Optimization of a Trace	2007/11/16
12/030,854	Memory Reconciliation Block	2008/02/13
12/030,851	Memory Ordering Queue / Versioning Cache Circuit	2008/02/13
12/030,846	Trace Based Deallocation of Entries in a Versioning Cache Circuit	2008/02/13
12/030,852	Trace Based Rollback of a Speculatively Updated Cache	2008/02/13
12/030,857	A Memory Ordering Queue Tightly Coupled with a Versioning Cache Circuit	2008/02/13
12/030,856	Delayed Store Buffer Entries Tagged with Trace IDs	2008/02/13
12/030,862	Checking for a Memory Ordering Violation after a Speculative Cache Write	2008/02/13
12/030,859	Rolling Back a Speculative Update of a Non-Modifiable Cache Line	2008/02/13
12/030,855	Versioning Cache Circuit Participating in a Cache Hierarchy	2008/02/13

12/030,865	A Trace-Based Store Operation Buffer	2008/02/13
12/030,858	Cache Rollback Acceleration via a Bank Based Versioning Cache Circuit	2008/02/13
11/543,598	Cache Operations With Hierarchy Control	2006/10/04
11/552,329	Timed Pause Instructions	2006/10/24
11/616,093	Timed Pause Instructions	2006/12/26
11/555,181	Selective Register File Disablement	2006/10/31
11/543,549	Cache Instructions with Hierarchy Control	2006/10/04
11/555,258	Synchronized register renaming in a multiprocessor	2006/10/31
11/555,263	Synchronized register renaming in a multiprocessor	2006/10/31
11/555,253	Dynamic Resource Allocation	2006/10/31
97103973	Memory Device With Split Power Switch and Related Methods	2008/02/01
11/932,555	Memory Device With Split Power Switch	2007/10/31
PCT/US08/52493	Memory Device With Split Power Switch and Related Methods	2008/01/30
11/932,643	Method of Selectively Powering Memory Device	2007/10/31
11/932,699	Memory Cell With Internal Power Switch	2007/10/31
11/932,738	Method of Operating Memory Cell Providing Internal Power Switching	2007/10/31
11/777,074	Memory Cells With Power Switch For Improved Low Voltage Operation	2007/07/12
11/745,370	Enhanced signaling sensitivity using multiple references	2007/05/07
11/932,311	Dynamic Voltage Scaling For Self-Timed or Racing Paths	2007/10/31
11/738,287	Dynamic Dual Output Latch	2007/04/20
11/737,103	NAND/NOR REGISTERS	2007/04/18
11/764,159	Symmetrical Differential Amplifier	2007/06/15
97103958	Elastic power for read and write margins	2008/02/01
11/932,967	Elastic power for read and write margins	2007/10/31
PCT/US08/52496	Elastic power for read and write margins	2008/01/30
11/938,196	Elastic Power for Read Margin	2007/11/09
11/277,761	Adaptive Computing Ensemble Microprocessor Architecture	2006/03/29
11/277,762	Microprocessor Architecture with Reconfigurable Function Units	2006/03/29
11/277,763	Statically Configured Microprocessor Architecture	2006/03/29
11/277,764	Configurable Multi-Core Processor Implementing Vitrual Processors	2006/03/29
11/277,765	Thread Migration and Reconfiguration of a Multi-Core Processor	2006/03/29
11/306,000	Software Hint to Specify the Preferred Branch Prediction to Use for a Branch Instruction	2005/12/16
11/351,059	Software Hint to Specify Preferred Load Value Prediction Mechanism	2006/02/09
11/279,880	Improved Prefetch Hardware Efficiency via Prefetch Hint Instructions	2006/04/15
11/279,882	Mechanisms for Software (OS) to Control Threads Between Multiple Cores	2006/04/15
11/279,883	Objective-Directed Mechanisms for Software (OS) to Control Thread Migration	2006/04/15
11/535,971	Efficient Trace Cache Management During Self-Modifying Code Processing	2006/09/27
11/535,972	Selective Trace Cache Invalidation for Self-Modifying Code Via Memory Aging	2006/09/27
11/535,977	Trace Cache for Efficient Self-Modifying Code Processing	2006/09/27
11/553,453	Checkpointing Flags During Atomic Trace Renaming	2006/10/26
11/553,455	Checkpointing Flags On Demand for Atomic Traces	2006/10/26
11/553,458	Flag Restoration from Checkpoints for Aborts of Atomic Traces	2006/10/26
11/561,270	Fusing Operations of a Target Architecture Operation Set	2006/11/17
11/561,274	Trace Optimization via Fusing Operations of a Target Operation Set	2006/11/17
11/561,281	Fusing Register Operations of a Target Architecture Operation Set	2006/11/17
11/561,284	Fusing Assert Operations of a Target Architecture Operation Set	2006/11/17
11/561,287	Executing Functions Determined via a Collection of Operations from Translated Instructions	2006/11/17
11/566,206	Microarchitecture for Compact Storage of Embedded Constants	2006/12/01
11/740,892	Reduced-Power Memory with Per-Sector Ground Control	2007/04/26
11/740,901	Reduced-Power Memory with Per-Sector Power/Ground Control and Early Address	2007/04/26
11/759,216	Software-Directed Rank Coalescing	2007/06/06
11/759,217	Physical Memory Allocating According to Ranks	2007/06/06
11/759,218	Associative Structure Rank Counters	2007/06/06
11/774,581	Executing Instruction Sequences According to Execution Mode	2007/07/07
11/774,583	Controlling Operation of a Processor According to Execution Mode of an Instruction Sequence	2007/07/07

11/751,949	Re-Fetching Cache Memory Enabling Low-Power Modes	2007/05/22
11/751,973	Re-Fetching Cache Memory Enabling Alternative Operational Modes	2007/05/22
11/751,985	Re-Fetching Cache Memory Having Coherrent Refetching	2007/05/22
11/490,778	Mechanism to Provide Software Access to Physical Memory in a Processing System	2006/07/21
11/408,784	Reducing Power Consumption for Processing of Common Values in Microprocessor Registers and Execution Units	2006/04/21
11/416,872	System and Method for Optimizing a Memory Controller	2006/05/02
11/435,528	System and Method for Processing Instructions in a Computer System	2006/05/17
11/450,103	System and Method for Conserving Power	2006/06/09
11/645,901	Prediction of Data Values Read from Memory by a Microprocessor Using a Dynamic Confidence Threshold	2006/12/26
11/781,949	A Method And System For Promoting Traces In An Instruction Processing Circuit	2007/07/24
11/782,163	Microprocessor with Coherent Caches for Basic Blocks and Traces	2007/07/24
11/591,024	Microprocessor with Coherent Caches for Instructions, Basic Blocks, and Traces	2006/10/31
11/782,140	Method and System for Promoting Traces in an Instruction Processing Circuit	2007/07/24
11/559,133	Power Conservation via DRAM Access Reduction	2006/11/13
11/559,192	Power Conservation via DRAM Access Reduction	2006/11/13
11/351,070	Power Conservation via DRAM Access Reduction	2006/02/09
PCT/US2006/044129	Power Conservation via DRAM Access Reduction	2006/11/14
95142014	Power Conservation via DRAM Access Reduction	2006/11/14
11/559,069	Small and Power-Efficient Cache that Can Provide Data for Background DMA Devices while the Processor Is in a Low-Power State	2006/11/13
11/351,058	Small and Power-Efficient Cache that Can Provide Data for Background DMA Devices while the Processor Is in a Low-Power State	2006/02/09
PCT/US2006/044095	Small and Power-Efficient Cache that Can Provide Data for Background DMA Devices while the Processor Is in a Low-Power State	2006/11/14
95142016	Small and Power-Efficient Cache that Can Provide Data for Background DMA Devices while the Processor Is in a Low-Power State	2006/11/14
11/645,935	Prediction of Data Values Read From Memory by a Microprocessor Using Selective Table Entry Replacement	2006/12/26
11/645,917	Low-Power Prediction of Data Values Read from Memory by a Microprocessor	2006/12/26
11/646,008	Prediction of Data Values Read from Memory by a Microprocessor Using the Storage Destination of a Load Operation	2006/12/26
11/963,579	Microprocessor Including a Display Interface in the Microprocessor (App 1 of 2)	2007/12/21
11/782,180	A Trace Verification System And Method For An Instruction Processing Circuit	2007/07/24
11/782,238	A Method And System For Utilizing a Common Structure For Trace Verification And Maintaining Coherency In An Instruction Processing Circuit	2007/07/24
11/963,603	Microprocessor Including a Display Interface in the Microprocessor (App 2 of 2)	2007/12/21
11/933,199	Virtual Core Management (App 2)	2007/10/31
11/933,267	Virtual Core Management (App 3)	2007/10/31
11/933,297	Virtual Core Management (App 4)	2007/10/31
11/933,319	Virtual Core Management (App 5)	2007/10/31
11/933,333	Virtual Core Management (App 6)	2007/10/31
11/933,349	Virtual Core Management (App 7)	2007/10/31
11/781,726	Virtual Core Management (App 1)	2007/07/23
11/941,895	Processor with Basic Block and Multi-Block Trace Caches	2007/11/16
11/941,883	A Method and System for Promoting Traces in an Instruction Processing Circuit	2007/11/16
60/707070	Adaptive Computing Ensemble Microprocessor Architecture	2005/08/10
60/721385	Efficient Trace Cache Management During Self-Modifying Code Processing	2005/09/28
60/721817	Software Hint to Specify Preferred Load Value Prediction Mechanism	2005/09/29
60/721818	Software Hint to Specify the Preferred Branch Prediction to Use for a Branch Instruction	2005/09/29
60/730550	Checkpointing Status Flags for Atomic Traces	2005/10/26

60/729558	A Timed Pause Instruction for More Power Efficient Handling of Microdelays in Software	2005/10/24
60/730810	Allocation and Deallocation of Shadow Registers used by Atomic Traces	2005/10/27
60/731784	Extend Cache Operations to Provide Control over which levels of the Hierarchy they Apply To	2005/10/31
60/731785	Maintaining Memory Coherency within a Trace Cache	2005/10/31
60/731962	Determining the Highest Priority Abort Trigger in an Atomic Trace	2005/10/31
60/731967	Synchronized Register Renaming by a Master Processor and a Coprocessor	2005/10/31
60/731968	Enhanced RF Detector Saves Power During Unnecessary Reads	2005/10/31
60/731969	Instructions Giving Hints to the Hardware Prefetcher for More Efficient Prediction of Prefetches	2005/10/31
60/732438	Zero-Cycle Execution of Clear Operation and Automatic Register Free	2005/11/01
60/736632	Power Conservation via DRAM Access Reduction	2005/11/14
60/736736	A Small and Power-Efficient Cache That Can Provide Data for Background DMA Devices While the Processor Is In A Low-Power State	2005/11/15
60/738225	Fusing of Register Operations, Merging, Status Flag Updates, Branches	2005/11/18
60/741724	A Microarchitecture For Compressed Storage of Operations with Embedded Constants	2005/12/02
60/743560	Improved Prefetch Hardware Efficiency via Prefetch Hint Instructions	2006/03/20
60/744010	Software-assisted Thread Migration Between Multiple Cores	2006/03/30
60/744592	Improved Prefetch Hardware Efficiency Via Prefetch Hint Instructions	2006/04/10
60/746049	Reduced-Power Memory with Per-Sector Power/Ground Control and Early Address	2006/04/30
60/747200	Reduced Power Cache Memory with Per-Sector Power Control	2006/05/14
60/747818	Re-Fetching Cache Memory	2006/05/22
60/749962	Software Hint to Specify the Preferred Branch Prediction To Use for a Branch Instruction	2005/12/12
60/751398	Adaptive Computing Ensemble Microprocessor Architecture	2005/12/17
60/757240	Extended Resource Credit Scheme to Support Dynamic Reassignment of Resources Among Data Producers	2006/01/09
60/758485	Microprocessor Architecture with Reconfigurable Function Units	2006/01/10
60/759484	Microprocessor Architecture with Reconfigurable Function Units	2006/01/17
60/761220	Power Conservation Via DRAM Access Reduction	2006/01/23
60/761925	A Small and Power-Efficient Cache That Can Provide Data For Background DMA Devices While the Processor is in a Low-Power State	2006/01/25
60/762817	Software Hint To Specify Preferred Load Value Prediction Mechanism	2006/01/27
60/777015	Statically Configured Microprocessor Architecture	2006/02/25
60/781772	Software-Assisted Thread Migration Between Multiple Cores	2006/03/13
60/803367	Re-Fetching Cache Memory	2006/05/28
60/804085	Application-Directed Rank Coalescing for Memory Power Management	2006/06/06
60/806786	Execution Modes Applied to Instruction Sequences	2006/07/09
60/832822	Microprocessor with Coherent Caches for Basic Blocks and Traces	2006/07/23
60/832823	Managing Multiple Physical Core Processors to Behave As One Virtual Core Processor	2006/07/23
60/832848	Microprocessor with Caches for Instructions, Basic Blocks, and Traces	2006/07/23
60/862609	Exception Handling for Atomic Traces	2006/10/24
60/863125	Method for Early Deallocation of Physical Registers When Shadow Registers Are Used	2006/10/26
60/866203	Processor with Basic Block and Multi-Block Trace Caches	2006/11/16
60/866205	Processor with Optimized Operation Sequences for Basic Block and Multi-Block Trace Caches	2006/11/16
60/888006	Split Power Switch for Memory Cells	2007/02/02
60/888011	Memory Cells with Power Switch for Write Operations	2007/02/02
60/889547	Instruction Sub-Type Tracking Unit	2007/02/13