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U.S. DEPARTMENT OF COMMERCE
United States Patent and Trademark Office

103535601

To the Director of the U.S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

1. Name of conveying party(ies)

Novias, LLC

Additional name(s) of conveying party(ies) attached? ☐ Yes ☑ No

2. Name and address of receiving party(ies)

Name: Interconnect Portfolio, LLC

Internal Address:

Street Address: 20400 Stevens Creek Blvd., Fifth Floor

City: Cupertino

State: CA

Country: USA Zip: 95023

Additional name(s) & address(es) attached? ☐ Yes ☑ No

3. Nature of conveyance/Execution Date(s):

Execution Date(s) March 14, 2008

☑ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☐ Joint Research Agreement
☐ Government Interest Assignment
☐ Executive Order 9424, Confirmatory License
☐ Other

4. Application or patent number(s): ☐ This document is being filed together with a new application.

A. Patent Application No.(s)

11/933,445 11/939,554 11/965,705
12/127,195 12/128,620 61/018,495

B. Patent No.(s)

7,404,746 7,192,320 7,227,759 7,278,855
7,310,239 7,347,697 7,404,746

Additional numbers attached? ☐ Yes ☑ No

5. Name and address to whom correspondence concerning document should be mailed:

Name: Interconnect Portfolio, LLC

Internal Address:

Street Address: 20400 Stevens Creek Blvd., Fifth Floor

City: Cupertino

State: CA Zip: 95023

Phone Number: (714) 650-0342

Fax Number:

Email Address: rshea@rshealaw.com

6. Total number of applications and patents involved: 13

7. Total fee (37 CFR 1.21(h) & 3.41) $ 520.00

☐ Authorized to be charged by credit card
☐ Authorized to be charged to deposit account
☑ Enclosed
☐ None required (government interest not affecting title)

8. Payment Information

a. Credit Card Last 4 Numbers
Expiration Date

b. Deposit Account Number 11/18/2008 MJAMAI 00000064 11933445
Authorized User Name 520.00 OP

9. Signature:

Signature

13 November 2008
Date

Ronalld R. Shea, Esq., Reg. No. 45,098
Name of Person Signing

Total number of pages including cover sheet, attachments, and documents: 6

Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to:
Mail Stop Assignment Recordation Services, Director of the USPTO, P.O.Box 1450, Alexandria, V.A. 22313-1450

EXHIBIT D

ASSIGNMENT

This Assignment ("Assignment") is entered into by and between Novias LLC, a California limited liability company, hereinafter sometimes ("Novias") on the one hand, and Interconnect Portfolio LLC ("IPL"), a Delaware limited liability company, hereinafter sometimes "IPL" on the other hand.

NOW THEREFORE, for and in consideration of the mutual covenants herein contained as well as of other good and valuable consideration the receipt and sufficiency of which is hereby acknowledged, and pursuant to that certain Master Agreement between Novias and IPL dated March 14, 2008 (the "Purchase Agreement"), it is covenanted and agreed by and between the parties hereto that:

1. Subject Matter

1.1 The patents and related materials described on the Interconnection Patent Schedule attached hereto as Schedule I as well as all inventions, improvements, developments, and discoveries that relate to Novias' high-speed copper interconnection technology conceived, discovered, or reduced to practice by Novias or its affiliates for the duration of Novias' entitlement to payments under the Purchase Agreement, all of which is hereinafter collectively referred to as the "Interconnection Technology".

1.2 Interconnection Technology shall also include all rights with respect to patent rights, copyrights, mask work rights, trade names, trademarks, trade secrets, know-how, and other intellectual property (and goodwill associated therewith) of whatsoever kind or nature and in whatever form which directly relate to the Interconnection Technology and in which Novias or its affiliates have an interest to the extent of such said interest, including specifically the rights and obligations of Novias arising under the License with IntellaSys BEC Ltd (the "BEC Product License").

2. Grant of Assignment

2.1 Novias hereby grants, sets-over, assigns, transfers, conveys, and acquits unto IPL all of the right, title, and interest of Novias of whatsoever kind or nature, now existing or hereafter arising, in and to the Interconnection Technology, subject to (i) those rights which enable and/or facilitate the use of the Interconnection Technology in connection with sales of products to customers outside the United States, which said rights have heretofore been licensed to IntellaSys BEC Ltd., and (ii) [description of implementation license], (together with the BEC Product License, the "Existing Licenses").

2.2 In conjunction with, as a part of, and subject to the limitations described in Sections 2.1 herein, Novias hereby grants, sets-over, assigns, transfers, conveys unto IPL the exclusive, worldwide right to:

2.2.1 Regulate and control by license, sublicense, affiliation, or other agreement the practice and/or use of the Interconnection Technology;

2.2.2 Otherwise pursue the commercialization thereof and the manufacture, sale, and use of products and/or services relaying on the Interconnection Technology;

2.2.3 Sue and collect for its own use and benefit all claims for damages by reason of past infringement or use of the Interconnection Technology; and,

2.2.4 Pursue all remedies of whatsoever kind or nature for its own use and benefit relating to the past, present, or future infringement or use of the Interconnection Technology.

2.3 Novias hereby grants, sets-over, assigns, transfers, conveys, and acquits unto IPL all of the right, title, and interest of Novias of whatsoever kind or nature, now existing or hereafter arising, in and to the Existing Licenses. All costs for the registration of the assignment of the patents and other transferred intellectual property rights will be borne by IPL.

4. Attachments

4.1 Schedule I: Schedule of Novias Patents

IN WITNESS WHEREOF, the parties have hereunto set their hands and seals as of March 14, 2008.

INTERCONNECT PORTFOLIO LLC

by: _____
Daniel E. Leckrone, Chmn

SKA

NOVIAS LLC

by: _____
Kevin Grundy, Manager

Schedule I

SCHEDULE OF Novias PATENTS

(see Interconnection Patent Schedule attached)

JUR	PAT NO	DESCRIPTION	PRIORITY	FILED	ISSUED	EXPIRES
US						
	6,809,608	Transmission Structure With An Air Dielectric			10/26/04	
	7,307,293	Direct-Connect Integrated Circuit Signaling System For Bypassing Intra-Substrate Printed Circuit Signal Paths			12/11/07	
	6,884,120	Array Connector With Deflectable Coupling Structure For Mating With Other Components			04/26/05	
	6,891,272	Multi-Path Via Interconnection Structures And Methods For Manufacturing The Same			05/10/05	
	7,014,472	System For Making High-Speed Connections To Board-Mounted Modules			03/21/06	
	7,308,524	Memory Chain			12/11/07	
	7,111,108	Memory System Having A Multiplexed High-Speed Channel			09/18/06	
	7,061,096	Multi-Surface IC Packaging Structures And Methods For Their Manufacture			06/13/06	
	6,933,610	Method Of Bonding A Semiconductor Die Without An Esd Circuit And A Separate Esd Circuit To An External Lead, And A Semiconductor Device Made Thereby			08/23/05	
	7,176,580	Structures And Methods For Wire Bonding Over Active, Brittle And Low K Dielectric Areas Of An IC Chip			02/13/07	
	7,279,783	Partitioned Integrated Circuit Package with Central Clock Driver			10/09/07	
	7,280,372	Stair Step Printed Circuit Board Structures For High Speed Signal Transmissions			10/09/07	
	7,205,613	Insulating Substrate For IC Packages Having Integral ESD Protection			04/17/07	
	7,278,855	High Speed, Direct Path Stair-Step, Electronic Connectors With Improved Signal Integrity Characteristics And Methods For Their Manufacture			10/09/07	
	7,310,239	IC Packaging Interposer Having Controlled Impedence for Optical Interconections and an integral Heat Spreader			12/18/07	

JUR	PAT NO	DESCRIPTION	PRIORITY	FILED	ISSUED	EXPIRES
	7,192,320	Electrical Interconnection Devices Incorporating Redundant Contact Points For Reducing Capacitive Stubs And Improved Signal Integrity			03/20/07	
	7,227,759	Signal Segregating Connector System			06/05/07	
	7,307,293	Direct Connect Integrated Circuit Signaling System For Bypassing Intra-Substrate Printed Circuit Signal Paths			11/12/2007	
	11/092,034	Active Connector			TBD	
	10/426,930	Direct Connect Integrated Circuit Signaling System For Bypassing Intra-Substrate Printed Circuit Signal Paths				
	11/930,217	Direct Connect Integrated Circuit Signaling System For Bypassing Intra-Substrate Printed Circuit Signal Paths	Divisional			
	10/659,210	Cable Signaling System and Components Thereof				
	11/930,217	Cable Signaling System and Components Thereof	Divisonal			
	10/757,000	Memory Chain				
	11/933,445	Memory Chain	Divisional			
	10/857,830	Low Profile Discrete Electronic Components And Applications Of Same				
	11/353,564	Multi-Surface IC Packaging Structures And Methods For Their Manufacture	Dvisional			
	10/964,578	Multi-Surface Contact IC Packaging Structures And Assemblies				
	11/868,963	Partitioned Integrated Circuit Package With Central Clock Driver	Divisional			
	10/987,187	Tapered Dielectric And Conductor Structures And Applications Thereof				
	11/868,947	High Speed, Direct Path Stair-Step, Electronic Connectors With Improved Signal Integrity Characteristics And Methods For Their Manufacture	Divisional			
	11/055,578	Interconnect System Without Through-Holes				
	11/607,143	Electrical Interconnection Devices Incorporating Redundant Contact Points For Reducing Capacitive Stubs And Improved Signal Integrity				
	11/748,045	Signal Segregating Connector System				
	11/123,863	Torsionally-Induced Contact-Force Conductors For Electrical Connector Systems				
	11/182,484	IC Package Structures Having Separate Circuit Interconnection Structures And Asssemblies				

JUR	PAT NO	DESCRIPTION	PRIORITY	FILED	ISSUED	EXPIRES
		Constructed Thereof				
	11/381,357	Memory Packages Having Stair Step Interconnection Structures				
	11/200,501	Torsionally-Induced Contact-Force Conductors for Electronic Connectors II				
	60877691	Memory IC Package Assembly Having Stair Step Metal Layer and Aperture	Provisional			
	60920845	Memory IC Package Assembly Having Stair Step Metal Layer and Aperture	Provisional			
EU		Direct Connect Signaling System (Filed: Europe; Japan; China)				
EU		European Pat. App 03/1998/.4D.				
CHI		Chinese Patent App. No. 03813758.5				
JP		Japan -- Still active no number available yet				
		Multi-Surface IC Packaging Structures And Methods For Their Manufacture				
EU		European Pat App 04788995.1				

This Schedule of Patents shall be deemed to include the items listed above, as well as all progenitors, progeny and enhancements thereof, and all additions, changes, amendments, modifications, actions, counterparts, continuations, continuations-in-part, extensions, reissues, divisionals and/or renewals of such progenitors, progeny and enhancements.