PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY AGREEMENT

CONVEYING PARTY DATA

Name	Execution Date
Endicott Interconnect Technologies, Inc.	09/30/2008

RECEIVING PARTY DATA

Name:	JPMorgan Chase Bank, N.A., as Administrative Agent
Street Address:	10 South Dearborn Street
City:	Chicago
State/Country:	ILLINOIS
Postal Code:	60603

PROPERTY NUMBERS Total: 128

Property Type	Number
Application Number:	12081051
Application Number:	12081042
Application Number:	11882473
Application Number:	11652633
Application Number:	11797236
Application Number:	11650520
Application Number:	12010335
Application Number:	12010469
Application Number:	12010004
Application Number:	11598647
Application Number:	12007178
Application Number:	12003299
Application Number:	11590888
Application Number:	11806685
Application Number:	11541776

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Application Number:	11976629
Application Number:	11500328
Application Number:	11492029
Application Number:	11905188
Application Number:	11902976
Application Number:	11896786
Application Number:	11454896
Application Number:	11889668
Application Number:	11438424
Application Number:	11822573
Application Number:	11396711
Application Number:	11802434
Application Number:	11797232
Application Number:	11730761
Application Number:	11305073
Application Number:	11253659
Application Number:	11634287
Application Number:	11607973
Application Number:	11352279
Application Number:	11352276
Application Number:	11244180
Application Number:	11482945
Application Number:	11455183
Application Number:	11110920
Application Number:	11401401
Application Number:	11086324
Application Number:	11429990
Application Number:	11390386
Application Number:	11215206
Application Number:	11324273
Application Number:	11031085
Application Number:	11350777
Application Number:	11334445
Application Number:	11265287
Application Number:	10860067

Application Number:	11086323
Application Number:	10740500
Application Number:	10449019
Application Number:	10868066
Patent Number:	7416996
Patent Number:	7416972
Patent Number:	7384856
Patent Number:	7383629
Patent Number:	7381587
Patent Number:	7377033
Patent Number:	7348677
Patent Number:	7343674
Patent Number:	7342183
Patent Number:	7334323
Patent Number:	7332818
Patent Number:	7332212
Patent Number:	7328502
Patent Number:	7326643
Patent Number:	7307022
Patent Number:	7294791
Patent Number:	7293355
Patent Number:	7292055
Patent Number:	7270845
Patent Number:	7253518
Patent Number:	7253502
Patent Number:	7235745
Patent Number:	7211470
Patent Number:	7211289
Patent Number:	7209368
Patent Number:	7176383
Patent Number:	7169313
Patent Number:	7163847
Patent Number:	7161810
Patent Number:	7157647
Patent Number:	7157646

Patent Number:	7152319
Patent Number:	7145221
Patent Number:	7142121
Patent Number:	7129732
Patent Number:	7109732
Patent Number:	7091066
Patent Number:	7087846
Patent Number:	7087441
Patent Number:	7084014
Patent Number:	7078816
Patent Number:	7071423
Patent Number:	7063762
Patent Number:	7047630
Patent Number:	7045897
Patent Number:	7035113
Patent Number:	7025607
Patent Number:	7023707
Patent Number:	7013563
Patent Number:	6995322
Patent Number:	6992896
Patent Number:	6964884
Patent Number:	6958106
Patent Number:	6905589
Patent Number:	6900392
Patent Number:	6872894
Patent Number:	6828514
Patent Number:	6815837
Patent Number:	6809269
Application Number:	11907006
Application Number:	11907004
Application Number:	11976468
Application Number:	12007820
Application Number:	12148271
Application Number:	11730212
Application Number:	11727314

Application Number:	11882149
Application Number:	11783306
Application Number:	11808140
Application Number:	11730404
Application Number:	11878673
Application Number:	12007704
Application Number:	12078206
Application Number:	12215079

CORRESPONDENCE DATA

Fax Number: (214)981-3400

Correspondence will be sent via US Mail when the fax attempt is unsuccessful.

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Address Line 4: Dallas, TEXAS 75201

ATTORNEY DOCKET NUMBER:	36084-36710
NAME OF SUBMITTER:	Dusan Clark

Total Attachments: 16

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CONFIRMATORY GRANT OF SECURITY INTEREST IN UNITED STATES PATENTS

THIS CONFIRMATORY GRANT OF SECURITY INTEREST IN UNITED STATES PATENTS (as the same may be amended, restated, supplemented or otherwise modified from time to time, the "Confirmatory Grant") is made effective as of September 30, 2008 by and from ENDICOTT INTERCONNECT TECHNOLOGIES, INC., a New York corporation (the "Grantor"), to and in favor of JPMORGAN CHASE BANK, N.A., for itself and as Administrative Agent for the Lenders (as defined in the Credit Agreement referenced below) (in such capacities, the "Grantee").

WHEREAS, Grantor, the Lenders and Grantee have entered into a Credit Agreement dated as of September 30, 2008 (as may be amended, restated, supplemented or otherwise modified from time to time, the "Credit Agreement").

WHEREAS, the Grantor has entered into a Pledge and Security Agreement dated as of September 30, 2008 (as may be amended, restated, supplemented or otherwise modified from time to time, the "Security Agreement").

WHEREAS, the Grantor owns the patents listed on Exhibit A attached hereto (the "Patents"), which Patents are registered or pending with the United States Patent and Trademark Office.

WHEREAS, this Confirmatory Grant has been granted in conjunction with the security interest granted under the Security Agreement to Grantee for the benefit of the Holders of Secured Obligations. The rights and remedies of Grantee with respect to the security interest granted herein are without prejudice to and are in addition to those set forth in the Security Agreement and the other Loan Documents, all terms and provisions of which are incorporated herein by reference. In the event that any provisions of this Confirmatory Grant are deemed to conflict with the Security Agreement, the provisions of the Security Agreement shall govern.

NOW, THEREFORE, in consideration of the mutual covenants and agreements set forth herein and for other good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, it is hereby agreed that:

1) Definitions. All capitalized terms not defined herein shall have the respective meaning given to them in the Credit Agreement.

2) The Security Interest.

(a) This Confirmatory Grant is made to secure the satisfactory performance and payment of (i) all the Secured Obligations and (ii) all of the obligations and liabilities of the Subsidiary Guarantors under the Guaranty. Upon the payment in full of all Secured Obligations (other than Unliquidated Obligations), Grantee shall promptly, upon such satisfaction, execute, acknowledge, and deliver to Grantor all reasonably requested instruments in writing releasing the security interest in the Patents acquired under the Security Agreement and this Confirmatory Grant.

(b) The Grantor hereby grants to Grantee a security interest in (1) all of Grantor's right, title and interest in and to the Patents now owned or from time to time after the date hereof owned or acquired by the Grantor, together with (2) all proceeds of the Patents, and (3) all causes of action arising prior to or after the date hereof for infringement of the Patents or unfair competition regarding the same.

3) Counterparts. This Confirmatory Grant may be executed in any number of counterparts and by different parties in separate counterparts, each of which when so executed shall be deemed to be an original and all of which taken together shall constitute one and the same agreement. Signature pages may be detached from multiple separate counterparts and attached to a single counterpart.

4) Governing Law. This Confirmatory Grant and the rights and obligations of the parties hereto shall be governed by, and construed and interpreted in accordance with, the law of the State of New York.

****

IN WITNESS WHEREOF, the Grantor has executed this Confirmatory Grant effective as of the date first written above.

ENDICOTT INTERCONNECT TECHNOLOGIES, INC., as Grantor

By: _____
Name: STEVEN P BURKE
Title: CFO

STATE OF New York)
Westchester COUNTY)

On September 29, 2008, before me, Jacqueline J Warner, Notary Public, personally appeared Steven P. Burke, personally known to me to be the person whose name is subscribed to the within instrument and acknowledged to me that he executed the same in his authorized capacity, and that by his signature on the instrument, the person, or the entity upon behalf of which the person acted, executed the instrument.

(SEAL)

_____
Notary Public, State of New York
My Commission Expires: 3/12/2011

JACQUELINE J. WARNER
Notary Public, State of New York
No. 02WA6056940
Residing in Westchester County
My Commission Expires 3/12/20 11

Signature Page for
Grant of Security Interest in United States Patents

Confirmatory Grant of Security Interest
in United States Patents
Exhibit A-Schedule of Patents

NO.	PATENT NO./ PUBLICATION NO./ SERIAL NO.	DATE ISSUED/ DATE FILED	TITLE:
1.	20080191354 12081051	8/14/2008 4/10/2008	CIRCUITIZED SUBSTRATE WITH P-ARAMID DIELECTRIC LAYERS AND METHOD OF MAKING SAME
2.	20080191353 12081042	8/14/2008 4/10/2008	MULTILAYERED CIRCUITIZED SUBSTRATE WITH P-ARAMID DIELECTRIC LAYERS AND METHOD OF MAKING SAME
3.	20080170670 11882473	7/17/2008 8/2/2007	METHOD OF INSPECTING ARTICLES USING IMAGING INSPECTION APPARATUS WITH DIRECTIONAL COOLING
4.	20080168651 11652633	7/17/2008 1/12/2007	METHOD OF PROVIDING A PRINTED CIRCUIT BOARD WITH AN EDGE CONNECTION PORTION AND/OR A PLURALITY OF CAVITIES THEREIN
5.	20080151515 11/797236	6/26/2008 5/2/2007	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH RESISTOR INCLUDING MATERIAL WITH METAL COMPONENT AND ELECTRICAL ASSEMBLY AND INFORMATION HANDLING SYSTEM UTILIZING SAID CIRCUITIZED SUBSTRATE
6.	20080164300 11650520	7/10/2008 1/8/2007	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH SOLDER BALLS HAVING ROUGHENED SURFACES, METHOD OF MAKING ELECTRICAL ASSEMBLY INCLUDING SAID CIRCUITIZED SUBSTRATE, AND METHOD OF MAKING MULTIPLE CIRCUITIZED SUBSTRATE ASSEMBLY
7.	20080142258 12010335	6/19/2008 1/24/2008	HIGH SPEED INTERPOSER
8.	20080120835 12010469	5/29/2008 1/25/2008	METHOD OF MAKING HIGH SPEED INTERPOSER
9.	20080117583 12010004	5/22/2008 1/18/2008	INFORMATION HANDLING SYSTEM UTILIZING

NO.	PATENT NO./ PUBLICATION NO./ SERIAL NO.	DATE ISSUED/ DATE FILED	TITLE:
			CIRCUITIZED SUBSTRATE WITH SPLIT CONDUCTIVE LAYER
10.	20080110016 11598647	5/15/2008 11/14/2006	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH SOLDER PASTE CONNECTIONS
11.	20080105457 12007178	5/8/2008 1/8/2008	CIRCUITIZED SUBSTRATE WITH SINTERED PASTE CONNECTIONS AND MULTILAYERED SUBSTRATE ASSEMBLY HAVING SAID SUBSTRATE AS PART THEREOF
12.	20080102562 12003299	5/1/2008 12/21/2007	METHOD OF MAKING MULTI-CHIP ELECTRONIC PACKAGE WITH REDUCED LINE SKEW
13.	20080098595 11590888	5/1/2008 11/1/2006	METHOD OF MAKING A CIRCUITIZED SUBSTRATE WITH ENHANCED CIRCUITRY AND ELECTRICAL ASSEMBLY UTILIZING SAID SUBSTRATE
14.	20080087459 11/806,685	4/17/2008 6/4/2007	CIRCUITIZED SUBSTRATE WITH INTERNAL RESISTOR, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE, AND ELECTRICAL ASSEMBLY UTILIZING SAID CIRCUITIZED SUBSTRATE
15.	20080078570 11541776	4/3/2008 10/3/2006	HALOGEN-FREE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION, METHOD OF MAKING SAME, MULTILAYERED SUBSTRATE STRUCTURE UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING
16.	20080054476 11976629	3/6/2008 10/26/2007	CIRCUITIZED SUBSTRATE WITH INCREASED ROUGHNESS CONDUCTIVE LAYER AS PART THEREOF
17.	20080038670 11500328	2/14/2008 8/8/2006	SOLDER MASK APPLICATION PROCESS
18.	20080026316	1/31/2008	PHOTORESIST

Confirmatory Grant of Security Interest
in United States Patents
Exhibit A-Schedule of Patents

NO.	PATENT NO./ PUBLICATION NO./ SERIAL NO.	DATE ISSUED/ DATE FILED	TITLE:
	11492029	7/25/2006	COMPOSITION WITH ANTIBACTERIAL AGENT
19.	20080022520 11905188	1/31/2008 9/28/2007	METHOD OF MAKING MULTI-LAYERED CIRCUITIZED SUBSTRATE ASSEMBLY
20.	20080020566 11902976	1/24/2008 9/27/2007	METHOD OF MAKING AN INTERPOSER
21.	20080003407 11896786	1/3/2008 9/6/2007	CIRCUITIZED SUBSTRATE WITH DIELECTRIC LAYER HAVING DIELECTRIC COMPOSITION NOT INCLUDING CONTINUOUS OR SEMICONTINUOUS FIBERS
22.	20070289773 11454896	12/20/2007 6/19/2006	HIGH SPEED INTERPOSER
23.	20070284140 11889668	12/13/2007 8/15/2007	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH IMPROVED IMPEDANCE CONTROL CIRCUITRY, ELECTRICAL ASSEMBLY AND INFORMATION HANDLING SYSTEM
24.	20070275525 11438424	11/29/2007 5/23/2006	CAPACITIVE SUBSTRATE AND METHOD OF MAKING SAME
25.	20070254408 11822573	11/1/2007 7/9/2007	METHOD OF MAKING WIREBOND ELECTRONIC PACKAGE WITH ENHANCED CHIP PAD DESIGN
26.	20070230130 11396711	10/4/2007 4/4/2006	ADJUSTABLE THICKNESS THERMAL INTERPOSER AND ELECTRONIC PACKAGE UTILIZING SAME
27.	20070221404 11802434	9/27/2007 5/23/2007	CIRCUITIZED SUBSTRATE AND CONDUCTIVE PASTE, ELECTRICAL ASSEMBLY INCLUDING SAID CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAID SUBSTRATE
28.	20070199195 11797232	8/30/2007 5/2/2007	METHOD FOR MAKING A MULTILAYERED CIRCUITIZED SUBSTRATE
29.	20070177331 11730761	8/2/2007 4/4/2007	NON-FLAKING CAPACITOR MATERIAL, CAPACITIVE SUBSTRATE HAVING AN

NO.	PATENT NO./ PUBLICATION NO./ SERIAL NO.	DATE ISSUED/ DATE FILED	TITLE:
			INTERNAL CAPACITOR THEREIN INCLUDING SAID NON-FLAKING CAPACITOR MATERIAL, AND METHOD OF MAKING A CAPACITOR MEMBER FOR USE IN A CAPACITIVE SUBSTRATE
30.	20070139977 11305073	6/21/2007 12/19/2005	METHOD OF IMPROVING ELECTRICAL CONNECTIONS IN CIRCUITIZED SUBSTRATES
31.	20070090170 11253659	4/26/2007 10/20/2005	METHOD OF MAKING A CIRCUITIZED SUBSTRATE HAVING A PLURALITY OF SOLDER CONNECTION SITES THEREON
32.	20070089290 11634287	4/26/2007 12/6/2006	METHOD OF MAKING A PRINTED CIRCUIT BOARD WITH LOW CROSS-TALK NOISE
33.	20070075726 11607973	4/5/2007 12/4/2006	INTERPOSER AND TEST ASSEMBLY FOR TESTING ELECTRONIC DEVICES
34.	20070010065 11352279	1/11/2007 2/13/2006	METHOD OF MAKING A CAPACITIVE SUBSTRATE FOR USE AS PART OF A LARGER CIRCUITIZED SUBSTRATE, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE AND METHOD OF MAKING AN INFORMATION HANDLING SYSTEM INCLUDING SAID CIRCUITIZED SUBSTRATE
35.	20070010064 11352276	1/11/2007 2/13/2006	METHOD OF MAKING A CAPACITIVE SUBSTRATE USING PHOTOIMAGEABLE DIELECTRIC FOR USE AS PART OF A LARGER CIRCUITIZED SUBSTRATE, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE AND METHOD OF MAKING AN INFORMATION HANDLING SYSTEM INCLUDING SAID CIRCUITIZED SUBSTRATE
36.	20070007033 11244180	1/11/2007 10/6/2005	CIRCUITIZED SUBSTRATE WITH SOLER-COATED MICROPARTICLE PASTE

NO.	PATENT NO./ PUBLICATION NO./ SERIAL NO.	DATE ISSUED/ DATE FILED	TITLE:
			CONNECTIONS, MULTI-LAYERED SUBSTRATE ASSEMBLY, ELECTRICAL ASSEMBLY AND INFORMATION HANDLING SYSTEM UTILIZING SAME AND METHOD OF MAKING SAID SUBSTRATE
37.	20060248717 11482945	11/9/2006 7/10/2006	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH FILLED ISOLATION BORDER
38.	20060240594 11455183	10/26/2006 6/19/2006	METHOD OF MAKING STACKED CHIP ELECTRONIC PACKAGE HAVING LAMINATE CARRIER
39.	20060240364 11110920	10/26/2006 4/21/2005	APPARATUS AND METHOD FOR MAKING CIRCUITIZED SUBSTRATES HAVING PHOTO-IMAGEABLE DIELECTRIC LAYERS IN A CONTINUOUS MANNER
40.	20060214010 11401401	9/28/2006 4/11/2006	CIRCUITIZED SUBSTRATE WITH SHIELDED SIGNAL LINES AND PLATED-THRU-HOLES AND METHOD OF MAKING SAME, AND ELECTRICAL ASSEMBLY AND INFORMATION HANDLING SYSTEM UTILIZING SAME
41.	20060213973 11086324	9/28/2006 3/23/2005	ELECTRONIC CARD ASSEMBLY
42.	20060200977 11429990	9/14/2006 5/9/2006	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH SIGNAL WIRE SHIELDING
43.	20060180936 11390386	8/17/2006 3/28/2006	FLUOROPOLYMER DIELECTRIC COMPOSITION FOR USE IN CIRCUITIZED SUBSTRATES AND CIRCUITIZED SUBSTRATE INCLUDING SAME
44.	20060180343 11215206	8/17/2006 8/31/2005	CIRCUITIZED SUBSTRATE UTILIZING THREE SMOOTH-SIDED CONDUCTIVE LAYERS AS PART THEREOF AND ELECTRICAL ASSEMBLIES

NO.	PATENT NO./ PUBLICATION NO./ SERIAL NO.	DATE ISSUED/ DATE FILED	TITLE:
			AND INFORMATION HANDLING SYSTEMS UTILIZING SAME
45.	20060154501 11324273	7/13/2006 1/4/2006	CAPACITOR MATERIAL WITH METAL COMPONENT FOR USE IN CIRCUITIZED SUBSTRATES, CIRCUITIZED SUBSTRATE UTILIZING SAME, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE, AND INFORMATION HANDLING SYSTEM UTILIZING SAID CIRCUITIZED SUBSTRATE
46.	20060151863 11031085	7/13/2006 1/10/2005	CAPACITOR MATERIAL FOR USE IN CIRCUITIZED SUBSTRATES, CIRCUITIZED SUBSTRATE UTILIZING SAME, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE, AND INFORMATION HANDLING SYSTEM UTILIZING SAID CIRCUITIZED SUBSTRATE
47.	20060125103 11350777	6/15/2006 2/10/2006	INFORMATION HANDLING SYSTEM
48.	20060121722 11334445	6/8/2006 1/19/2006	METHOD OF MAKING PRINTED CIRCUIT BOARD HAVING VARYING DEPTH CONDUCTIVE HOLES
49.	20060054870 11265287	3/16/2006 11/3/2005	DIELECTRIC COMPOSITION FOR USE IN CIRCUITIZED SUBSTRATES AND CIRCUITIZED SUBSTRATE INCLUDING SAME
50.	20050289019 10860067	12/29/2005 6/4/2004	METHOD AND SYSTEM FOR TRACKING GOODS
51.	20050218524 11086323	10/6/2005 3/23/2005	LOW MOISTURE ABSORPTIVE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME

NO.	PATENT NO./ PUBLICATION NO./ SERIAL NO.	DATE ISSUED/ DATE FILED	TITLE:
52.	20050137890 10740500	6/23/2005 12/22/2003	ITEM IDENTIFICATION AND CONTROL SYSTEM
53.	20040242270 10449019	12/2/2004 6/2/2003	ELECTRONIC CARD
54.	20040238970 10868066	12/2/2004 6/16/2004	ELECTRONIC PACKAGE WITH CONDUCTIVE PAD CAPABLE OF WITHSTANDING SIGNIFICANT LOADS
55.	7416996 11349990	8/26/2008 2/9/2006	METHOD OF MAKING CIRCUITIZED SUBSTRATE
56.	7416972 11730942	8/26/2008 4/5/2007	METHOD OF MAKING SAME LOW MOISTURE ABSORPTIVE CIRCUITIZED SUBSTRATE WITH REDUCED THERMAL EXPANSION
57.	7384856 11172794	6/10/2008 7/5/2005	METHOD OF MAKING AN INTERNAL CAPACITIVE SUBSTRATE FOR USE IN A CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE
58.	7383629 10991532	6/10/2008 11/19/2004	METHOD OF MAKING CIRCUITIZED SUBSTRATES UTILIZING SMOOTH-SIDED CONDUCTIVE LAYERS AS PART THEREOF
59.	7381587 11324432	6/3/2008 1/4/2006	METHOD OF MAKING CIRCUITIZED SUBSTRATE
60.	7377033 11641810	5/27/2008 12/20/2006	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH SPLIT CONDUCTIVE LAYER AND INFORMATION HANDLING SYSTEM UTILIZING SAME
61.	7348677 11397713	3/25/2008 4/5/2006	METHOD OF PROVIDING PRINTED CIRCUIT BOARD WITH CONDUCTIVE HOLES AND BOARD RESULTING THEREFROM
62.	7343674 11349998	3/18/2008 2/9/2006	METHOD OF MAKING CIRCUITIZED SUBSTRATE ASSEMBLY
63.	7342183 11177442	3/11/2008 7/11/2005	CIRCUITIZED SUBSTRATE WITH SINTERED PASTE CONNECTIONS, MULTILAYERED SUBSTRATE ASSEMBLY, ELECTRICAL ASSEMBLY

NO.	PATENT NO./ PUBLICATION NO./ SERIAL NO.	DATE ISSUED/ DATE FILED	TITLE:
			AND INFORMATION HANDLING SYSTEM UTILIZING SAME
64.	7334323 11177413	2/26/2008 7/11/2005	METHOD OF MAKING MULTILAYERED CIRCUITIZED SUBSTRATE ASSEMBLY HAVING SINTERED PASTE CONNECTIONS
65.	7332818 11127160	2/19/2008 5/12/2005	MULTI-CHIP ELECTRONIC PACKAGE WITH REDUCED LINE SKEW AND CIRCUITIZED SUBSTRATE FOR USE THEREON
66.	7332212 11242841	2/19/2008 10/5/2005	CIRCUITIZED SUBSTRATE WITH CONDUCTIVE POLYMER AND SEED MATERIAL ADHESION LAYER
67.	7328502 11882625	2/12/2008 8/3/2007	APPARATUS FOR MAKING CIRCUITIZED SUBSTRATES IN A CONTINUOUS MANNER
68.	7326643 11808596	2/5/2008 6/12/2007	METHOD OF MAKING CIRCUITIZED SUBSTRATE WITH INTERNAL ORGANIC MEMORY DEVICE
69.	7307022 11327493	12/11/2007 1/9/2006	METHOD OF TREATING CONDUCTIVE LAYER FOR USE IN A CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAID SUBSTRATE HAVING SAID CONDUCTIVE LAYER AS PART THEREOF
70.	7294791 10953923	11/13/2007 9/29/2004	CIRCUITIZED SUBSTRATE WITH IMPROVED IMPEDANCE CONTROL CIRCUITRY, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY AND INFORMATION HANDLING SYSTEM UTILIZING SAME
71.	7293355 11110919	11/13/2007 4/21/2005	APPARATUS AND METHOD FOR MAKING CIRCUITIZED SUBSTRATES IN A CONTINUOUS MANNER
72.	7292055 11110901	11/6/2007 4/21/2005	INTERPOSER FOR USE WITH TEST APPARATUS
73.	7270845	9/18/2007	DIELECTRIC

NO.	PATENT NO./ PUBLICATION NO./ SERIAL NO.	DATE ISSUED/ DATE FILED	TITLE:
	10812889	3/31/2004	COMPOSITION FOR FORMING DIELECTRIC LAYER FOR USE IN CIRCUITIZED SUBSTRATES
74.	7253518 11152048	8/7/2007 6/15/2005	WIREBOND ELECTRONIC PACKAGE WITH ENHANCED CHIP PAD DESIGN, METHOD OF MAKING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME
75.	7253502 10900385	8/7/2007 7/28/2004	CIRCUITIZED SUBSTRATE WITH INTERNAL ORGANIC MEMORY DEVICE, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME
76.	7235745 11172786	6/26/2007 7/5/2005	RESISTOR MATERIAL WITH METAL COMPONENT FOR USE IN CIRCUITIZED SUBSTRATES, CIRCUITIZED SUBSTRATE UTILIZING SAME, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE, AND INFORMATION HANDLING SYSTEM UTILIZING SAID CIRCUITIZED SUBSTRATE
77.	7211470 11216133	5/1/2007 9/1/2005	METHOD AND APPARATUS FOR DEPOSITING CONDUCTIVE PASTE IN CIRCUITIZED SUBSTRATE OPENINGS
78.	7211289 10737974	5/1/2007 12/18/2003	METHOD OF MAKING MULTILAYERED PRINTED CIRCUIT BOARD WITH FILLED CONDUCTIVE HOLES
79.	7209368 10790747	4/24/2007 3/3/2004	CIRCUITIZED SUBSTRATE WITH SIGNAL WIRE SHIELDING, ELECTRICAL ASSEMBLY UTILIZING SAME AND METHOD OF MAKING
80.	7176383 10740398	2/13/2007 12/22/2003	PRINTED CIRCUIT BOARD WITH LOW CROSS-TALK NOISE
81.	7169313 11128272	1/30/2007 5/13/2005	PLATING METHOD FOR CIRCUITIZED SUBSTRATES

NO.	PATENT NO./ PUBLICATION NO./ SERIAL NO.	DATE ISSUED/ DATE FILED	TITLE:
82.	7163847 11258092	1/16/2007 10/26/2005	METHOD OF MAKING CIRCUITIZED SUBSTRATE
83.	7161810 11238960	1/9/2007 9/30/2005	STACKED CHIP ELECTRONIC PACKAGE HAVING LAMINATE CARRIER AND METHOD OF MAKING SAME
84.	7157647 10882170	1/2/2007 7/2/2004	CIRCUITIZED SUBSTRATE WITH FILLED ISOLATION BORDER, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME
85.	7157646 10882167	1/2/2007 7/2/2004	CIRCUITIZED SUBSTRATE WITH SPLIT CONDUCTIVE LAYER, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME
86.	7152319 10811817	12/26/2006 3/30/2004	METHOD OF MAKING HIGH SPEED CIRCUIT BOARD
87.	7145221 10920235	12/5/2006 8/18/2004	LOW MOISTURE ABSORPTIVE CIRCUITIZED SUBSTRATE, METHOD OF MAKING SAME, ELECTRICAL ASSEMBLY UTILIZING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME
88.	7142121 10860071	11/28/2006 6/4/2004	RADIO FREQUENCY DEVICE FOR TRACKING GOODS
89.	7129732 11281456	10/31/2006 11/18/2005	SUBSTRATE TEST APPARATUS AND METHOD OF TESTING SUBSTRATES
90.	7109732 10630722	9/19/2006 7/31/2003	ELECTRONIC COMPONENT TEST APPARATUS
91.	7091066 11259043	8/15/2006 10/27/2005	METHOD OF MAKING CIRCUITIZED SUBSTRATE
92.	7087846 10423972	8/8/2006 4/28/2003	PINNED ELECTRONIC PACKAGE WITH STRENGTHENED CONDUCTIVE PAD
93.	7087441 10968929	8/8/2006 10/21/2004	METHOD OF MAKING A CIRCUITIZED SUBSTRATE HAVING A PLURALITY OF

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			SOLDER CONNECTION SITES THEREON
94.	7084014 10679302	8/1/2006 10/7/2003	METHOD OF MAKING CIRCUITIZED SUBSTRATE
95.	7078816 10812890	7/18/2006 3/31/2004	CIRCUITIZED SUBSTRATE
96.	7071423 10915483	7/4/2006 8/11/2004	CIRCUITIZED SUBSTRATE ASSEMBLY AND METHOD OF MAKING SAME
97.	7063762 10643909	6/20/2006 8/20/2003	CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAME
98.	7047630 10811915	5/23/2006 3/30/2004	METHOD OF MAKING CIRCUITIZED SUBSTRATE ASSEMBLY
99.	7045897 10900386	5/16/2006 7/28/2004	ELECTRICAL ASSEMBLY WITH INTERNAL MEMORY CIRCUITIZED SUBSTRATE HAVING ELECTRONIC COMPONENTS POSITIONED THEREON, METHOD OF MAKING SAME, AND INFORMATION HANDLING SYSTEM UTILIZING SAME
100.	7035113 10394107	4/25/2006 3/24/2003	MULTI-CHIP ELECTRONIC PACKAGE HAVING LAMINATE CARRIER AND METHOD OF MAKING SAME
101.	7025607 11031074	4/11/2006 1/10/2005	CAPACITOR MATERIAL WITH METAL COMPONENT FOR USE IN CIRCUITIZED SUBSTRATES, CIRCUITIZED SUBSTRATE UTILIZING SAME, METHOD OF MAKING SAID CIRCUITIZED SUBSTRATE, AND INFORMATION HANDLING SYSTEM UTILIZING SAID CIRCUITIZED SUBSTRATE
102.	7023707 10394135	4/4/2006 3/24/2003	INFORMATION HANDLING SYSTEM
103.	7013563 10616932	3/21/2006 7/11/2003	METHOD OF TESTING SPACINGS IN PATTERNS OF OPENINGS IN PCB CONDUCTIVE LAYER
104.	6995322 10955741	2/7/2006 9/30/2004	HIGH SPEED CIRCUITIZED SUBSTRATE WITH REDUCED THRU-HOLE

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			STUB, METHOD FOR FABRICATION AND INFORMATION HANDLING SYSTEM UTILIZING SAME
105.	6992896 10661616	1/31/2006 9/15/2003	STACKED CHIP ELECTRONIC PACKAGE HAVING LAMINATE CARRIER AND METHOD OF MAKING SAME
106.	6964884 10991451	11/15/2005 11/19/2004	CIRCUITIZED SUBSTRATES UTILIZING THREE SMOOTH-SIDED CONDUCTIVE LAYERS AS PART THEREOF, METHOD OF MAKING SAME, AND ELECTRICAL ASSEMBLIES AND INFORMATION HANDLING SYSTEMS UTILIZING SAME
107.	6958106 10409066	10/25/2005 4/9/2003	MATERIAL SEPARATION TO FORM SEGMENTED PRODUCT
108.	6905589 10370529	6/14/2005 2/24/2003	CIRCUITIZED SUBSTRATE AND METHOD OF MAKING SAME
109.	6900392 10933260	5/31/2005 9/3/2004	INFORMATION HANDLING SYSTEM UTILIZING CIRCUITIZED SUBSTRATE
110.	6872894 10379575	3/29/2005 3/6/2003	INFORMATION HANDLING SYSTEM UTILIZING CIRCUITIZED SUBSTRATE
111.	6828514 10354000	12/7/2004 1/30/2003	HIGH SPEED CIRCUIT BOARD AND METHOD FOR FABRICATION
112.	6815837 10423877	11/9/2004 4/28/2003	ELECTRONIC PACKAGE WITH STRENGTHENED CONDUCTIVE PAD
113.	6809269 10322527	10/26/2004 12/19/2002	CIRCUITIZED SUBSTRATE ASSEMBLY AND METHOD OF MAKING SAME
114.	11907006	10/9/2007	PCB WITH OPTICAL PATHWAYS
115.	11907004	10/9/2007	PCB WITH OPTICAL PATHWAYS
116.	11976468	10/25/2007	IC/PACKAGE WITH THERMAL COOLING STRUCTURE
117.	12007820	1/16/2008	STRUCTURE AND METHOD FOR HIGH-SPEED PRECISION RESISTOR

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			FORMATION
118.	12148271	4/17/2008	CIRCUITIZED SUBSTRATES UTILIZING SMOOTH-SIDED CONDUCTIVE LAYERS AS PART THEREOF
119.	11598647	11/14/2006	MULTILAYERED LAMINATE ASSEMBLY PROCESS
120.	11730212	3/30/2007	HASL ALTERNATIVE PROCESSING FOR WIREBOND PACKAGES
121.	11727314	3/26/2007	ELECTRONIC PACKAGE WITH SHRINKING ADHESIVE
122.	11882149	7/31/2007	STRUCTURE AND METHOD FOR OPTIMIZED ADHESION OF GOLD SURFACES TO ELECTRONIC DEVICES
123.	11783306	4/9/2007	STACKED CHIP PACKAGE
124.	11808140	6/7/2007	METHOD AND STRUCTURE FOR OUT OF THE PLANE PWB
125.	11730404	4/2/2007	FORMED LED CIRCUIT BOARD HEAT SINK
126.	11878673	7/26/2007	MULTILAYER EMBEDDED CAPACITORS (MLECS)
127.	12007704	1/15/2008	COST EFFECTIVE LARGE BOARD STRUCTURE AND BUILD METHODOLOGY
128.	12078206	3/28/2008	Z-INTERCONNECT JOINING STRUCTURE AND METHOD FOR HIGH SPEED PWBS
129.	12215079	6/24/2008	SPRING ACTUATED LGA CLAMPING MECHANISM