PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Icemos Technology Corporation	09/17/2008

RECEIVING PARTY DATA

Name:	Icemos Technology Ltd.
Street Address:	5 Hannahstown Hill
City:	Belfast
State/Country:	UNITED KINGDOM
Postal Code:	BT17 0LT

PROPERTY NUMBERS Total: 58

Property Type	Number
Application Number:	60673935
Application Number:	10596720
Application Number:	60677510
Application Number:	11381605
Application Number:	12202638
Application Number:	11925329
Application Number:	60706918
Application Number:	11463613
Application Number:	12116286
Application Number:	60710234
Application Number:	11466132
Application Number:	12191035
Application Number:	60725876
Application Number:	11548546
Application Number:	12142185

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Application Number:	12204371
Application Number:	60778481
Application Number:	11681543
Application Number:	12116638
Application Number:	60778480
Application Number:	11681576
Application Number:	60806150
Application Number:	11772104
Application Number:	60750873
Application Number:	11609934
Application Number:	60822261
Application Number:	60822263
Application Number:	11838359
Application Number:	60731171
Application Number:	11554437
Application Number:	12175586
Application Number:	11380457
Application Number:	11675407
Application Number:	12203995
Application Number:	60821993
Application Number:	11837150
Application Number:	61020540
Application Number:	60913432
Application Number:	11962523
Application Number:	60913425
Application Number:	12029857
Application Number:	60915939
Application Number:	11962530
Application Number:	60975878
Application Number:	12031895
Application Number:	12031909
Application Number:	61028215
Application Number:	61028321
Application Number:	61040210
PCT Number:	US0615310

PCT Number:	US0617024
PCT Number:	US0715253
PCT Number:	US0775810
PCT Number:	US0767640
PCT Number:	US0775613
PCT Number:	US0789036
PCT Number:	US0861139
PCT Number:	US0789048

CORRESPONDENCE DATA

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ATTORNEY DOCKET NUMBER:	681443-5002
NAME OF SUBMITTER:	John D. Simmons

Total Attachments: 9
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ASSIGNMENT

WHEREAS, the inventors listed in Schedule A (hereinafter referred to as "Inventor-Assignors") respectively invented certain new and useful inventions as listed in Schedule B, for which United States patent applications were filed as described in Schedule B (hereinafter the "Applications");

WHEREAS, in respective Original Assignments listed in Schedule B, Inventor-Assignors previously assigned rights in the inventions, Applications, foreign applications derived therefrom, and in any patents issuing thereon (hereinafter the "Patents") to Icemos Technology Corporation, a Delaware Corporation, having an address of P.O. Box 24619, Tempe, Arizona, 85285 (hereinafter the "Assignor"), which Assignments were recorded in the U.S. Patent and Trademark Office as described in Schedule B (such Assignments hereinafter referred to as the "Original Assignments");

WHEREAS, a mistake was made by the Inventor-Assignors and Assignor, since the Original Assignments should have been made to Icemos Technology Ltd. (hereinafter referred to as the "Assignee"), the Assignee having a current address of 5 Hannahstown Hill, Belfast BT17 0LT, Northern Ireland, United Kingdom, because the Inventor-Assignors generally work for the Assignee, the development work for the inventions described in the Applications and Patents was performed using the equipment and facilities of the Assignee, and the Assignee is the manufacturer of any products covered by the inventions described in the Applications and Patents; and

WHEREAS, the Assignor and Assignee wish to confirm the intended assignments to the Assignee of the inventions, Applications, foreign applications derived therefrom, and the Patents, as well as any and all choses in action, including all claims for damages and injunctive relief by reason of past, present or future infringement of the Applications and/or Patents issuing from the Applications, with the right to sue for and collect such damages and injunctive relief for its own use and behalf; and wish to properly indicate that title of the inventions, Applications, foreign applications derived therefrom, and the Patents are in the Assignee;

NOW, THEREFORE, for good and valuable consideration, the full receipt and sufficiency of which are hereby acknowledged, the Assignor and the Assignee, intending to be legally bound, do hereby agree and confirm, *nunc pro tunc*, as of the respective dates of the Original Assignments, as listed in Schedule B, as follows:

Assignor, assigns, transfers and conveys to the Assignee the whole and entire right, title and interest for the United States and its possessions and territories and all foreign countries in and to the inventions which are disclosed in the Applications listed in Schedule B, in and to any and all patent applications related thereto including, but not limited to, all provisionals, non-provisionals, divisionals, continuations, continuations-in-part, substitutes, reexaminations, reissues and all other applications for patent which have been or shall be filed in the United States and all foreign countries on the inventions; the Patents and any and reissued and

reexamined patents and extensions thereof which have been or shall be issued in the United States and all foreign countries on the inventions, to the full end of the term or terms for which the patent(s) may be granted, as fully and entirely as the same would have been held by the undersigned Assignor had this Assignment not been made; and specifically including all rights of priority created by the Applications under any treaty, convention or law relating thereto, as well as any and all choses in action, including all claims for damages and injunctive relief by reason of past, present or future infringement of the Patents, with the right to sue for and collect such damages and injunctive relief for its own use and behalf.

Assignor warrants and represents that no assignment (other than the Original Assignments), grant, mortgage, license or other agreement affecting the rights and properties herein conveyed has been or will be made to others by the Assignor, and that the full right to convey the same as herein expressed was originally possessed by the Assignor;

This Assignment is to be binding on the heirs, assigns, representatives and successors of the Assignor and extend to the successors, assigns, and nominees of the Assignee.

Executed, *nunc pro tunc*, as of the respective date of the original assignments, by the parties as follows:

Assignor:

Icemos Technology Corporation
(by Matt Dick, CFO)

9-17-08
Date

SCHEDULE A - INVENTORS

Full name inventor	Samuel Anderson
Residence	Tempe, Arizona
Citizenship	United Kingdom
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Full name inventor	Conor Brogan
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Citizenship	United Kingdom
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Full name inventor	Xu Cheng
Residence	Chandler, Arizona
Citizenship	China
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Full name inventor	Hugh J. Griffin
Residence	Newtownabbey, United Kingdom
Citizenship	United Kingdom
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SCHEDULE A - INVENTORS

Full name inventor	Takeshi Ishiguro
Residence	Fukushima-ken, Japan
Citizenship	Japan
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Full name inventor	Cormac MacNamara
Residence	Belfast, United Kingdom
Citizenship	United Kingdom
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Full name inventor	Kenji Sugiura
Residence	Kawasaki-shi, Japan
Citizenship	Japan
Post Office Address	1-17-9-2, Arima, Miyamae-ku, Kawasaki-shi 216-0003

Full name inventor	Koon Chong So
Residence	Tempe, Arizona
Citizenship	United States
Post Office Address	7855 South River Parkway P.O. Box 24619, Tempe, Arizona 85284

SCHEDULE A - INVENTORS

Full name inventor	Robin Wilson
Residence	Belfast, United Kingdom
Citizenship	United Kingdom
Post Office Address	41 Loopland Gardens, Belfast, BT6 9EB United Kingdom

SCHEDULE B - ASSIGNMENTS

INVENTION	INVENTORS	REEL/FRAME NO.	EXEC DATE	REC DATE	APPLICATION NOS.
Superjunction Device having Oxide Lined Trenches and Method for Manufacturing a Superjunction Device having Oxide Lined Trenches	Samuel Anderson	016308/0189	5/6/2005	7/26/2005	60/673,935 TW 95114267 PCT/US2006/015310 CN 200680013510.6 EP 06751120.4 JP 2008-507968 KR 10-2007-7026601
		020102/0153	11/7/2007	11/13/2007	10/596,720
Silicon Wafer Having Through-Wafer Vias	Cormac MacNamara Conor Brogan Hugh J. Griffin Robin Wilson	017631/0422	4/18/2005 4/23/2005 4/26/2005	5/17/2006	60/677,510 TW 95115728 PCT/US2006/017024 CN 200680015411.1 EP 06769996.7 JP 2008-510176 KR 10-2007-7027859
		018624/0517	7/25/2006 11/9/2006	12/13/2006	11/381,605 12/202,638
		020379/0029	1/10/2008	1/17/2008	11/925,329
Positive-Intrinsic-Negative (PIN)/Negative-Intrinsic-Positive (NIP) Diode	Robin Wilson Conor Brogan Hugh J. Griffin Cormac MacNamara	016505/0873	8/25/2005 8/29/2005 8/30/2005	9/8/2005	60/706,918
		018624/0187	11/20/2006 11/21/2006	12/13/2006	11/463,613 12/116,286
Bonded-wafer Superjunction Semiconductor Device	Cormac MacNamara Conor Brogan Hugh J. Griffin Robin Wilson	016620/0754	8/25/2005 8/30/2005	10/5/2005	60/710,234
		018624/0573	11/20/2006 11/21/2006	12/13/2006	11/466,132 12/191,035
Photodetector Array Using Isolation Diffusions as Crosstalk Inhibitors Between Adjacent Pixels	Robin Wilson Conor Brogan Hugh J. Griffin	018624/0573	4/18/2006 4/23/2006 4/26/2006	5/17/2006	60/725,876

SCHEDULE B - ASSIGNMENTS

INVENTION	INVENTORS	REEL/FRAME NO.	EXEC DATE	REC DATE	APPLICATION NOS.
	Cormac MacNamara	018695/0056	10/31/2006 11/2/2006	12/19/2006	11/548,546 12/142,185 12/204,371
Front Side Electrical Contact for Photodetector Array and Method of Making Same	Robin Wilson Conor Brogan Hugh J. Griffin Cormac MacNamara	017631/0242	4/18/2006 4/23/2006 4/26/2006	5/17/2006	60/778,481 JP 2008-_____ (filed 9/2/2008)
		019309/0664	4/30/2007 5/14/2007	5/17/2007	11/681,543 12/116,638
Photodiode Having Increased Proportion of Light-Sensitive Area To Light-Insensitive Area	Robin Wilson Conor Brogan Hugh J. Griffin Cormac MacNamara	017631/0328	4/18/2006 4/23/2006 4/26/2006	5/17/2006	60/778,480 JP 2008-_____ (filed 9/2/2008)
		019308/0988	4/30/2007 5/14/2007	5/17/2007	11/681,576
Varying Pitch Adapter and a Method of Forming a Varying Pitch Adapter	Conor Brogan Cormac MacNamara Hugh J. Griffin Robin Wilson	018164/0399	7/25/2006 7/31/2006	8/24/2006	60/806,150 TW 96124449 PCT/US2007/015253
		019670/0922	7/9/2007 7/10/2007	8/9/2007	11/772,104
Backlit Photodiode and Method of Manufacturing a Backlit Photodiode	Robin Wilson Conor Brogan Hugh J. Griffin Cormac MacNamara	017630/0723	4/18/2006 4/23/2006 4/26/2006	5/17/2006	60/750,873 JP 2006-337706
		018952/0139	1/15/2007 1/17/2007 1/19/2007	3/2/2007	11/609,934
Sealed Trench in a Super Junction Schottky Diode and Method of Making the Same Semiconductor Devices With Sealed, Unlined Trenches and Methods of Forming Same	Samuel Anderson Koon Chong So	018228/0994	8/25/2006 8/31/2006	9/11/2006	60/822,261 TW 96129812 PCT/US2007/075810
		018229/0009	8/25/2006 8/31/2006	9/11/2006	60/822,263 TW 96129812 PCT/US2007/075810
		019993/0001	10/18/2007	10/22/2007	11/838,359

SCHEDULE B - ASSIGNMENTS

INVENTION	INVENTORS	REEL/FRAME NO.	EXEC DATE	REC DATE	APPLICATION NOS.
Front Lit PIN/NIP Diode Having a Continuous Anode/Cathode	Robin Wilson Conor Brogan Hugh J. Griffin Cormac MacNamara	017631/0216	4/18/2006 4/23/2006 4/26/2006	5/17/2006	60/731,171
		018702/0615	11/20/2006 11/21/2006	1/3/2007	11/554,437 12/175,586
Technique for Stable Processing of Thin/Fragile Substrates	Robin Wilson Conor Brogan Hugh J. Griffin Cormac MacNamara	017629/0764	4/18/2006 4/23/2006 4/26/2006	5/17/2006	11/380,457 11/675,407 12/203,995 TW 96113603 PCT/US2007/067640
Method of Manufacturing a Photodiode Array with Through-Wafer Vias	Robin Wilson Conor Brogan Cormac MacNamara Hugh J. Griffin	018105/0379	7/25/2006 7/31/2006	8/15/2006	60/821,993 TW 96129395 PCT/US2007/075613
		020378/0950	1/10/2008 1/11/2008	1/17/2008	11/837,150
Superjunction Semiconductor Device Having a Dielectric Termination and Methods for Manufacturing the Device	Xu Cheng	020356/0209	6/7/2007	1/11/2008	61/020,540
Methods for Manufacturing A Trench Type Semiconductor Device Having a Thermally Sensitive Refill Material	Takeshi Ishiguro	019195/0755	4/19/2007	4/23/2007	60/913,432 TW 97101331 PCT/US2007/089036
		020363/0662	12/17/2007	1/15/2008	11/962,523
Methods for Manufacturing a Trench Type Semiconductor Device Having A Thermally Sensitive Refill Material	Takeshi Ishiguro	019195/0689	4/19/2007	4/23/2007	60/913,425 TW 97114464 PCT/US2008/061139
		020514/0741	1/10/2008	2/15/2008	12/029,857
Superjunction Devices Having Narrow Surface Layout of Terminal Structures And Methods of Manufacturing The Devices	Takeshi Ishiguro	019248/0193	4/19/2007	5/4/2007	60/915,939 TW 97101329 PCT/US2007/089048
		020363/0679	12/13/2007	1/15/2008	11/962,530

SCHEDULE B - ASSIGNMENTS

INVENTION	INVENTORS	REEL/FRAME NO.	EXEC DATE	REC DATE	APPLICATION NOS.
Multi-Directional Trenching in Manufacturing Superjunction Devices	Takeshi Ishiguro Hugh J. Griffin Kenji Sugiura	019986/0024	10/12/2007 10/19/2007	10/19/2007	60/975,878
		020514/0741	1/10/2008 2/11/2008	2/25/2008	12/031,895
		020554/0723	1/10/2008 2/11/2008	2/25/2008	12/031,909
Multi-Angle Rotation for Ion Implantation of Trenches in Superjunction Devices	Takeshi Ishiguro Hugh J. Griffin Kenji Sugiura	020524/0531	1/10/2008	2/19/2008	61/028,215
Trench Depth Monitor for Semiconductor Manufacturing	Takeshi Ishiguro Hugh J. Griffin Kenji Sugiura	020797/0904	2/21/2008 4/11/2008	4/14/2008	61/028,321
Bonded Wafer Substrate for Use in MEMS Structures	Robin Wilson	020731/0674	3/21/2008	4/1/2008	61/040,210