PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Applied Micro Circuits Corporation	07/15/2008

RECEIVING PARTY DATA

Name:	Qualcomm Incorporated
Street Address:	5775 Morehouse Drive
City:	San Diego
State/Country:	CALIFORNIA
Postal Code:	92121-1714

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	12317296

CH $40.00 12317296

CORRESPONDENCE DATA

Fax Number: (858)658-2520
Correspondence will be sent via US Mail when the fax attempt is unsuccessful.
Phone: 858-845-2174
Email: trlasher@qualcomm.com
Correspondent Name: Qualcomm Incorporated
Address Line 1: 5775 Morehouse Drive
Address Line 4: San Diego, CALIFORNIA 92121-1714

ATTORNEY DOCKET NUMBER:	082713C1
NAME OF SUBMITTER:	Thomas Lasher

Total Attachments: 10
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ASSIGNMENT OF PATENTS AND PATENT APPLICATIONS

WHEREAS, Applied Micro Circuits Corporation, a corporation organized under the laws of Delaware, is the owner of certain patents and patent applications, as more particularly described on Attachment 1 and Attachment 2, respectively, hereto; and

WHEREAS, Applied Micro Circuits Corporation has agreed to assign all of its right, title and interest in and to such patents and patent applications listed on Attachment 1 and Attachment 2, respectively, attached hereto and all reissues, reexaminations, extensions, divisions, continuations, continuations-in-part and foreign counterparts of such patents and patent applications arising from or related thereto, to QUALCOMM Incorporated, a corporation organized under the laws of Delaware, pursuant to a certain Patent Purchase Agreement of even date herewith and further evidence such assignment in this Assignment.

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged:

Applied Micro Circuits Corporation hereby sells, assigns, transfers and conveys to QUALCOMM Incorporated, and its successors and assigns, all right, title, and interest in and to each of the patents and patent applications listed on Attachment 1 and Attachment 2, respectively, attached hereto and all reissues, reexaminations, extensions, divisions, continuations, continuations-in-part and foreign counterparts of such patents and patent applications arising from or related thereto.

This sale, assignment, transfer and conveyance to QUALCOMM Incorporated, and its successors and assigns, is made subject to certain nonexclusive retained rights in favor of Applied Micro Circuits Corporation and certain pre-existing nonexclusive patent licenses granted by Applied Micro Circuits Corporation for the patents and patent applications listed on Attachment 1 and Attachment 2, respectively, attached hereto and all reissues, reexaminations, extensions, divisions, continuations, continuations-in-part and foreign counterparts of such patents and patent applications arising from or related thereto, all as are set forth in that certain Patent Purchase Agreement by and between QUALCOMM Incorporated and Applied Micro Circuits Corporation effective as of July 11, 2008, as amended (the "Agreement"). As to such nonexclusive retained rights, Applied Micro Circuits Corporation hereby acknowledges and agrees that, on and after this sale, assignment, transfer and conveyance, Applied Micro Circuits Corporation shall not retain any right under such patents and patent applications listed on Attachment 1 and Attachment 2, respectively, attached hereto and all reissues, reexaminations, extensions, divisions, continuations, continuations-in-part and foreign counterparts of such patents and patent applications arising from or related thereto: (i) to commence or prosecute any patent infringement litigation (including, but not limited to, any past claim of infringement) or procedure for resolution of a controversy (or to indicate or convey, either expressly, by implication or otherwise, any intention to do so), whether arising or created by any claim, counterclaim or otherwise (as determined in the broadest sense and in whatever form), and whether administrative, judicial, arbitral or otherwise, including, but not limited to, any proceeding before the U.S. International Trade Commission or in any jurisdiction throughout the world; or (ii) to exclude others (including, but not limited to, QUALCOMM Incorporated) from making, having made, selling, offering to sell, using, importing or otherwise disposing of any products or services, or from practicing or having practiced any of the inventions claimed therein.

Initials:

This sale, assignment, transfer and conveyance to QUALCOMM Incorporated, and its successors and assigns, also includes, without limitation, the right to enforce, assert and sue for past, present and future infringement on each of the foregoing items, including without limitation the right to seek injunctive relief, and the right to recover and collect for past, present and future damages with respect thereto.

IN WITNESS WHEREOF, the undersigned has caused this Assignment of Patents and Patent Applications to be executed on July 15, 2008.

Applied Micro Circuits Corporation

By: Cynthia J Moreland

Name: Cynthia J Moreland

Title: VP, General Counsel

STATE OF CALIFORNIA)
) SS
COUNTY OF Santa Clara

The foregoing Assignment of Patents and Patent Applications was hereby acknowledged and executed before me on this 15 day of July, 2008 by Cynthia J Moreland as VP General Counsel of Applied Micro Circuits Corporation, a corporation organized under the laws of Delaware, on behalf of such corporation.

Notary Public:

My commission expires: 1/31/2011

KENDALL R. SUMMERS
COMM. #1714159
NOTARY PUBLIC - CALIFORNIA
SANTA CLARA COUNTY
COMM. EXPIRES JAN. 31, 2011

Initials: MGC

CALIFORNIA ALL-PURPOSE CERTIFICATE OF ACKNOWLEDGMENT

State of California

County of Santa Clara

On July 15, 2010 before me, KENDALL R. SUMMERS NOTARY PUBLIC
(Here insert name and title of the officer)

personally appeared Emma I. Morelos

who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is/are subscribed to the within instrument and acknowledged to me that he/she/they executed the same in his/her/their authorized capacity(ies), and that by his/her/their signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

KENDALL R. SUMMERS
COMM. #1714159
NOTARY PUBLIC - CALIFORNIA
SANTA CLARA COUNTY
COMM. EXPIRES JAN. 31, 2011

Signature of Notary Public (Notary Seal)

ADDITIONAL OPTIONAL INFORMATION

DESCRIPTION OF THE ATTACHED DOCUMENT

(Title or description of attached document)

(Title or description of attached document continued)

Number of Pages _____ Document Date _____

(Additional information)

CAPACITY CLAIMED BY THE SIGNER

- ☐ Individual(s)
- ☐ Corporate Officer

(Title)

- ☐ Partner(s)
- ☐ Attorney-in-Fact
- ☐ Trustee(s)
- ☐ Other _____

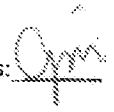
INSTRUCTIONS FOR COMPLETING THIS FORM

Any acknowledgment completed in California must contain verbiage exactly as appears above in the notary section or a separate acknowledgment form must be properly completed and attached to that document. The only exception is if a document is to be recorded outside of California. In such instances, any alternative acknowledgment verbiage as may be printed on such a document so long as the verbiage does not require the notary to do something that is illegal for a notary in California (i.e. certifying the authorized capacity of the signer). Please check the document carefully for proper notarial wording and attach this form if required.

- State and County information must be the State and County where the document signer(s) personally appeared before the notary public for acknowledgment.
- Date of notarization must be the date that the signer(s) personally appeared which must also be the same date the acknowledgment is completed.
- The notary public must print his or her name as it appears within his or her commission followed by a comma and then your title (notary public).
- Print the name(s) of document signer(s) who personally appear at the time of notarization.
- Indicate the correct singular or plural forms by crossing off incorrect forms (i.e. ~~he/she/they,~~ is /~~are~~) or circling the correct forms. Failure to correctly indicate this information may lead to rejection of document recording.
- The notary seal impression must be clear and photographically reproducible. Impression must not cover text or lines. If seal impression smudges, re-seal if a sufficient area permits, otherwise complete a different acknowledgment form.
- Signature of the notary public must match the signature on file with the office of the county clerk.
  - Additional information is not required but could help to ensure this acknowledgment is not misused or attached to a different document.
  - Indicate title or type of attached document, number of pages and date.
  - Indicate the capacity claimed by the signer. If the claimed capacity is a corporate officer, indicate the title (i.e. CEO, CFO, Secretary).
- Securely attach this document to the signed document.

Attachment 1
List of Patents

No.	Patent No.	Issue Date	Filing Date	Description
1.	US 4835420	5/30/1989	11/17/1987	Method & Apparatus for Signal Level Conversion with Clamped Capacitive Bootstrap
2.	US 4876216	10/24/1989	3/7/1988	Semiconductor Integrated Circuit Mfg Process Providing Oxide-Filled Trench Isolation of Circuit Devices
3.	US 4874970	10/17/1989	5/11/1988	ECL Output with Darlington or Common Collector-Common Emitter Drive
4.	US 4845385	7/4/1989	6/21/1988	BICMOS Logic Circuits with Reduced Crowbard Current
5.	CA 1289630	9/24/1991	11/16/1988	Method & Apparatus for Coupling an ECL Output Signal Using a Clamped Capacitive Bootstrap Circuit
6.	US 4875003	10/17/1989	2/21/1989	Non-Contact I/O Signal PAD Scan Testing of VLSI Circuits
7.	US 4970414	11/13/1990	7/7/1989	TTL-Level-Output Interface Circuit
8.	US 5047711	9/10/1991	8/23/1989	Wafer-Level Burn-in Testing of Integrated Circuits
9.	US 5440523	8/8/1995	8/19/1993	Multiple-Port Shared Memory Interface and Associated Method
10.	AU 682211	2/5/1998	8/17/1994	Multiple-Port Shared Memory Interface and Associated Method
11.	CA 2168666	6/12/2001	8/17/1994	Multiple-Port Shared Memory Interface and Associated Method
12.	DE '0714534	7/28/1999	8/17/1994	Multiple-Port Shared Memory Interface and Associated Method
13.	FR 714534	7/28/1999	8/17/1994	Multiple-Port Shared Memory Interface and Associated Method
14.	GB 714534	7/28/1999	8/17/1994	Multiple-Port Shared Memory Interface and Associated Method
15.	JP 3241045	10/19/2001	8/17/1994	Multiple-Port Shared Memory Interface and Associated Method
16.	US 5732041	3/24/1998	8/7/1995	Multiple-Port Shared Memory Interface and Associated Method
17.	DE 0843854	12/10/2003	7/18/1996	Multiple-Port Shared Memory Interface and Associated Method
18.	EP 0843854	12/10/2003	7/18/1996	Multiple-Port Shared Memory Interface and Associated Method
19.	FR 0843854	12/10/2003	7/18/1996	Multiple-Port Shared Memory Interface and Associated Method
20.	GB 0843854	12/10/2003	7/18/1996	Multiple-Port Shared Memory Interface and Associated Method

Initials: 

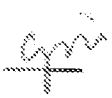
21.	JP 3628706	12/17/2004	7/18/1996	Multiple-Port Shared Memory Interface and Associated Method
22.	JP 3899085	1/5/2007	7/18/1996	Multiple-Port Shared Memory Interface and Associated Method
23.	KR 0356447	9/30/2002	7/18/1996	Multiple-Port Shared Memory Interface and Associated Method
24.	US 6170046	1/2/2001	10/28/1997	Accessing a Memory System via a Data or Address Bus that Provides Access to more than one Part
25.	US 5910928	6/8/1999	12/29/1997	Multiple-Port Shared Memory Interface and Associated Method
26.	US 5914621	6/22/1999	2/5/1998	Charge Balanced Ramp with Improved Signal Linearity
27.	US 5952949	9/14/1999	2/5/1998	Timer with Dynamic Reset Threshold
28.	US 5973522	10/26/1999	2/5/1998	Current Injected Ramp with Reduced Recovery Time
29.	US 5985924	9/21/1999	4/21/1998	Differential Metal-Oxide Semiconductor (MOS) Push-Pull Buffer
30.	US 6021086	2/1/2000	8/12/1998	Multiple-Port Shared Memory Interface and Associated Method
31.	US 6037841	3/14/2000	10/7/1998	Impedance Matched CMOS Trans-impedance Amplifier for High-Speed Fiber Optic Communications
32.	JP 3615948	11/12/2004	10/27/1998	Accessing a Memory System via a Data or Address Bus that Provides Access to more than one Part
33.	US 6198352	3/6/2001	11/20/1998	Radio Frequency Low Noise Amplifier Fabricated in Complementary Metal Oxide Semiconductor Technology
34.	US 6201443	3/13/2001	11/20/1998	Radio Frequency Variable Gain Amplifier Fabricated in Complementary Metal Oxide Semiconductor Technology
35.	US 6268777	7/31/2001	11/20/1998	Single Inductor Fully Integrated Differential Voltage Controlled Oscillator with Automatic Amplitude Adjustment and On-Chip Varactor
36.	US 6211721	4/3/2001	12/28/1998	Multiplexer with Short Propagation Delay and Low Power Consumption
37.	US 6272160	8/7/2001	2/3/1999	High Speed CMOS Driver for Vertical-Cavity Surface Emitting Lasers
38.	US 6512617	1/28/2003	2/3/1999	Methods and Systems for Control and Calibration of VCSEL-Based Optical Transceivers
39.	US 6300802	10/9/2001	2/19/1999	Output Buffer with Programmable Voltage Swing
40.	US 6198309	3/6/2001	3/31/1999	Emitter Follower Output with Programmable Current
41.	US 6169421	1/2/2001	5/3/1999	Complimentary Metal Oxide Semiconductor Buffer
42.	US 6493359	12/10/2002	5/4/1999	Reconfigurable Frame Counter
43.	US 6493847	12/10/2002	6/15/1999	Sonet B2 Parity Byte Calculation Method & Apparatus

Initials:

44.	US 6169007	1/2/2001	6/25/1999	Self-Aligned Non-Selective Thin-EPI-Base SIGE Heterojunction Bipolar Transistor BICMOS Process Using Side
45.	US 6222470	4/24/2001	9/23/1999	Voltage/Current Reference with Digitally Programmable Temperature Coefficient
46.	US 6205523	3/20/2001	10/7/1999	Accessing a Memory System via a Data or Address Bus that Provides Access to more than one Part
47.	US 6559020	5/6/2003	10/20/1999	Bipolar Device with Silicon Germanium (SIGE) Base Region
48.	US 6275114	8/14/2001	1/6/2000	Impedance Matched CMOS Transimpedance Amplifier for High-Speed Fiber Optic Communications
49.	US 6437376	8/20/2002	3/1/2000	Heterojunction Bipolar Transistor (HBT) with Three-Dimensional Base Contact
50.	US 6775799	8/10/2004	3/17/2000	Protocol Independent Performance with Selectable FEC Encoding and Decoding
51.	US 6782009	8/24/2004	3/17/2000	Multi-Port Data Arbitration Control
52.	US 6795451	9/21/2004	3/17/2000	Programmable Synchronization Structure with Auxiliary Data Link
53.	US 6892336	5/10/2005	3/17/2000	Gigabit Ethernet Performance Monitoring
54.	US 7035292	4/25/2006	3/17/2000	Transposable Frame Synchronization Structure
55.	US 6452267	9/17/2002	4/4/2000	Selective Flip Chip Underfill Processing for High Speed Signal Isolation
56.	US 6566851	5/20/2003	8/10/2000	Output Conductance Correction for High Compliance Short-Channel MOS Switched Current Minor
57.	US 6429085	8/6/2002	9/6/2000	Self-Aligned Non-Selective Thin-EPI-Base SIGE Heterojunction Bipolar Transistor BICMOS Process Using Side
58.	US 6437669	8/20/2002	9/29/2000	Microwave to Millimeter Wave Frequency Substrate Interface
59.	US 6469383	10/22/2002	11/8/2000	Temperature Stable CMOS Device
60.	US 6466081	10/15/2002	11/8/2000	Temperature Stable CMOS Device
61.	US 6684351	1/27/2004	12/22/2000	System and Method for Diagnosing Errors in Multidimensional Digital Frame Structure Communications
62.	US 7002996	2/21/2006	4/9/2001	System and Method for Switch Timing Synchronization
63.	US 6574861	6/10/2003	4/11/2001	System and Method for Solder Ball Rework
64.	US 6879596	4/12/2005	4/11/2001	System and Method for Systolic Array Sorting of Information Segments
65.	US 7016344	3/21/2006	4/17/2001	Time Slot Interchanging of Time Slots from Multiple Sonet Signals without First Passing the Signals through Pointer Processors to Synchronize them to a Common Clock
66.	US 6502231	12/31/2002	5/31/2001	Integrated Circuit Template Cell System & Method

Initials:

67.	US 6389050	5/14/2002	6/11/2001	High Speed CMOS Driver for Vertical-Cavity Surface Emitting Lasers
68.	US 6617943	9/9/2003	7/27/2001	Package Substrate Interconnect Layout for Providing Bandpass/Lowpass Filtering
69.	US 6476736	11/5/2002	8/27/2001	Single Interconnect, Multi-bit Interface
70.	US 6514783	2/4/2003	9/17/2001	Flip-Chip Transition Interface Structure
71.	US 6639322	10/28/2003	9/17/2001	Flip-Chip Transition Interface Structure
72.	US 6570414	5/27/2003	9/27/2001	Methods & Apparatus for Reducing the Crowbar Current in a Driver Circuit
73.	US 6683489	1/27/2004	9/27/2001	Methods & Apparatus for Generating a Supply-Independent and Temperature-Stable Bias Current
74.	US 7079545	7/18/2006	12/17/2001	System and Method for Simultaneous Deficit Round Robin Prioritization
75.	US 6993700	1/31/2006	12/21/2001	System and Method for Generating FEC Based Alarms
76.	US 7020131	3/28/2006	12/24/2001	System and Method for Hierarchical Switching
77.	US 6665367	12/16/2003	12/27/2001	Embedded Frequency Counter with Flexible Configuration
78.	US 6531369	3/11/2003	2/14/2002	Heterojunction Bipolar Transistor (HBT) Fabrication Using a Selectively Deposited Silicon Germanium (SIGE)
79.	US 6912667	6/28/2005	3/8/2002	System and Method for Communicating Fault Type and Fault Location Messages
80.	US 7072361	7/4/2006	3/8/2002	System and Method for the Transport of Backwards Information between Simplex Devices
81.	US 6797891	9/28/2004	3/26/2002	Flexible Interconnect Cable with High Frequency Electrical Transmission Line
82.	US 6867668	3/15/2005	3/26/2002	High Frequency Signal Transmission from the Surface of a Circuit Substrate to a Flexible Interconnect Cable
83.	US 7073001	7/4/2006	4/3/2002	Fault-Tolerant Digital Communications Channel having Synchronized Unidirectional Links
84.	US 6744293	6/1/2004	4/9/2002	Global Clock tree De-Skew
85.	US 7130367	10/31/2006	4/9/2002	Digital Delay Lock Loop for Setup and Hold Time Enhancement
86.	US 6642556	11/4/2003	4/22/2002	Modular Macro Cell Layout Method
87.	US 6566761	5/20/2003	5/3/2002	Electronic Device Package with High Speed Signal Interconnect between Die Pad and External Substrate Pad
88.	US 6812576	11/2/2004	5/14/2002	Fanned Out Interconnect via Structure for Electronic Package Substrates
89.	US 6774742	8/10/2004	5/23/2002	System and Method for Interfacing a Coaxial Connector to a Coplanar Waveguide Substrate
90.	US 7028241	4/11/2006	6/13/2002	Optical Transport Network Frame Structure with Dynamically Allocatable In-band Data Channel and Forward Error Correction Byte Capacity

Initials: 

91.	US 7278081	10/2/2007	6/13/2002	Optical Transport Network Frame Structure with In-Band Data Channel and Forward Error Correction
92.	US 6713853	3/30/2004	7/23/2002	Electronic Package with Offset Reference Plane Cutout
93.	US 6775635	8/10/2004	8/12/2002	System and Method for Measuring Amplifier Gain in a Digital Network
94.	US 6801090	10/5/2004	8/13/2002	High Performance Differential Amplifier
95.	US 6862705	3/1/2005	8/21/2002	System and Method for Testing High Pin Count Electronic Devices Using a Test Board with Limited Test Channels
96.	US 6686797	2/3/2004	9/9/2002	Temperature Stable CMOS Devices
97.	US 6762494	7/13/2004	9/24/2002	Electronic Package Substrate with an Upper Dielectric Layer Covering High Speed Signal Traces
98.	US 6690207	2/10/2004	9/25/2002	Power Efficient Emitter-Coupled Logic Circuit
99.	US 6825964	11/30/2004	10/22/2002	Device for Coupling Drive Circuitry to Electroabsorption Modulator
100.	US 6725443	4/20/2004	10/24/2002	Integrated Circuit Template Cell System & Method
101.	US 6720818	4/13/2004	11/8/2002	Method & Apparatus for Maximizing an Amplitude of an Output Signal of a Differential Multiplexer
102.	US 6731161	5/4/2004	11/15/2002	Method for Measuring the Frequency of a Transimpedance Amplifier Packaged with an Integrated Limiter
103.	US 6798263	9/28/2004	11/25/2002	Reset Feature for a Low Voltage Differential Latch
104.	US 6949817	9/27/2005	12/3/2002	Stackable Test Apparatus for Protecting Integrated Circuit Packages during Testing
105.	US 7327672	2/5/2008	1/31/2003	Signal Routing in a Node of 1:N Automatic Protection Switching Network
106.	US 7352694	4/1/2008	2/24/2003	System and Method for Tolerating Data Link Faults in a Packet Communications Switch Fabric
107.	US 7209453	4/24/2007	3/3/2003	System and Method for Tolerating Control Link Faults in a Packet Communications Switch Fabric
108.	US 7221652	5/22/2007	3/3/2003	System and Method for Tolerating Data Link Faults in Communications with a Switch Fabric
109.	US 7230947	6/12/2007	3/3/2003	Minimum Latency Cut-Through Switch Fabric
110.	US 7298739	11/20/2007	3/3/2003	System and Method for Communicating Switch Fabric Control Information
111.	US 6897700	5/24/2005	3/21/2003	Amplifier with Digital DC Offset Cancellation Feature
112.	US 7308023	12/11/2007	3/21/2003	Dual Function Clock Signal Suitable for Host Control of Synchronous and Asynchronous Target Devices
113.	US 7263066	8/28/2007	3/24/2003	Switch Fabric Backplane Flow Management using Credit-Based Flow Control

Initials:

114.	US 7304987	12/4/2007	3/24/2003	System and Method for Synchronizing Switch Fabric Backplane Link Management Credit Counters
115.	US 6770554	8/3/2004	3/27/2003	On-Chip Interconnect Circuits with use of Large-Sized Cooper Fill in CMP Process
116.	US 7212523	5/1/2007	3/27/2003	Pipeline Architecture for the Design of Single-Stage Cross-Connect System
117.	US 7304988	12/4/2007	3/28/2003	A Technique for Building Large Single-Stage Cross-Connect Using Multiple Devices without Interleaving
118.	US 6879608	4/12/2005	3/31/2003	High Compliance Laser Driver
119.	US 7242686	7/10/2007	3/31/2003	System and Method for Communicating TDM Traffic Through a Packet Switch Fabric
120.	US 7298754	11/20/2007	3/31/2003	Configurable Switch Fabric Interface Bandwidth System and Method
121.	US 7298756	11/20/2007	3/31/2003	System and Method for Programming Cell Packet Headers
122.	US 6774721	8/10/2004	4/4/2003	High Speed Logic Circuits
123.	US 7225274	5/29/2007	5/23/2003	Method and Apparatus for Transferring Data Across a Protocol Bridge
124.	US 7239645	7/3/2007	9/9/2003	Method and Apparatus for Managing Payload Buffer Segments in a Networking Device
125.	US 7260112	8/21/2007	9/9/2003	Method and Apparatus for Terminating and Bridging Network Protocols
126.	US 6836350	12/28/2004	3/5/2004	Device for Coupling Drive Circuitry to Electroabsorption Modulator
127.	US 7145411	12/5/2006	9/27/2004	Flexible Interconnect Cable with High Frequency Electrical Transmission Line
128.	US 7132861	11/7/2006	6/20/2005	Amplifier with Digital DC Offset Cancellation Feature
129.	US 7336139	2/26/2008	10/27/2006	Flexible Interconnect Cable with High Frequency Electrical Transmission Line
130.	US 7382788		05/08/2003	Method and apparatus for implementing a data frame processing model
131.	US 7352694		02/24/2003	System and Method for Tolerating Data Link Faults in a Packet Communications Switch Fabric
132.	US 4926065			Method and Apparatus for Coupling an ECL output signal using a clamped capacity bootstrap circuit
133.	US 7327672			Signal routing in a node of a 1:N Automatic protection switching network
134.	US 7376149		06/21/2007	Method and Apparatus for Bridging Network Protocols

Initials: _____

Attachment 2
List of Patent Applications

No.	Publication No.	Description	Application Date
1.	US 20050198236	System and method for performing driver configuration operations without a system reboot	January 30, 2004
2.	US 10/291156	Stress reduction for electronic package connections	November 8, 2002
3.	US 10/404573	Detection Circuit and Method for AC coupled circuitry	March 31, 2003
4.	US 11/652921	System and method for selectively etching an integrated circuit	
5.	US 20050102419	Extended link monitoring channel for 10 Gb/s Ethernet	November 6, 2003
6.	US 10/029581	System and method for granting arbitrated bids in the switching of information	December 20, 2001
7.	US 10/400380	Method for Automatically Generating Code to Define a System of Hardware Elements	March 26, 2003
8.	US 10/401474	Synchronous rate adapter	March 28, 2003
9.	US 11/519549	Serial-to-Parallel Transceiver with Programmable Parallel Data Path Width	
10.	US 12/049222 (Divisional)	Method and Apparatus for Bridging Network Protocols	March 14, 2008
11.	US 12/009,740	Flexible Interconnect Cable for an Electronic Assembly	January 22, 2008
12.	US 12/102,415	System and Method for Reevaluating Granted Arbitrated Bids	April 14, 2008
13.	US 12/103,683	Method for Defining the Physical Configuration of a Communication System	April 15, 2008
14.	US 12/105,218	Data Link Fault Tolerance	April 17, 2008
15.	US 12/106,125	Data Frame Processing	April 18, 2008
16.	US 12/107,721	Driver Configuration	April 22, 2008
17.	US 12/110,156	Ethernet Link Monitoring Channel	April 25, 2008

Initials: _____