

PATENT ASSIGNMENT

Electronic Version v1.1

Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY AGREEMENT
CONVEYING PARTY DATA	
Name	Execution Date
DFT Microsystems, Inc.	01/29/2009
RECEIVING PARTY DATA	
Name:	Advantest Corporation
Street Address:	336-1 Ohwa Meiwa-machi, Ora-gun
City:	Gunma
State/Country:	JAPAN
Postal Code:	370-0718
PROPERTY NUMBERS Total: 5	
Property Type	Number
Patent Number:	7242209
Patent Number:	7315574
Application Number:	11776865
Application Number:	11776825
Application Number:	12028577
CORRESPONDENCE DATA	
Fax Number:	(415)276-7010
<i>Correspondence will be sent via US Mail when the fax attempt is unsuccessful.</i>	
Phone:	4152687000
Email:	tdinh@mofo.com
Correspondent Name:	Tuan H. Dinh
Address Line 1:	Morrison & Foerster LLP
Address Line 2:	425 Market Street
Address Line 4:	San Francisco, CALIFORNIA 94105
ATTORNEY DOCKET NUMBER:	33377-85
NAME OF SUBMITTER:	Tuan H. Dinh

PATENT

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REEL: 022191 FRAME: 0078

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Total Attachments: 4

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PATENT SECURITY AGREEMENT

THIS PATENT SECURITY AGREEMENT, dated as of January 29, 2009 (this "Agreement"), is made between DFT Microsystems, Inc., a Delaware corporation ("Debtor"), and Advantest Corporation, a Japanese Corporation ("Secured Party").

Debtor and Secured Party hereby agree as follows:

SECTION 1 Definitions; Interpretation.

(a) As used in this Agreement, the following terms shall have the following meanings:

"Development Agreement" means that certain Development and License Agreement, dated as of December 24, 2008, between Debtor and Secured Party.

"Documents" means this Agreement, the Development Agreement, the Purchase Agreement, the Escrow Agreement and all other certificates, documents, agreements and instruments delivered to Secured Party in connection therewith.

"Escrow Agreement" means that certain Preferred Escrow Agreement, effective December 1, 2008, among DSI Technology Escrow Services, Inc., Debtor and Secured Party.

"Obligations" means the indebtedness, liabilities and other obligations of Debtor to Secured Party under or in connection with this Agreement and the other Documents.

"Purchase Agreement" means that certain Purchase Agreement, dated as of December 24, 2008, between Debtor and Secured Party.

SECTION 2 Security Interest.

Debtor hereby grants to Secured Party a security interest in all of Debtor's right, title and interest in, to and under all of the following, wherever located and whether now existing or owned or hereafter acquired or arising (collectively, the "Collateral"):

(i) all patents and patent applications, domestic or foreign, all licenses relating to any of the foregoing and all income and royalties with respect to any licenses (including such patents and patent applications as described in Schedule 1), all rights to sue for past, present or future infringement thereof, all rights arising therefrom and pertaining thereto and all reissues, divisions, continuations, renewals, extensions and continuations-in-part thereof;

(ii) all of the Debtor's present and future United States registered copyrights and copyright registrations, including the Debtor's United States registered copyrights and copyright registrations listed in Schedule 1 to this Agreement, all of the Debtor's present and future United States applications for copyright registrations, including the Debtor's United States applications for copyright registrations listed in Schedule 1 to this Agreement, and all of the Debtor's present and future copyrights which are not registered in the United States Copyright Office (collectively, the "Copyrights"), and any and all royalties, payments, and other amounts payable to the Debtor

in connection with the Copyrights, together with all renewals and extensions of the Copyrights, the right to recover for all past, present, and future infringements of the Copyrights, and all computer programs, computer databases, computer program flow diagrams, source codes, object codes and all tangible property embodying or incorporating the Copyrights, and all other rights of every kind whatsoever accruing thereunder or pertaining thereto;

(iii) the entire goodwill of or associated with the businesses now or hereafter conducted by the Debtor connected with and symbolized by any of the aforementioned properties and assets;

(iv) all commercial tort claims associated with or arising out of any of the aforementioned properties and assets;

(v) all accounts, all intangible intellectual or other similar property and other general intangibles associated with or arising out of any of the aforementioned properties and assets and not otherwise described above, including all license payments and payments under insurance (whether or not the Secured Party is the loss payee thereof) or any indemnity, warranty or guaranty payable by reason of loss or damage to or otherwise with respect to the foregoing Collateral; and

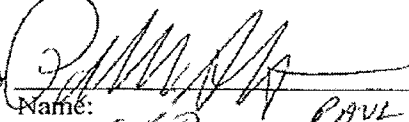
(vi) all products, proceeds and supporting obligations of or with respect to any and all of the foregoing Collateral.

SECTION 3 Supplement to Security Agreement. This Agreement has been granted in conjunction with the security interests granted to Secured Party under the Intellectual Property Security Agreement, dated the date hereof, between Debtor and Secured Party. The rights and remedies of Secured Party with respect to the security interests granted herein are without prejudice to, and are in addition to those set forth in the Security Agreement, all terms and provisions of which are incorporated herein by reference.


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IN WITNESS WHEREOF, the parties hereto have duly executed this Agreement, as of the date first above written.

DFT MICROSYSTEMS, INC.

By 
Name: PAUL SAKAMOTO
Title: CEO

ADVANTEST CORPORATION

By 
Name: Shinichiro Kuroe
Title: Senior Vice President
SoC Tester Business Group

SCHEDULE 1
to the Intellectual Property Security Agreement

1. Patents and Patent Applications.

Patents:

Patent Number	Jurisdiction	Description	Filing Date	Status
7,242,209	U.S.	System and method for testing integrated circuits	05/03/2004	Issued 7/10/2007
TW 0286609	Taiwan	System and method for testing integrated circuits	05/02/2005	Issued 9/11/2007
7,315,574	U.S.	System and method for generating a jittered test signal	04/26/2005	Issued 1/1/2008

Patent Applications:

Application No.	Jurisdiction	Description	Filing Date	Status
2564297	Canada	System and method for testing integrated circuits	05/02/2005	Pending
05744211.3 (EP 1747617)	EP	System and method for generating a jittered test signal	05/02/2005	Pending
2564351	Canada	System and method for generating a jittered test signal	05/02/2005	Pending
200580021086 (CN 1985459)	China	System and method for generating a jittered test signal	05/02/2005	Pending
11/776,865 (US2008/0013456)	U.S.	High-speed signal testing system having oscilloscope functionality	07/12/2007	Pending
11/776,825 (US2008/0048726)	U.S.	Signal integrity measurement systems and methods using a predominantly digital time-base generator	07/12/2007	Pending
12/028,577 (US2008/0192814)	U.S.	System and method for physical-layer testing of high-speed serial links in their mission environments	02/08/2008	Pending

2. Copyrights (Registered and Unregistered) and Copyright Applications.