

PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY AGREEMENT
CONVEYING PARTY DATA	
Name	Execution Date
ATRENTA INC.	04/14/2009
RECEIVING PARTY DATA	
Name:	SILICON VALLEY BANK
Street Address:	2400 HANOVER STREET
City:	PALO ALTO
State/Country:	CALIFORNIA
Postal Code:	94304
PROPERTY NUMBERS Total: 20	
Property Type	Number
Application Number:	11276819
Patent Number:	7451427
Patent Number:	7349835
Patent Number:	7277840
Patent Number:	7216321
Patent Number:	7152216
Patent Number:	7076748
Patent Number:	7073146
Patent Number:	6993733
Patent Number:	6876934
Application Number:	11959427
Application Number:	11837174
Application Number:	11755764
Application Number:	11749090
Application Number:	11692949

OP \$800.00 11276819

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PATENT
REEL: 022542 FRAME: 0570

Application Number:	11676232
Application Number:	11426936
Application Number:	11419624
Application Number:	11260225
Application Number:	10906571

CORRESPONDENCE DATA

Fax Number: (404)962-6736

Correspondence will be sent via US Mail when the fax attempt is unsuccessful.

Phone: (404) 885-3038

Email: michael.brignati@troutmansanders.com

Correspondent Name: MICHAEL J. BRIGNATI, PH.D.

Address Line 1: TROUTMAN SANDERS LLP

Address Line 2: 600 PEACHTREE STREET, N.E.

Address Line 4: ATLANTA, GEORGIA 30308-2216

ATTORNEY DOCKET NUMBER:	220763.001046
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NAME OF SUBMITTER:	Michael J. Brignati, Ph.D.
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Total Attachments: 9

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INTELLECTUAL PROPERTY SECURITY AGREEMENT

THIS INTELLECTUAL PROPERTY SECURITY AGREEMENT is entered into as of April 14, 2009 (the "**Effective Date**") by and between SILICON VALLEY BANK ("**Bank**") and ATRENTA INC. ("**Grantor**").

RECITALS

A. Bank has agreed to make certain advances of money and to extend certain financial accommodation to Grantor (the "**Loans**") in the amounts and manner set forth in that certain Loan and Security Agreement by and between Bank and Grantor dated the Effective Date (as the same may be amended, modified or supplemented from time to time, the "**Loan Agreement**"; capitalized terms used herein are used as defined in the Loan Agreement). Bank is willing to make the Loans to Grantor, but only upon the condition, among others, that Grantor shall grant to Bank a security interest in certain Copyrights, Trademarks, Patents, and Mask Works (as each term is described below) to secure the obligations of Grantor under the Loan Agreement.

B. Pursuant to the terms of the Loan Agreement, Grantor has granted to Bank a security interest in all of Grantor's right, title and interest, whether presently existing or hereafter acquired, in, to and under all of the Collateral.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of its obligations under the Loan Agreement, Grantor hereby represents, warrants, covenants and agrees as follows:

AGREEMENT

To secure its obligations under the Loan Agreement, Grantor grants and pledges to Bank a security interest in all of Grantor's right, title and interest in, to and under its intellectual property (all of which shall collectively be called the "**Intellectual Property Collateral**"), including, without limitation, the following:

(a) Any and all copyright rights, copyright applications, copyright registrations and like protections in each work or authorship and derivative work thereof, whether published or unpublished and whether or not the same also constitutes a trade secret, now or hereafter existing, created, acquired or held, including without limitation those set forth on Exhibit A attached hereto (collectively, the "**Copyrights**");

(b) Any and all trade secrets, and any and all intellectual property rights in computer software and computer software products now or hereafter existing, created, acquired or held;

(c) Any and all design rights that may be available to Grantor now or hereafter existing, created, acquired or held;

(d) All patents, patent applications and like protections including, without limitation, improvements, divisions, continuations, renewals, reissues, extensions and continuations-in-part of the same, including without limitation the patents and patent applications set forth on Exhibit B attached hereto (collectively, the “**Patents**”);

(e) Any trademark and servicemark rights, whether registered or not, applications to register and registrations of the same and like protections, and the entire goodwill of the business of Grantor connected with and symbolized by such trademarks, including without limitation those set forth on Exhibit C attached hereto (collectively, the “**Trademarks**”);

(f) All mask works or similar rights available for the protection of semiconductor chips, now owned or hereafter acquired, including, without limitation those set forth on Exhibit D attached hereto (collectively, the “**Mask Works**”);

(g) Any and all claims for damages by way of past, present and future infringements of any of the rights included above, with the right, but not the obligation, to sue for and collect such damages for said use or infringement of the intellectual property rights identified above;

(h) All licenses or other rights to use any of the Copyrights, Patents, Trademarks, or Mask Works and all license fees and royalties arising from such use to the extent permitted by such license or rights;

(i) All amendments, extensions, renewals and extensions of any of the Copyrights, Trademarks, Patents, or Mask Works; and

(j) All proceeds and products of the foregoing, including without limitation all payments under insurance or any indemnity or warranty payable in respect of any of the foregoing.

This security interest is granted in conjunction with the security interest granted to Bank under the Loan Agreement. The rights and remedies of Bank with respect to the security interest granted hereby are in addition to those set forth in the Loan Agreement and the other Loan Documents, and those which are now or hereafter available to Bank as a matter of law or equity. Each right, power and remedy of Bank provided for herein or in the Loan Agreement or any of the Loan Documents, or now or hereafter existing at law or in equity shall be cumulative and concurrent and shall be in addition to every right, power or remedy provided for herein and the exercise by Bank of any one or more of the rights, powers or remedies provided for in this Intellectual Property Security Agreement, the Loan Agreement or any of the other Loan Documents, or now or hereafter existing at law or in equity, shall not preclude the simultaneous or later exercise by any person, including Bank, of any or all other rights, powers or remedies.

Bank will release the security interest granted pursuant to this Agreement at the Borrower's expense, at the time all of the Borrower's Obligations to the Bank are paid in full and Bank has no further commitment to make any further Credit Extensions to Borrower.

[Signature Page Follows.]

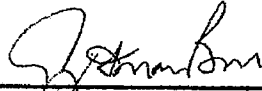
IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

Address of Grantor:

ATRENTA INC.

2077 Gateway Drive, Suite 300
San Jose, California 95110
Attn: Ajoy K. Bose

By: 
Name: Ajoy K. Bose
Title: Chairman, President & CEO

BANK:

Address of Bank:

SILICON VALLEY BANK

2400 Hanover Street
Palo Alto, California 94304
Attn: Eric C. Johnson

By: _____
Name: _____
Title: _____

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

Address of Grantor:

ATRENTA INC.

2077 Gateway Drive, Suite 300

San Jose, California 95110

Attn: _____

By: _____

Name:

Title:

BANK:

Address of Bank:

SILICON VALLEY BANK

2400 Hanover Street

Palo Alto, California 94304

Attn: Eric C. Johnson

By: 

Name: Joseph S Restrepo

Title: SRM

(Signature Page to Intellectual Property Security Agreement)

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EXHIBIT A

Copyrights

Description

Registration/
Application
Number

Registration/
Application
Date

None

EXHIBIT B

Patents

<u>Title</u>	<u>Patent/Patent Application Number (Publication Number)</u>	<u>Issue/Filing Date</u>
Method for clock synchronization validation in integrated circuit design	7,506,292	03/17/2009
Bus representation for efficient physical synthesis of integrated circuit designs	7,451,427	11/11/2008
Method, system and computer program product for generating and verifying isolation logic modules in design of integrated circuits	7,349,835	03/25/2008
Method for detecting bus contention from RTL description	7,277,840	10/02/2007
Pattern recognition in an integrated circuit design	7,216,321	05/08/2007
Method, system, and computer program product for automatic insertion and correctness verification of level shifters in integrated circuits with multiple voltage domains	7,152,216	12/19/2006
Identification and implementation of clock gating in the design of integrated circuits	7,076,748	07/11/2006
Method for clock synchronization validation in integrated circuit design	7,073,146	07/04/2006
Apparatus and method for handling of multi-level circuit design data	6,993,733	01/31/2006
Method for determining fault coverage from RTL description	6,876,934	04/05/2005
METHOD, SYSTEM, AND COMPUTER PROGRAM PRODUCT FOR GENERATING AND VERIFYING ISOLATION LOGIC MODULES IN DESIGN OF INTEGRATED CIRCUITS	11/959,427	12/18/2007

METHOD FOR COMPUTING POWER SAVINGS AND DETERMINING THE PREFERRED CLOCK GATING CIRCUIT OF AN INTEGRATED CIRCUIT DESIGN	11/837,174	08/10/2007
METHOD FOR CHECKING CONSTRAINTS EQUIVALENCE OF AN INTEGRATED CIRCUIT DESIGN	11/755,764	05/31/2007
METHOD FOR MODELING AND VERIFYING TIMING EXCEPTIONS	11/749,090	05/15/2007
METHOD FOR ACCELERATING THE GENERATION OF AN OPTIMIZED GATE-LEVEL REPRESENTATION FROM A RTL REPRESENTATION	11/692,949	03/29/2007
METHOD FOR GENERATING TIMING EXCEPTIONS	11/676,232	02/16/2007
METHOD FOR RECOGNIZING AND VERIFYING FIFO STRUCTURES IN INTEGRATED CIRCUIT DESIGNS	11/426,936	06/27/2006
A METHOD OF OPTIMIZATION OF CLOCK GATING IN INTEGRATED CIRCUIT DESIGNS	11/419,624	05/22/2006
Chip development system enabled for the handling of multi-level circuit design data	11/260,225	10/28/2005
A Method for Automatic Recognition of Handshake Data Exchange at Clock- Domain Crossing in Integrated Circuit Design	10/906,571	02/24/2005

EXHIBIT C

Trademarks

<u>Description</u>	<u>Registration/ Application Number</u>	<u>Registration/ Application Date</u>
EARLY DESIGN CLOSURE (Registered)	3,304,662	10/02/2007
ATRENTA (Registered)	3,230,964	04/17/2007
1TEAM:EMBEDDED (Registered)	3,256,970	06/26/2007
1TEAM (Registered)	3,230,954	04/17/2007
1TEAM:IMPLEMENT (Registered)	3,160,627	10/17/2006
PERISCOPE (Registered)	3,046,985	01/17/2006
ATRENTA THE PREDICTIVE ANALYSIS COMPANY (Registered)	2,799,296	12/23/2003
SPYGLASS PREDICTIVE ANALYZER (Registered)	2,778,737	10/28/2003
ATRENTA (Registered)	2,762,455	09/09/2003
SPYGLASS(Registered)	2,603,761	08/06/2002
1TEAM:ANALYZE SPYGLASS (Abandoned)	78/726,104	10/04/2005
1TEAM:SPYGLASS (Abandoned)	78/726,061	10/04/2005
FUTURE PERFECT (Suspended)	78/579,382	03/03/2005
1TEAM:VERIFY (Abandoned)	78/572,545	02/22/2005
1TEAM:ANALYZE (Abandoned)	78/572,528	02/22/2005
BLUEPRINT (Abandoned)	78/394,711	04/01/2004
ACTIVESPEC (Abandoned)	78/168,426	09/26/2002

EXHIBIT D

Mask Works

Description

Registration/
Application
Number

Registration/
Application
Date

None

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