

PATENT ASSIGNMENT

Electronic Version v1.1

Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE BY SECURED PARTY
CONVEYING PARTY DATA	
Name	Execution Date
COMERICA BANK	04/15/2009
RECEIVING PARTY DATA	
Name:	ATRENTA, INC.
Street Address:	2077 Gateway Place
Internal Address:	Suite 300
City:	San Jose
State/Country:	CALIFORNIA
Postal Code:	95110
PROPERTY NUMBERS Total: 6	
Property Type	Number
Patent Number:	6993733
Patent Number:	7277840
Patent Number:	6876934
Patent Number:	7076748
Patent Number:	7073146
Patent Number:	7216321
CORRESPONDENCE DATA	
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PATENT
REEL: 022552 FRAME: 0216

ATTORNEY DOCKET NUMBER:	036703-1181 ATRENTA
NAME OF SUBMITTER:	Erin O'Brien
Total Attachments: 2 source=Atrenta Pat release#page1.tif source=Atrenta Pat release#page2.tif	

REASSIGNMENT AND RELEASE OF SECURITY INTEREST

This Reassignment and Release of Security Interest is made as of the 15th day of April 2009 Comerica Bank ("LENDER") in favor of Atrenta, Inc. ("COMPANY") a Delaware Corporation with its principal place of business at 2077 Gateway Place, Suite 300, San Jose, CA 95110

Recital

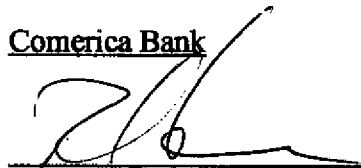
WHEREAS, COMPANY assigned certain interests in the Patents described on Exhibit A (the Patents) and to LENDER under a Intellectual Property Security Agreement dated May 25, 2006, and recorded with the U.S. Patent and Trademark Office on August 8, 2006 at Reel 018073 Frame 0119, and

WHEREAS, COMPANY has satisfied all its obligations to LENDER in the Intellectual Property Security Agreement and LENDER wishes to reassign all interest that LENDER may have in the Patents

Agreement

Now Therefore, LENDER agrees that it releases its security interest in the Patents and reassigns to COMPANY, without warranty or recourse, all interest of LENDER in the Patents.

Comerica Bank



Robert L Hernandez
VP - Western Division
75 E. Trimble Road
San Jose, CA 95131

EXHIBIT "A"

- 1 **Patent #:** 6993733 **Issue Dt:** 01/31/2006 **Application #:** 10118242 **Filing Dt:** 04/09/2002
 Publication #: US20030192023 **Pub Dt:** 10/09/2003
 Title: APPARATUS AND METHOD FOR HANDLING OF MULTI-LEVEL CIRCUIT DESIGN DATA
- 2 **Patent #:** 7277840 **Issue Dt:** 10/02/2007 **Application #:** 10172996 **Filing Dt:** 06/18/2002
 Publication #: US20030233504 **Pub Dt:** 12/18/2003
 Title: METHOD FOR DETECTING BUS CONTENTION FROM RTL DESCRIPTION
- 3 **Patent #:** 6876934 **Issue Dt:** 04/05/2005 **Application #:** 10217535 **Filing Dt:** 08/14/2002
 Publication #: US20040034495 **Pub Dt:** 02/19/2004
 Title: METHOD FOR DETERMINING FAULT COVERAGE FROM RTL DESCRIPTION
- 4 **Patent #:** 7076748 **Issue Dt:** 07/11/2006 **Application #:** 10631755 **Filing Dt:** 08/01/2003
 Publication #: US20050028118 **Pub Dt:** 02/03/2005
 Title: IDENTIFICATION AND IMPLEMENTATION OF CLOCK GATING IN THE DESIGN OF INTEGRATED CIRCUITS
- 5 **Patent #:** 7073146 **Issue Dt:** 07/04/2006 **Application #:** 10695803 **Filing Dt:** 10/30/2003
 Publication #: US20050097484 **Pub Dt:** 05/05/2005
 Title: METHOD FOR CLOCK SYNCHRONIZATION VALIDATION IN INTEGRATED CIRCUIT DESIGN
- 6 **Patent #:** 7216321 **Issue Dt:** 05/08/2007 **Application #:** 10783091 **Filing Dt:** 02/23/2004
 Publication #: US20050108675 **Pub Dt:** 05/19/2005
 Title: PATTERN RECOGNITION IN AN INTEGRATED CIRCUIT DESIGN