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PATENT ASSIGNMENT

Electronic Version v1.1 Stylesheet Version v1.1

SUBMISSION TYPE: NEW ASSIGNMENT

NATURE OF CONVEYANCE: RELEASE BY SECURED PARTY

CONVEYING PARTY DATA

Name	Execution Date
HERCULES TECHNOLOGY GROWTH CAPITAL, INC.	04/14/2009

RECEIVING PARTY DATA

Name:	ATRENTA INC.
Street Address:	2077 GATEWAY DRIVE
Internal Address:	SUITE 300
City:	SAN JOSE
State/Country:	CALIFORNIA
Postal Code:	95110

PROPERTY NUMBERS Total: 17

Property Type	Number
Patent Number:	7451427
Patent Number:	7349835
Patent Number:	7277840
Patent Number:	7216321
Patent Number:	7152216
Patent Number:	7076748
Patent Number:	7073146
Patent Number:	6993733
Patent Number:	6876934
Application Number:	11837174
Application Number:	11755764
Application Number:	11749090
Application Number:	11692949
Application Number:	11676232

Application Number:	11426936	
Application Number:	11419624	
Application Number:	10906571	

CORRESPONDENCE DATA

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Correspondence will be sent via US Mail when the fax attempt is unsuccessful.

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Address Line 4: ATLANTA, GEORGIA 30308-2216

ATTORNEY DOCKET NUMBER:	220763.001046
NAME OF SUBMITTER:	Michael J. Brignati, Ph.D.

Total Attachments: 5

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RELEASE OF SECURITY INTEREST IN INTELLECTUAL PROPERTY

THIS RELEASE OF SECURITY INTEREST IN INTELLECTUAL PROPERTY (the "Release") is made as of the 14 day of April 2009, between ATRENTA, INC., a Delaware corporation ("Assignee") and HERCULES TECHNOLOGY GROWTH CAPITAL, INC. (the "Assignor").

WHEREAS, in connection with certain loan documents, Assignee and Assignor entered into certain loan and security agreements (as amended, supplemented, or otherwise modified from time to time, the "Agreements") for the purpose of securing certain obligations of Assignee to Assignor;

WHEREAS, pursuant to the Agreements, Assignee granted the Assignor, for the benefit of the Assignor, a security interest in all of the Patents, Trademarks, and Copyrights (as defined in the Agreements) (collectively hereinafter the "Intellectual Property"), including the Copyrights, Patents and Trademarks, identified on Exhibits A. B. and C. attached hereto, and pledged and mortgaged (but did not transfer title to) the Intellectual Property to Assignor; and

WHEREAS, all of the indebtedness and other obligations secured by the Assignor's security interest in the Intellectual Property have been repaid in their entirety, and the Assignor is therefore obligated to release its security interest in the Intellectual Property.

NOW, THEREFORE, for valuable consideration and pursuant to the terms and conditions set forth in the Agreements:

The Assignor hereby terminates and releases its security interest in the Intellectual Property, including without limitation, the Copyrights, Patents and Trademarks identified on Exhibits A, B, and \underline{C} attached hereto

Assignor hereby agrees to execute such further instruments and documents and perform such further acts as Assignee may deem necessary to secure to Assignee the rights herein conveyed.

IN WITNESS WHEREOF, the Assignor has caused this Release to be executed as of the day and year first above written.

HERCULES TECHNOLOGY GROWTH CAPITAL, INC.

Dy.

Title:

Tyson01 391314v1 220763,001046

EXHIBIT A - COPYRIGHTS

Description

Registration/ Application Number Registration/ Application Date



N/A

N/A

EXHIBIT B - PATENTS

<u>Title</u>	Patent/Patent Application Number	Issue/Filing Date
BUS REPRESENTATION FOR EFFICIENT PHYSICAL SYNTHESIS OF INTEGRATED CIRCUIT DESIGNS	7,451,427	11/11/2008
METHOD, SYSTEM AND COMPUTER PROGRAM PRODUCT FOR GENERATING AND VERIFYING ISOLATION LOGIC MODULES IN DESIGN OF INTEGRATED CIRCUITS	7,349,835	03/25/2008
METHOD FOR DETECTING BUS CONTENTION FROM RTL DESCRIPTION	7,277,840	10/02/2007
PATTERN RECOGNITION IN AN INTEGRATED CIRCUIT DESIGN	. 7,216,321	05/08/2007
METHOD, SYSTEM, AND COMPUTER PROGRAM PRODUCT FOR AUTOMATIC INSERTION AND CORRECTNESS VERIFICATION OF LEVEL SHIFTERS IN INTEGRATED CIRCUITS WITH MULTIPLE VOLTAGE DOMAINS	7,152,216	12/19/2006
IDENTIFICATION AND IMPLEMENTATION OF CLOCK GATING IN THE DESIGN OF INTEGRATED CIRCUITS	7,076,748	07/11/2006
METHOD FOR CLOCK SYNCHRONIZATION VALIDATION IN INTEGRATED CIRCUIT DESIGN	7,073,146	07/04/2006
APPARATUS AND METHOD FOR HANDLING OF MULTI-LEVEL CIRCUIT DESIGN DATA	6,993,733	01/31/2006
METHOD FOR DETERMINING FAULT COVERAGE FROM RTL DESCRIPTION	6,876,934	04/05/2005
METHOD FOR COMPUTING POWER SAVINGS AND DETERMINING THE PREFERRED CLOCK GATING CIRCUIT OF AN INTEGRATED CIRCUIT DESIGN	11/837,174	08/10/2007

PATENT

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METHOD FOR CHECKING CONSTRAINTS EQUIVALENCE OF AN INTEGRATED CIRCUIT DESIGN	11/755,764	05/31/2007
METHOD FOR MODELING AND VERIFYING TIMING EXCEPTIONS	11/749,090	05/15/2007
METHOD FOR ACCELERATING THE GENERATION OF AN OPTIMIZED GATE-LEVEL REPRESENTATION FROM A RTL REPRESENTATION	11/692,949	03/29/2007
METHOD FOR GENERATING TIMING EXCEPTIONS	11/676,232	02/16/2007
METHOD FOR RECOGNIZING AND VERIFYING FIFO STRUCTURES IN INTEGRATED CIRCUIT DESIGNS	11/426,936	06/27/2006
A METHOD OF OPTIMIZATION OF CLOCK GATING IN INTEGRATED CIRCUIT DESIGNS	11/419,624	05/22/2006
A METHOD FOR AUTOMATIC RECOGNITION OF HANDSHAKE DATA EXCHANGE AT CLOCK-DOMAIN CROSSING IN INTEGRATED CIRCUIT DESIGN	10/906,571	02/24/2005

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EXHIBIT C - TRADEMARKS

Description	Registration/ Application Number	Registration/ Application Date
EARLY DESIGN CLOSURE (Registered)	3,304,662	10/02/2007
ATRENTA (Registered)	3,230,964	04/17/2007
1TEAM:EMBEDDED (Registered)	3,256,970	06/26/2007
ITEAM (Registered)	3,230,954	04/17/2007
1TEAM:IMPLEMENT (Registered)	3,160,627	10/17/2006
PERISCOPE (Registered)	3,046,985	01/17/2006
ATRENTA THE PREDICTIVE ANALYSIS COMPANY (Registered)	2,799,296	12/23/2003
SPYGLASS PREDICTIVE ANALYZER (Registered)	2,778,737	10/28/2003
ATRENTA (Registered)	2,762,455	09/09/2003
SPYGLASS(Registered)	2,603,761	08/06/2002
ITEAM:ANALYZE SPYGLASS (Abandoned)	78/726,104	10/04/2005
1TEAM;SPYGLASS (Abandoned)	78/726,061	10/04/2005
FUTURE PERFECT (Suspended)	78/579,382	03/03/2005
TEAM:VERIFY (Abandoned)	78/572,545	02/22/2005
ITEAM:ANALYZE (Abandoned)	78/572,528	02/22/2005

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RECORDED: 04/17/2009