PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	Patent Security Agreement

CONVEYING PARTY DATA

Name	Execution Date
Amkor Technology, Inc.	04/16/2009

RECEIVING PARTY DATA

Name:	Bank of America, N.A.
Street Address:	901 Main Street
Internal Address:	22nd Floor
City:	Dallas
State/Country:	TEXAS
Postal Code:	75202

PROPERTY NUMBERS Total: 243

Property Type	Number
Application Number:	10634541
Application Number:	10662248
Application Number:	10766101
Application Number:	10910089
Application Number:	10992036
Application Number:	11079836
Application Number:	11096461
Application Number:	11098995
Application Number:	11111316
Application Number:	11168168
Application Number:	11177904
Application Number:	11180463
Application Number:	11228791
Application Number:	11288906

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Application Number:	11293999
Application Number:	11298016
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Patent Number:	7332712
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Patent Number:	7473584
Patent Number:	7485490
Patent Number:	7485491
Patent Number:	7485952
Patent Number:	7501338
Patent Number:	7507603

CORRESPONDENCE DATA

Fax Number: (804)344-7999
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ATTORNEY DOCKET NUMBER:	46124.090387
NAME OF SUBMITTER:	Edward T. White

Total Attachments: 12
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PATENT SECURITY AGREEMENT
(Amkor Technology, Inc.)

THIS PATENT SECURITY AGREEMENT ("Agreement") is between AMKOR TECHNOLOGY, INC., a Delaware corporation (the "Debtor"), and BANK OF AMERICA, N.A., a national banking association (the "Secured Party"), acting in its capacity as administrative agent pursuant to that certain Amended and Restated Loan and Security Agreement dated as of April 16, 2009 (as amended, restated, or otherwise modified, the "Loan Agreement") among Debtor, its Subsidiaries party thereto from time to time, the lending institutions party thereto and the Secured Party (capitalized terms defined by the Loan Agreement wherever used in this Agreement, unless otherwise defined in this Agreement, shall have the meanings specified in the Loan Agreement).

RECITALS:

A. Pursuant to the terms of the Loan Agreement, the Debtor has granted to the Secured Party a lien and security interest in all General Intangibles of the Debtor including, without limitation, all of the Debtor's right, title, and interest in, to, and under all now owned and hereafter acquired Patents (as defined below) and Patent Licenses (as defined below), and all products and proceeds thereof, to secure the payment of the Obligations.

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged, the Debtor hereby grants to the Secured Party a lien and continuing security interest in all of the Debtor's right, title, and interest in, to, and under the following (all of the following items or types of property being herein collectively referred to as the "Patent Collateral"), whether presently existing or hereafter created or acquired:

(1) each patent (the "Patent") and each application for a Patent ("Patent Application"), including, without limitation, each Patent and Patent Application referred to in Schedule 1 annexed hereto, together with any reissues, continuations, divisions, modifications, substitutions, or extensions thereof;

(2) each patent license (the "Patent License"), to the extent allowable under the license agreement, including, without limitation, each Patent License referred to in Schedule 1 annexed hereto; and

(3) all products and proceeds of the foregoing, including, without limitation, any claim by the Debtor against third parties for past, present, or future infringement or breach of any Patent or Patent License, including, without limitation, any Patent or Patent License referred to in Schedule 1 annexed hereto, and any Patent issued pursuant to a Patent Application referred to in Schedule 1 annexed hereto.

The lien and security interest contained in this Agreement is granted in conjunction with the liens and security interests granted to the Secured Party pursuant to the Loan Agreement.

The Debtor hereby acknowledges and affirms that the rights and remedies of the Secured Party with respect to the liens and security interests in the Patent Collateral made and granted hereby are more fully set forth in the Loan Agreement, the terms and provisions of which are incorporated by reference herein as if fully set forth herein.

IN WITNESS WHEREOF, the Debtor has caused this Agreement to be duly executed by its duly authorized officer as of the 16th day of April, 2009.

DEBTOR:

AMKOR TECHNOLOGY, INC.

By: _____
Name: Joanne Solomon
Title: Corporate Vice President and Chief Financial Officer

SECURED PARTY:

BANK OF AMERICA, N.A.

By: _____
Name: Joy L. Bartholomew
Title: Senior Vice President

IN WITNESS WHEREOF, the Debtor has caused this Agreement to be duly executed by its duly authorized officer as of the 16th day of April, 2009.

DEBTOR:

AMKOR TECHNOLOGY, INC.

By: _____
Name: Joanne Solomon
Title: Corporate Vice President and Chief Financial Officer

SECURED PARTY:

BANK OF AMERICA, N.A.

By: _____
Name: Joy L. Bartholomew
Title: Senior Vice President

ACKNOWLEDGMENT

STATE OF ARIZONA)
)
COUNTY OF Maricopa)

This instrument was acknowledged before me this 14th day of April, 2009, by Joanne Solomon, as Corporate Vice President and Chief Financial Officer of Amkor Technology, Inc., a Delaware corporation, on behalf of such corporation.

{Seal}

Kathleen Cole Shoopman
NOTARY PUBLIC -- ARIZONA
PINAL COUNTY
My Commission Expires
September 7, 2010

Kathleen Cole Shoopman
Notary Public in and for the State of Arizona

My commission expires: Sept 7, 2010

STATE OF TEXAS)
)
COUNTY OF DALLAS)

This instrument was acknowledged before me this __ day of April, 2009, by Joy L. Bartholomew, as Senior Vice President of Bank of America, N.A., a national banking association, on behalf of such banking association.

{Seal}

Notary Public in and for the State of Texas

My commission expires:_____

ACKNOWLEDGMENT

STATE OF ARIZONA)
)
COUNTY OF _____)

This instrument was acknowledged before me this __ day of April, 2009, by Joanne Solomon, as Corporate Vice President and Chief Financial Officer of Amkor Technology, Inc., a Delaware corporation, on behalf of such corporation.

{Seal}

_____
Notary Public in and for the State of Arizona

My commission expires:_____

STATE OF TEXAS)
)
COUNTY OF DALLAS)

This instrument was acknowledged before me this 15th day of April, 2009, by Joy L. Bartholomew, as Senior Vice President of Bank of America, N.A., a national banking association, on behalf of such banking association.

{Seal}

MARGARET A. HENDERSON
Notary Public,
State of Texas
Comm. Exp. 07-05-11

Margaret A. Henderson
Notary Public in and for the State of Texas

My commission expires: 7.5.2011

Schedule 1
to
Patent Security Agreement

#	USPN	Issued	Title
405	6,987,314	01/17/06	Stackable Semiconductor Package With Solder On Pads On Which Second Semiconductor Package Is Stacked
406	6,987,319	01/17/06	Wafer-Level Chip-Scale Package
407	6,987,661	01/17/06	Integrated Circuit Substrate Having Embedded Passive Components And Methods Therefor
409	6,995,448	02/07/06	Semiconductor Package Including Passive Elements And Method Of Manufacture
410	6,995,459	02/07/06	Semiconductor Package With Increased Number Of Input And Output Pins
411	6,998,702	02/14/06	Front Edge Chamfer Feature For Fully-Molded Memory Cards
412	7,001,799	02/21/06	Method Of Making A Leadframe For Semiconductor Devices
413	7,005,326	02/28/06	Method Of Making An Integrated Circuit Package
414	7,008,825	03/07/06	Leadframe Strip Having Enhanced Testability
415	7,009,283	03/07/06	Nonexposed Heat Sink For Semiconductor Package
416	7,009,296	03/07/06	Semiconductor Package With Substrate Coupled To A Peripheral Side Surface Of A Semiconductor Die
417	7,011,251	03/14/06	Die Down Multi-Media Card And Method Of Making Same
418	7,019,387	03/28/06	Lead-Frame Connector And Circuit Module Assembly
419	7,028,400	04/18/06	Integrated Circuit Substrate Having Laser-Exposed Terminals
420	7,030,474	04/18/06	Plastic Integrated Circuit Package And Method And Leadframe For Making The Package
421	7,030,508	04/18/06	Substrate For Semiconductor Package And Wire Bonding Method Using Thereof
422	7,042,068	05/09/06	Leadframe And Semiconductor Package Made Using The Leadframe
423	7,042,072	05/09/06	Semiconductor Package And Method Of Manufacturing The Same Which Reduces Warpage
424	7,045,396	05/16/06	Stackable Semiconductor Package And Method For Manufacturing Same
425	7,045,882	05/16/06	Semiconductor Package Including Flip Chip
426	7,045,883	05/16/06	Thermally Enhanced Chip Scale Lead On Chip Semiconductor Package And Method Of Making Same
427	7,045,893	05/16/06	Semiconductor Package And Method For Manufacturing The Same
428	7,049,682	05/23/06	Multi-Chip Semiconductor Package With Integral Shield And Antenna
429	7,057,268	06/06/06	Cavity Case With Clip/Plug For Use On Multimedia Card
430	7,057,280	06/06/06	Leadframe Having Lead Locks To Secure Leads To Encapsulant
431	7,059,040	06/13/06	Optical Module With Lens Integral Holder Fabrication Method
432	7,061,120	06/13/06	Stackable Semiconductor Package Having Semiconductor Chip Within Central Through Hole Of Substrate
433	7,064,009	06/20/06	Thermally Enhanced Chip Scale Lead On Chip Semiconductor Package and Method of Making Same
434	7,067,908	06/27/06	Semiconductor Package Having Improved Adhesiveness And Ground Bonding
435	7,071,541	07/04/06	Plastic Integrated Circuit Package And Method And Leadframe For Making The Package
436	7,071,568	07/04/06	Stacked-Die Extension Support Structure And Method Thereof
437	7,074,654	07/11/06	Tape Supported Memory Card Leadframe Structure
438	7,091,571	08/15/06	Image Sensor Package And Method For Manufacturing Thereof
439	7,091,594	08/15/06	Leadframe Type Semiconductor Package Having Reduced Inductance And Its Manufacturing Method

#	USPN	Issued	Title
440	7,095,103	08/22/06	Leadframe Based Memory Card
441	7,102,208	09/05/06	Leadframe And Semiconductor Package With Improved Solder Joint Strength
442	7,102,214	09/05/06	Pre-Molded Leadframe
443	7,102,216	09/05/06	Semiconductor Package And Leadframe With Horizontal Leads Spaced In The Vertical Direction And Method Of Making
444	7,102,891	09/05/06	Circuit Module Having Interconnects For Connecting Functioning And Non-Functioning Add Ons And Method Therefor
445	7,112,474	09/26/06	Method Of Making An Integrated Circuit Package
446	7,112,875	09/26/06	Secure Digital Memory Card Using Land Grid Arrary Structure
447	7,115,445	10/03/06	Semiconductor Package Having Reduced Thickness
448	7,126,111	10/24/06	Camera Module Having A Threaded Lens Barrel And A Ball Grid Array Connecting Device
449	7,126,218	10/24/06	Embedded Heat Spreader Ball Grid Array
450	7,132,753	11/07/06	Stacked Die Assembly Having Semiconductor Die Overhanging Support
451	7,138,707	11/21/06	Semiconductor Package Including Leads And Conductive Posts For Providing Increased Functionality
452	7,144,517	12/05/06	Manufacturing Method For Leadframe And For Semiconductor Package Using The Leadframe
453	7,145,238	12/05/06	Semiconductor Package And Substrate Having Multi-Level Vias
454	7,145,251	12/05/06	Colored Conductive Wires For A Semiconductor Package
455	7,145,253	12/05/06	Encapsulated Sensor Device
456	7,146,106	12/05/06	Optic Semiconductor Module And Manufacturing Method
457	7,154,171	12/26/07	Stacking Structure For Semiconductor Devices Using A Folded Over Flexible Substrate And Method Therefor
458	7,170,150	01/30/07	Lead Frame For Semiconductor Package
459	7,170,183	01/30/07	Wafer Level Stacked Package
460	7,176,062	02/13/07	Lead-Frame Method And Assembly For Interconnecting Circuits Within A Circuit Module
461	7,183,630	02/27/07	Lead Frame With Plated End Leads
462	7,185,426	03/06/07	Method Of Manufacturing A Semiconductor Package
463	7,190,062	03/13/07	Embedded Leadframe Semiconductor Package
464	7,190,071	03/13/07	Semiconductor Package And Method For Fabricating The Same
465	7,192,807	03/20/07	Wafer Level Package And Fabrication Method
466	7,193,305	03/20/07	Memory Card ESC Substrate Insert
467	7,119,359	04/03/07	Camera Module Fabrication Method Including Singulating A Substrate
468	7,201,327	04/10/07	Memory Card And Its Manufacturing Method
469	7,202,554	04/10/07	Semiconductor Package And Its Manufacturing Method
470	7,211,471	05/01/07	Exposed Lead QFP Package Fabricated Through The Use Of A Partial Saw Process
471	7,211,879	05/01/07	Semiconductor Package With Chamfered Corners And Method Of Manufacturing The Same
472	7,211,900	05/01/07	Thin Semiconductor Package Including Stacked Dies
473	7,214,326	05/08/07	Increased Capacity Leadframe And Semiconductor Package Using The Same
474	7,217,991	05/15/07	Fan-In Leadframe Semiconductor Package
475	7,220,915	05/22/07	Memory Card And Its Manufacturing Method
476	7,227,236	06/05/07	Image Sensor Package And Its Manufacturing Method
477	7,245,007	07/17/07	Exposed Lead Interposer Leadframe Package
478	7,247,523	07/24/07	Two-Sided Wafer Escape Package
479	7,253,503	08/07/07	Integrated Circuit Device Packages And Substrates For Making The Packages

#	USPN	Issued	Title
480	7,293,716	11/13/07	Secure Digital Memory Card Using Land Grid Array Structure
481	7,297,562	11/20/07	Circuit-On-Foil Process For Manufacturing A Laminated Semiconductor Package Substrate Having Embedded Conductive Patterns
482	7,312,103	12/25/07	Method For Making An Integrated Circuit Substrate Having Laser-Embedded Conductive Patterns
483	7,317,245	01/08/08	Method For Manufacturing A Semiconductor Device Substrate
484	7,321,162	01/22/08	Semiconductor Package Having Reduced Thickness
485	7,322,507	01/29/08	Transducer Assembly, Capillary And Wire Bonding Method Using The Same
486	7,332,375	02/19/08	Method Of Making An Integrated Circuit Package
487	7,332,712	02/19/08	Camera Module Fabrication Method Including The Step Of Removing A Lens Mount And Windoe From The Mold
488	7,334,326	02/26/08	Method For Making An Integrated Circuit Substrate Having Embedded Passive Components
489	7,335,986	02/26/08	Wafer Level Chip Scale Package
490	RE40,112	02/26/08	Semiconductor Package And Method For Fabricating The Same
491	7,342,303	03/11/08	Semiconductor Device Having RF Shielding And Method Therefor
492	7,358,174	04/15/08	Methods Of Forming Solder Bumps On Exposed Metal Pads
493	7,358,600	04/15/08	Interposer for Interconnecting Components In A Memory Card
494	7,359,204	04/15/08	Multiple Cover Memory Card
495	7,359,579	04/15/08	Image Sensor Package And Its Manufacturing Method
496	7,361,533	04/22/08	Stacked Embedded Leadframe
497	7,362,038	04/22/08	Surface Acoustic Wave (SAW) Device Package And Method For Packaging A SAW Device
498	7,365,006	04/29/08	Semiconductor Package And Substrate Having Multi-Level Vias Fabrication Method
499	7,375,975	05/20/08	Enhanced Durability Memory Card
500	7,385,408	06/10/08	Apparatus and Method For Testing Integrated Circuit Devices Having Contacts on Multiple Surfaces
501	7,399,661	07/15/08	Method For Making An Integrated Circuit Substrate Having Embedded Back-side Access Conductors And Vias
502	7,408,254	08/05/08	Stack Land Grid Array Package And Method For Manufacturing The Same
503	7,420,272	09/02/08	Two-Sided Wafer Escape Package
504	7,425,750	09/16/08	Sanp Lid Camera Module
505	7,429,799	09/30/08	Land Patterns For A Semiconductor Stacking Structure And Method Therefor
506	7,446,422	11/04/08	Wafer Level Chip Scale Package and Manufacturing Method For The Same
507	7,459,349	12/02/08	Method Of Forming A Stack Of Semiconductor Packages
508	7,459,776	12/02/09	Stacked Die Assembly Having Semiconductor Die Projecting Beyond Support
509	7,473,584	01/06/09	Method For Fabricating A Fan-In Leadframe Semiconductor Package
510	7,485,490	02/03/09	Method Of Forming A Stacked Semiconductor Package
511	7,485,491	02/03/09	Secure Digital Memory Card Using Land Grid Array Structure
512	7,485,952	02/03/09	Drop Resistant Bumpers For Fully Molded Memory Cards
513	7,501,338	03/10/09	Semiconductor Package Substrate Fabrication Method
514	7,507,603	03/24/09	Etch Singulated Semiconductor Package

Amkor Technology, Inc.
Pending Patent Applications
CONFIDENTIAL

#	Serial No.	Filed on	Title
1	10/634,541	08/04/03	Semiconductor Memory Card
2	10/662,248	09/15/03	Near Chip Size Semiconductor Package
3	10/766,101	01/28/04	Double Mold Memory Card And Its Manufacturing Method
4	10/910,089	08/03/04	Offset Etched Corner Leads For Semiconductor Package
5	10/992,036	11/17/04	Shielded Package Having Shield Fence
6	11/079,836	03/14/05	Reduced Size Semiconductor Package With Stacked Dies
7	11/096,461	04/01/05	Molded Camera Module and Fabrication Method
8	11/098,995	04/05/05	Method For Making An Integrated Circuit Substrate Having Laminated Laser-Embedded Circuit Layers
9	11/111,316	04/21/05	Trace Fill Substrate For Die Attach Film and Semiconductor Package Using The Same
10	11/168,168	06/27/05	Package In Package (PIP)
11	11/177,904	07/07/05	Direct Glass Attach On Die Camera Module And Method
12	11/180,463	07/12/05	Apparatus and Method For Testing Integrated Circuit Devices Having Contacts on Multiple Surfaces
13	11/228,791	09/16/05	Wire Bonding Machine Capable Of Removing Particles From Capillary And Cleaning Method Of Capillary Bottom Tip
14	11/288,906	11/29/05	Modular Memory Card And Method Of Making Same
15	11/293,999	12/05/05	Semiconductor Package Including A Top-Surface Metal Layer For Implementing Circuit Features
16	11/298,016	12/08/05	Embedded Electronic Component Package
17	11/315,994	12/21/05	Optical Module Having Cavity Substrate
18	11/356,921	02/17/06	Stacked Electronic Component Package Having Film-On-wire Spacer
19	11/365,246	03/01/06	Leadframe Having Lead Locks To Secure Leads To Encapsulant
20	11/367,171	03/03/06	Land Patterns For A Semiconductor Stacking Structure And Method Thereof
21	11/372,597	03/10/06	Leadframe And Semiconductor Package Made Using The Leadframe
22	11/379,550	04/20/06	Chamfered Memory Card Module And Method Of Making Same
23	11/408,521	04/21/06	Semiconductor Package Having Improved Adhesiveness And Ground Bonding
24	11/382,615	05/10/06	Semiconductor Package Including Premold And Method Of Manufacturing The Same
25	11/440,662	05/24/06	Semiconductor Package And Method Of Making The Same
26	11/440,548	05/24/06	Substrate For Semiconductor Device And Manufacturing Method Thereof
27	11/472,874	06/21/06	Passive Device Structure And Fabrication Method
28	11/425,502	06/21/06	Tape Supported Memory Card Leadframe Structure
29	11/425,505	06/21/06	Side Leaded, Bottom Exposed Pad And Bottom Exposed Lead Fusion Quad Flat Semiconductor Package
30	11/497,617	08/01/06	Buildup Dielectric And Metallization Process And Semiconductor Package
31	11/510,544	08/25/06	Lead Frame For Semiconductor Package
32	11/543,540	10/04/06	Method And Structure For Creating Embedded Metal Features
33	11/592,889	11/02/06	Exposed Die Overmolded Flip Chip Package and Fabrication Method
34	11/557,884	11/08/06	Thermally Enhanced Semiconductor Package
35	11/595,411	11/09/06	Semiconductor Package Including Top-Surface Terminals For Mounting Another Semiconductor Package
36	11/560,496	11/16/06	Stacked Redistribution Layer (RDL) Die Assembly Package
37	11/605,740	11/28/06	Electronic Component Package Comprising Fan-Out And Fan-In

#	Serial No.	Filed on	Title
			Traces
38	11/566,731	12/05/06	A Membrane Die Attach Element Package And Method Therefor
39	11/615,467	12/22/06	Blind Via Capture Pad Structure And Fabrication Method
40	11/616,069	12/26/06	Exposed Metal Bezel For Use In Sensor Devices And Method Therefor
41	11/616,747	12/27/06	Semiconductor Package Having Leadframe With Exposed Anchor Pads
42	11/621,402	01/09/07	Embedded Circuit Pattern Fabrication Method And Structure
43	11/621,630	01/10/07	Methods Of Forming Back Side Layers For Thinned Wafers And Related Structures
44	11/624,648	01/18/07	Stackable Semiconductor Package Including Laminate Interposer
45	11/671,026	02/05/07	Methods Of Forming Electronic Interconnections Including Compliant Layers And Related Devices
46	11/671,018	02/05/07	Methods Of Forming Metal Layers Using Multi-Laer Lift-Off Patterns
47	11/677,506	02/21/07	Semiconductor Package In Package
48	11/681,121	03/01/07	High Density Memory Card Using Folded Flex
49	11/682,666	03/06/07	Stackable Semiconductor Package Having Partially Exposed Semiconductor Die And Method Of Fabricating Of The Same
50	11/734,999	04/13/07	Semiconductor Package And Fabricating Method Thereof
51	11/754,209	05/25/07	A Semiconductor Device Having EMI Shielding And Method Therefor
52	11/810,799	06/06/07	Direct-Write Wafer Level Chip Scale Package
53	11/765,806	06/20/07	Metal Etch Stop Fabrication Method And Structure
54	11/765,858	06/20/07	Embedded Die Metal Etch Stop Fabrication Method And Structure
55	11/824,395	06/29/07	Build Up Motherboard Fabrication Method And Structure
56	11/775,566	07/10/07	Fusion Quad Flat Semiconductor Package
57	11/775,492	07/10/07	A Semiconductor Device Having RF Shielding And Method Therefor
58	11/832,571	08/01/07	A Semiconductor Package And Method Of Manufacturing
59	11/835,235	08/07/07	Dual Laminate Package Structure With Embedded Elements
60	11/839,277	08/15/07	Straight Conductor Blind Via Capture Pad Structure And Fabrication Method
61	11/903,002	09/19/07	Substrate Having Stiffner Fabrication Method
62	11/865,617	10/01/07	Thin Stacked Interposer Package
63	11/866,886	10/03/07	Semiconductor Package With Increased I/O Density And Method Of Making The Same
64	11/867,293	10/04/07	Wafer Level Package Utilizing Laser-Activated Dielectric Material
65	11/873,229	10/16/07	Structure Of Bond Pad For Semiconductor Die And Method Therefor
66	11/875,597	10/19/07	Solder Attach Film And Method Of Forming Solder Ball Using The Same
67	11/924,156	10/25/07	Embedded Passive Component Network Substrate And Fabrication Method
68	11/982,637	11/01/07	Circuit-On-Foil Process For Manufacturing A Laminated Semiconductor Package Substrate Having Embedded Conductive Patterns
69	11/933,908	11/01/07	Semiconductor Package And Fabrication Method Thereof
70	11/935,314	11/05/07	Reduced Size Stacked Semiconductor Package And Method Of Making The Same
71	11/942,254	11/19/07	A Semiconductor Device Having RF Shielding And Method Therefor
72	11/947,505	11/29/07	Semiconductor Package Having Reduced Thickness
73	1/953,680	12/10/07	Thin Substrate Fabrication Method And Structure
74	12/005,081	12/21/07	Method Of Using A Camera Module
75	11/970,712	01/08/08	Integrated Circuit Package And Method Of Making The Same
76	11/971,577	01/09/08	A Semiconductor Device Having RF Shielding And Method Therefor
77	12/015,428	01/16/08	Semiconductor Package With Patterning Layer And Method Of Making Same

#	Serial No.	Filed on	Title
78	12/017,266	01/21/08	Stacked Semiconductor Package And Method Of making Same
79	12/018,435	01/23/08	Shielded Trace Structure And Fabrication Method
80	12/025,336	02/04/08	Semiconductor Package And Fabricating Method Thereof
81	12/036,498	02/25/08	A Semiconductor Device Having Improved Contact Interface Reliability And Method Therefor
82	12/100,886	04/10/08	Flat Semiconductor Package With Half Package Molding
83	12/105,196	04/17/08	Semiconductor Package With Fast Power-Up Cycle And Method Of Making Same
84	12/107,478	04/22/08	A System And Method To Reduce Shorting Of Radis Frequency (RF) Shielding
85	12/108,419	04/23/08	A Semiconductor Device Having Reduced Thermal Interface Material (TIM) Degradation And Method Therefor
86	12/108,909	04/24/08	Lead Free Alloy Bump Structure And Fabrication Method
87	12/116,127	05/06/08	Semiconductor Package With Half-Etched Locking Features
88	12/116,695	05/07/08	Semiconductor Device And Manufacturing Method Thereof
89	12/151,857	05/09/08	Multi-Level Circuit Substrate And Fabrication Method
90	12/144,145	06/23/08	Flip Chip Bump Structure And Fabrication Method
91	12/169,151	07/07/08	A Semiconductor Device Having Improved Contact Interface Reliability And Method Therefor
92	12/181,256	07/28/08	Increased I/O Semiconductor Package And Method Of Making Same
93	12/183,779	07/31/08	Stacked Inverted Flip Chip Package And Fabrication Method
94	12/183,979	07/31/08	Increased Capacity Semiconductor Package
95	12/221,797	08/05/08	Tow-Sided Fan-Out Wafer Escape Package
96	12/187,578	08/07/08	Land Patterns For A Semiconductor Stacking Structure And Method Thereof
97	12/221,948	08/08/08	Camera Module With Window Attachment
98	12/190,039	08/12/08	Semiconductor package And Fabricating Method Thereof
99	12/204,692	09/04/08	Semiconductor Device And Fabricating Method Therefor
100	12/237,173	09/24/08	Ultra Thin Package And Fabrication Method
101	12/242,603	09/30/08	Semiconductor Device Including Leadframe With Increased I/O
102	12/246,226	10/06/08	Increased I/O Semiconductor Package And Method Of Making Same
103	12/259,096	10/27/08	Semiconductor Device With Increased I/O Leadframe
104	12/291,119	11/05/08	Stackable Semiconductor Package
105	12/291,767	11/12/08	Stacked Flip Chip Die Assembly
106	12/269,357	11/12/08	Package Failure Prognostic Structure And Method
107	12/270,690	11/13/08	Semiconductor Devices And Fabricating Methods Thereof
108	12/272,606	11/17/08	Semiconductor Device Including Increased Capacity Leadframe
109	12/273,500	11/18/08	Semiconductor Device With Increased I/O Leadframe Including Passive Device
110	12/276,108	11/21/08	Package In Package Semiconductor Device With Shortened Signal Paths
111	12/276,121	11/21/08	Semiconductor Device Including Leadframe Having Power Bars And Increased I/O
112	12/323,124	11/25/08	A System And Method To Provide RF Shielding For MEMS Microphone Package
113	12/327,716	12/03/08	Shielding For A Semiconductor Package
114	12/327,763	12/03/08	Package In Package Semiconductor Device
115	12/330,424	12/08/08	Package In Package Semiconductor Device With Film Over Wire
116	12/330,769	12/09/08	A System And Method For Conformal Shielding Of Stacked Packages
117	12/335,365	12/15/08	A Semiconductor Device Having EMI Shielding And Method Therefor
118	12/342,386	12/23/08	Semiconductor Package Having A Heat Spreader With A Top Mold Gate
119	12/342,829	12/23/08	A System And Method For Shielding Of Package On Package (PoP) Assemblies

#	Serial No.	Filed on	Title
120	12/342,839	12/23/08	Protruding Post Substrate Package Structure And Method
121	12/317,649	12/23/08	Adhesive On Wire Stacked Semiconductor Package
122	12/348,813	01/05/09	Semiconductor Device With Through Mold Via
123	12/348,853	01/05/09	Leadframe Structure For Concentrated Photovoltaic Receiver Package
124	12/351,596	01/09/09	Extended Landing Pad Substrate Package Structure And Method
125	12/351,690	01/09/09	Package In Package Device For RF Transceiver Module
126	12/365,682	02/04/09	Etch Singulated Semiconductor Package
127	12/390,999	02/23/09	Reducted Profile Stackable Semiconductor Device
128	12/339,772	03/03/09	Semiconductor Device
129	12/397,470	03/04/09	Reversible Top/Bottom Package
130	12/398,089	03/04/09	Conformal Shiled On Punch QFN Semiconductor Package
131	12/399,600	03/06/09	Leadframe For Semiconductor Package
132	12/405,854	03/17/09	Adhesive Composite For Semiconductor Device
133	12/414,220	03/30/09	Fine Pitch Copper Pillar Package And Method
134	12/419,180	04/06/09	Semiconductor Device With Increased I/O Leadframe Including Power Bars