PATENT ASSIGNMENT

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NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
IRVINE SENSORS CORPORATION	03/16/2009

RECEIVING PARTY DATA

Name:	APROLASE DEVELOPMENT CO., LLC
Street Address:	2711 Centerville Road
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City:	Wilmington
State/Country:	DELAWARE
Postal Code:	19808

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	07985837

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ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, Irvine Sensors Corporation, a Delaware corporation, with an office at 3001 Redhill Ave., Bldg. 4, Suite 108, Costa Mesa, CA 92672 (***"Assignor"***), does hereby sell, assign, transfer, and convey unto Aprolase Development Co., LLC, a Delaware limited liability company, having an address at 2711 Centerville Road, Suite 400, Wilmington, DE 19808 (***"Assignee"***), or its designees, all right, title, and interest that exist today and may exist in the future in and to any and all of the following (collectively, the ***"Patent Rights"***):

(a) the provisional patent applications, patent applications and patents listed in the table below (the ***"Patents"***);

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
5,235,672 (07/651,477)	US	8/10/1993 (2/6/1991)	Hardware for electronic neural network Carson, John C.
6,389,404 (09/223,476)	US	5/14/2002 (12/30/1998)	Neural processing module with input architectures that make maximal use of a weighted synapse array Carson, John C.; Saunders, Christ H.
6,650,704 (09/427,384)	US	11/18/2003 (10/25/1999)	Method of producing a high quality, high resolution image from a sequence of low quality, low resolution images that are undersampled and subject to jitter Carlson, Randolph S.; Arnold, Jack L.; Feldmus, Valentine G.
6,829,237 (09/973,857)	US	12/7/2004 (10/9/2001)	High speed multi-stage switching network formed from stacked switching layersCarson, John C.; Ozguz, Volkan H.
7,082,591 (10/346,363)	US	7/25/2006 (1/17/2003)	Method for effectively embedding various integrated circuits within field programmable gate arrays Carlson, Randolph S.
6,856,167 (10/347,038)	US	2/15/2005 (1/17/2003)	Field programmable gate array with a variably wide word width memory Ozguz, Volkan H.; Carlson, Randolph S.; Gann, Keith D.; Leon, John P.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
7,265,579 (11/037,490)	US	9/4/2007 (1/18/2005)	Field programmable gate array incorporating dedicated memory stacks Carlson, Randolph Stuart; Ozguz, Volkan; Gann, Keith D.; Leon, John P.
5,508,836 (08/305,066)	US	4/16/1996 (9/13/1994)	Infrared wireless communication between electronic system components DeCaro, Robert; Saunders, Christ H.; Maeding, Dale
5,635,705 (08/526,415)	US	6/3/1997 (9/11/1995)	Sensing and selecting observed events for signal processing Saunders, Christ H.
6,195,268 (09/031,435)	US	2/27/2001 (2/26/1998)	Stacking layers containing enclosed IC chips Eide, Floyd K.
5,045,685 (07/534,969)	US	9/3/1991 (6/6/1990)	Analog to digital conversion on multiple channel IC chips Wall, Llewellyn E.
5,104,820 (07/720,025)	US	4/14/1992 (6/24/1991)	Method of fabricating electronic circuitry unit containing stacked IC layers having lead rerouting Go, Tiong C.(deceased,); Minahan, Joseph A.; Shanken, Stuart N.
5,279,991 (07/996,794)	US	1/18/1994 (12/24/1992)	Method for fabricating stacks of IC chips by segmenting a larger stack Minahan, Joseph A.; Pepe, Angel A.
5,432,318 (08/178,923)	US	7/11/1995 (1/7/1994)	Apparatus for segmenting stacked IC chips Minahan, Joseph A.
5,304,790 (07/956,914)	US	4/19/1994 (10/5/1992)	Apparatus and system for controllably varying image resolution to reduce data output Arnold, Jack
5,347,428 (07/985,837)	US	9/13/1994 (12/3/1992)	Module comprising IC memory stack dedicated to and structurally combined with an IC microprocessor chip Carson, John C.; Indin, Ronald J.; Shanken, Stuart N.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
5,406,701 (08/120,675)	US	4/18/1995 (9/13/1993)	Fabrication of dense parallel solder bump connections Pepe, Angel A.; Reinker, David M.; Minahan, Joseph A.
5,424,920 (08/232,739)	US	6/13/1995 (4/25/1994)	Non-conductive end layer for integrated stack of IC chips Miyake, Michael K.
5,432,729 (08/255,465)	US	7/11/1995 (6/8/1994)	Electronic module comprising a stack of IC chips each interacting with an IC chip secured to the stack Carson, John C.; Some, Raphael R.
5,581,498 (08/326,645)	US	12/3/1996 (10/20/1994)	Stack of IC chips in lieu of single IC chip Ludwig, David E.; Saunders, Christ H.; Some, Raphael R.; Stuart, John J.
5,688,721 (08/62,2671)	US	11/18/1997 (3/26/1996)	3D stack of IC chips having leads reached by vias through passivation covering access plane Johnson, Tony K.
5,953,588 (08/777,747)	US	9/14/1999 (12/21/1996)	Stackable layers containing encapsulated IC chips Camien, Andrew N; Yamaguchi, James S.
6,072,234 (09/316,740)	US	6/6/2000 (5/21/1999)	Stack of equal layer neo-chips containing encapsulated IC chips of different sizes Camien, Andrew N.; Yamaguchi, James S.
5,955,668 (09/166,458)	US	9/21/1999 (10/5/1998)	Multi-element micro gyro Hsu, Ying W.; Reeds, III, John W.; Saunders, Christ H.
6,089,089 (09/301,847)	US	7/18/2000 (4/29/1999)	Multi-element micro gyro Hsu, Ying W.
6,578,420 (09/604,782)	US	6/17/2003 (6/26/2000)	Multi-axis micro gyro structure Hsu, Ying Wen
6,014,316 (09/095,416)	US	1/11/2000 (6/10/1998)	IC stack utilizing BGA contacts Eide, Floyd K.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
6,028,352 (09/095,415)	US	2/22/2000(6/10/1998)	IC stack utilizing secondary lead frames Eide, Floyd K.
6,117,704 (09/282,704)	US	9/12/2000 (3/31/1999)	Stackable layers containing encapsulated chips Yamaguchi, James S.; Ozguz, Volkan H.; Camien, Andrew N.
6,476,392 (09/853,819)	US	11/5/2002 (5/11/2001)	Method and apparatus for temperature compensation of an uncooled focal plane array Kaufman, Charles S.; Carson, Randolph S.; Hornback, William B.
6,891,160 (10/281,393)	US	5/10/2005 (10/25/2002)	Method and apparatus for temperature compensation of an uncooled focal plane array Kaufman, Charles S.; Carson, Randolph S.; Hornback, William B.
7,235,785 (11/048,634)	US	6/26/2007 (1/31/2005)	Imaging device with multiple fields of view incorporating memory-based temperature compensation of an uncooled focal plane array Hornback, Bert; Harwood, Doug; Boyd, W. Eric; Carlson, Randy
6,596,997 (09/921,525)	US	7/22/2003 (8/3/2001)	Retro-reflector warm stop for uncooled thermal imaging cameras and method of using the same Kaufman, Charles S.
6,706,971 (10/142,557)	US	3/16/2004 (5/10/2002)	Stackable microcircuit layer formed from a plastic encapsulated microcircuit Albert, Douglas M.; Gann, Keith D.
7,174,627 (10/338,974)	US	2/13/2007 (1/9/2003)	Method of fabricating known good dies from packaged integrated circuits Gann, Keith D.
6,560,109 (09/949,024)	US	5/6/2003 (9/7/2001)	Stack of multilayer modules with heat-focusing metal layer Yamaguchi, James Satsuo; Pepe, Angel Antonio; Ozguz, Volkan H.; Camien, Andrew Nelson

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
6,717,061 (09/949,512)	US	4/6/2004 (9/7/2001)	Stacking of multilayer modules Yamaguchi, James Satsuo; Pepe, Angel Antonio; Ozguz, Volkan H.; Camien, Andrew Nelson
6,734,370 (09/948,950)	US	5/11/2004 (9/7/2001)	Multilayer modules with flexible substrates Yamaguchi, James Satsuo; Pepe, Angel Antonio; Ozguz, Volkan H.; Camien, Andrew Nelson
7,127,807 (10/431,914)	US	10/31/2006 (5/7/2003)	Process of manufacturing multilayer modules Yamaguchi, James Satsuo; Pepe, Angel Antonio; Ozguz, Volkan H.; Camien, Andrew Nelson
6,797,537 (09/938,686)	US	9/28/2004 (10/30/2001)	Method of making stackable layers containing encapsulated integrated circuit chips with one or more overlaying interconnect layers Pepe, Angel Antonio; Yamaguchi, James Satsuo
6,784,547 (10/302,680)	US	8/31/2004 (11/21/2002)	Stackable layers containing encapsulated integrated circuit chips with one or more overlying interconnect layers Pepe, Angel Antonio; Yamaguchi, James Satsuo
7,239,012 (10/951,990)	US	7/3/2007 (9/28/2004)	Three-dimensional module comprised of layers containing IC chips with overlying interconnect layers Pepe, Angel; Yamaguchi, James
6,806,559 (10/128,728)	US	10/19/2004(4/22/2002)	Method and apparatus for connecting vertically stacked integrated circuit chips Gann, Keith D.; Albert, Douglas M.
6,912,862 (10/615,641)	US	7/5/2005 (7/8/2003)	Cryopump piston position tracking Sapir, Itzhak
6,967,411 (10/360,244)	US	11/22/2005 (2/7/2003)	Stackable layers containing ball grid array packages Eide, Floyd K.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
7,242,082 (11/229,351)	US	6/10/2007 (9/15/2005)	Stackable layer containing ball grid array package Eide, Floyd
6,993,835 (10/726,888)	US	2/7/2006 (12/4/2003)	Method for electrical interconnection of angularly disposed conductive patterns Albert, Douglas Marice
6,998,328 (10/701,783)	US	2/14/2006 (11/5/2003)	Method for creating neo-wafers from singulated integrated circuit die and a device made according to the method Stern, Jonathan Michael
7,417,323 (10/703,177)	US	(11/6/2003)	Neo-wafer device and method Sambo S. He
7,198,965 (11/354,370)	US	4/3/2007 (2/14/2006)	Method for making a neo-layer comprising embedded discrete components He, Sambo
7,180,579 (10/806,037)	US	2/20/2007 (3/22/2004)	Three-dimensional imaging processing module incorporating stacked layers containing microelectronic circuits Ludwig, David E.; Kennedy, John V.; Kleinhans, William; Liu, Tina; Krutzik, Christian
7,436,494 (11/706,724)	US	10/14/2008 (2/15/2007)	Three-dimensional LADAR module with alignment reference insert circuitry Ludwig, David E.; Kennedy, John V.; Kleinhans, William; Liu, Tina; Krutzik, Christian
7,335,576 (11/197,828)	US	2/26/2008 (8/5/2005)	Method for precision integrated circuit die singulation using differential etch rates David, Ludwig; Yamaguchi, James; Clark, Stuart; Boyd, W. Eric
7,380,459 (11/654,292)	US	6/3/2008 (1/16/2007)	Absolute pressure sensor Sapir, Itzhak
10/968,572	US	10/19/2004	Vertically stacked pre-packaged integrated circuit chips Keith Gann; Douglas N. Albert

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
7,440,449 (10/960,712)	US	10/6/2004	High speed switching module comprised of stacked layers incorporating T-connect structures John C. Carson; Volkan H. Orguz
11/977,447	US	10/24/2007	Wire bond method for angularly disposed conductive pads and a device made from the method Randy Wayne Bindrup
11/897,938	US	08/31/2007	Field programmable gate array utilizing dedicated memory stacks in a vertical layer format Ozguz, Volkan; Carlson, Randolph Stuart; Gann, Keith D.; Leon, John P.; Boyd, W Eric
11/825,643	US	7/7/2007	Ball grid array package format layers and structure Keith Gann; W Eric Boyd
11/807,671	US	5/30/2007	Large Format Thermoelectic Infrared Detector and a Method of Fabrication Ying Hsu
11/731,154	US	3/31/2007	Ball Grid Array Stack Frank Mantz
11/524,090	US	9/20/2006	Stackable tier structure comprising high density feedthrough Volkan Ozguz; Jonathan Stern
11/511,117	US	8/26/2006	MEMS cooling device Itzhak Sapir
11/499,403	US	8/4/2006	High density interconnect assembly comprising stacked electronic module John V. Kennedy
11/441,908	US	5/26/2006	Stackable tier structure comprising prefabricated high density feedthrough Volkan Ozguz; Jonathan Stern
11/429,468	US	5/5/2006	Global positioning using planetary constants Sapir Itzhak

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
11/415,891	US	5/1/2006	Low power electronic circuit incorporating real time clock Gary Gottlieb
11/350,974	US	2/8/2006	Stacked ball grid array package module utilizing one or more interposer layers William E. Boyd; Daniel Michaels
11/301,645	US	12/12/2005	Cornerbond assembly comprising three-dimensional electronic modules Albert Douglas
11/259,683	US	10/25/2005	Stacked microelectronic layer and module with three-axis channel T-connects Keith D. Gann; W. Eric Boyd
11/248,659	US	10/11/2005	Anti-tamper module Volkan H. Ozguz; John Leon
10/178,390	US	6/24/2002	Video event capture, storage and processing method and apparatus Randolph S. Carlson
60/993,689	US		Chip scale vacuum pump Itzhak Sapir
11/150,712	US	6/10/2005	Stackable semiconductor chip layer comprising prefabricated trench interconnect vias W. Eric Boyd; Angel Pepe; James Yamaguchi; Volkan Ozguz; Andrew Camien; Douglas Albert
11/062,507	US	2/22/2005	BGA-scale stacks comprised of layers containing integrated circuit die and a method for making the same Gann Keith; William E. Boyd
12/008,253	US	1/8/2008	Microcombustion power system Ying Hsu
61/007,497	US	12/12/2007	Forced vibration piezo generator Itzhak Sapir
SE0570479 (SE92905662.0)	SE	10/10/2001 (1/29/1992)	Hardware for electronic neural network Carson, John C.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
NL0570479 (NL92905662.0)	NL	10/10/2001 (1/29/1992)	Hardware for electronic neural network Carson, John C.
JP2005-507894	JP	1/16/2006	Stackable layers containing ball grid array packages Inventorship not available
JP2006-286556	JP	10/20/2006	Stackable tier structure comprising high density feedthrough Volkan Ozguz; Jonathan Stern
JP2000-591490	JP	12/30/1999	Neural processing module with input architectures that make maximal use of a weighted synapse array Carson, John C.; Saunders, Christ H.
JP3308265 (JP12-554175)	JP	6/10/1999	IC stack utilizing flexible circuits with BGA contacts Eide, Floyd K.
JP3511008 (JP12-553982)	JP	6/10/1999	IC stack utilizing secondary leadframes Eide, Floyd K.
JP3544974 (JP06-0502691)	JP	5/5/1993	Non-conductive end layer for integrated stack of IC chips Miyake, Michael K.
GB0570479 (GB92905662.0)	GB	10/10/2001 (1/29/1992)	Hardware for electronic neural network Carson, John C.
GB1097467 (GB9992850.2)	GB	11/2/2006 (6/10/1993)	IC stack utilizing secondary leadframes Eide, Floyd K.
GB1596433 (GB04394026.1)	GB	1/2/2008 (5/12/2004)	A method for creating neo-wafers from singulated integrated circuit die and a device made according to the methodStern, Jonathan Michael
GB0596075 (GB93911250.4)	GB	8/22/2001 (5/5/1993)	Non-conductive end layer for integrated stack of IC chips Miyake, Michael K.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
GB0683968 (GB94903352.6)	GB	10/24/2002 (12/1/1993)	Module comprising IC memory stack dedicated to and structurally combined with an IC microprocessor chip Carson, John C.; Indin, Ronald J.; Shanken, Stuart N.
GB0695494 (GB94915397.7)	GB	2/24/2001 (4/19/1994)	Electronic module comprising a stack of IC chips Carson, John C.; Some, Raphael R.
GB0713609 (GB94925876.8)	GB	5/7/2003(8/12/1994)	Stack of IC chips as substitute for single IC chipLudwig, David E.; Saunders, Christ H.; Some, Raphael R.; Stuart, John J.
GB067087 (GB94909418.9)	GB	(12/16/1993)	Fabricating stacks of IC chips by segmenting a larger stack MINIHAN JOSEPH A; PEPE ANGEL A
FR1097467 (FR99928570.2)	FR	11/2/2006 (6/10/1993)	IC stack utilizing secondary leadframes Eide, Floyd K.
FR1596433 (FR04394026.1)	FR	1/2/2008 (5/12/2004)	A method for creating neo-wafers from singulated integrated circuit die and a device made according to the method Stern, Jonathan Michael
FR0596075 (FR93911250.4)	FR	8/22/2001 (5/5/1993)	Non-conductive end layer for integrated stack of IC chips Miyake, Michael K.
FR0683968 (FR94903352.6)	FR	10/24/2002 (12/1/1993)	Module comprising IC memory stack dedicated to and structurally combined with an IC microprocessor chip Carson, John C.; Indin, Ronald J.; Shanken, Stuart N.
FR0695494 (FR94915397.7)	FR	2/24/2001 (4/19/1994)	Electronic module comprising a stack of IC chips Carson, John C.; Some, Raphael R.
FR0713609 (FR94925876.8)	FR	5/7/2003 (8/12/1994)	Stack of IC chips as substitute for single IC chip Ludwig, David E.; Saunders, Christ H.; Some, Raphael R.; Stuart, John J.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
EP02705988.0	EP	1/25/2002	A stackable microcircuit layer formed from a plastic encapsulated microcircuit and method of making the same Albert, Douglas M.; Gann, Keith D.
EP06255467.0	EP	10/24/2006	Stackable tier structure comprising high density feedthrough Volkan Ozguz; Jonathan Stern
EP99967712.3	EP	12/30/1999	Neural processing module with input architectures that make maximal use of a weighted synapse array Carson, John C.; Saunders, Christ H.
EP99928570.2	EP	6/10/1993	IC stack utilizing flexible circuits with BGA contacts Eide, Floyd K.
EP02805694.3	EP	7/16/2002	Wearable biomonitor with flexible thinned integrated circuit Ogzuz, Volkhan H; Khashayar, Abbas
EP02789292.6	EP	10/25/2002	Stackable layers containing encapsulated integrated circuit chips with one or more overlying interconnect layers and a method of making the same Pepe, Angel Antonio; Yamaguchi, James Satsuo
EP02798173.7	EP	9/9/2002	Stacking of multilayer modules Yamaguchi, James Satsuo; Pepe, Angel Antonio; Ozguz, Volkan H.; Camien, Andrew Nelson
EP95935157.8	EP	9/27/1995	Infrared wireless communication between electronic system components DeCaro, Robert; Saunders, Christ H.; Maeding, Dale
EP03721978.9	EP	4/22/2003	Method and apparatus for connecting vertically stacked integrated circuit chips Gann, Keith D.; Albert, Douglas M.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
DE69232116 (DE69232116)	DE	10/10/2001 (1/29/1992)	Hardware for electronic neural network Carson, John C.
DE69330630 (DE69330630)	DE	8/22/2001 (5/5/1993)	Non-conductive end layer for integrated stack of IC chips Miyake, Michael K.
DE69426695 (DE6942669.5)	DE	2/24/2001 (4/19/1994)	Electronic module comprising a stack of IC chips Carson, John C.; Some, Raphael R.
DE602004011025 (DE602004011025)	DE	1/2/2008 (5/12/2004)	A method for creating neo-wafers from singulated integrated circuit die and a device made according to the method Stern, Jonathan Michael
PCT/US06/039915	WO	8/26/2006	MEMS cooling device Itzhak Sapir
4,814,629 (07/107352)	US	3/21/1989 (10/13/1987)	Pixel displacement by series-parallel analog switching Arnold, Jack L.
11/825,643	US	7/7/2007	Ball grid array package format layers and structure Keith Gann
EP06738029.5	EP	3/10/2006	Method for making a neo-layer comprising embedded discrete components Sambo S. He
JP2000-519921	JP	11/10/1998	Method for thinning semiconductor wafers with circuits and wafers made by the same Inventorship not available
JP2004-72804	JP	3/15/2004	Stackable layer, mini stack, and laminated electronic module Volkan Ozguz
EP06735419.1	EP	2/14/2006	Stacked ball grid array package module utilizing one or more interposer layers William E. Boyd
5,635,010	US	4/14/1995	Dry adhesive joining of layers of electronic devices Angel A. Pepe
6,731,121	US	10/16/2000	Highly configurable capacitive transducer interface circuit Christ Ying Hsu

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
6,513,380	US	6/19/2001	Mems sensor with single central anchor and motion-limiting connection geometry John William Reeds III
6,715,352	US	6/26/2001	Method of designing a flexure system for tuning the modal response of a decoupled micromachined gyroscope and a gyroscoped designed according to the method Michael J. Tracy
6,370,937	US	3/19/2001	Method of canceling quadrature error in an angular rate sensor Ying Wen Hsu
JP2664754	JP	1/4/1998	High density electronic package comprising stacked sub-modules Tiong C. Go
JP2001-533437	JP	10/16/2000	Highly configurable capacitive transducer interface circuit Christ Ying Hsu
EP02744453.8	EP	6/18/2002	Mems sensor with single central anchor and motion-limiting connection geometry John William Reeds III
EP02746710.9	EP	6/18/2002	Method of designing a flexure system for tuning the modal response of a decoupled micromachined gyroscope and a gyroscoped designed according to the method Michael J. Tracy
JP2002-562134	JP	1/25/2002	A stackable microcircuit layer formed from a plastic encapsulated microcircuit and method of making the same
12/287,691	US	10/10/2008	Three dimensional LADAR module with alignment reference insert circuitry comprising high density interconnect structure John Kennedy; David Ludwig; Christian Krutzik
EP03818224.2	EP	8/8/2003	Stackable layers containing ball grid array packages Eide, Floyd K.

(b) all patents and patent applications (i) to which any of the Patents directly or indirectly claims priority, (ii) for which any of the Patents directly or indirectly forms a basis for priority, and/or (iii) that were co-owned applications that incorporate by reference, or are incorporated by reference into, the Patents;

(c) all reissues, reexaminations, extensions, continuations, continuations in part, continuing prosecution applications, requests for continuing examinations, divisions, registrations of any item in any of the foregoing categories (a) and (b);

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(1) damages,
(2) injunctive relief, and
(3) any other remedies of any kind

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(1) Assignor has the full power and authority, and has obtained all third party consents, approvals and/or other authorizations required to enter into this Agreement and to carry out its obligations hereunder, including the assignment of the Patent Rights to Assignee; and

(2) Assignor owns, and by this document assigns to Assignee, all right, title, and interest to the Patent Rights, including, without limitation, all right, title, and interest to sue for infringement of the Patent Rights. Assignor has obtained and properly recorded previously executed assignments for the Patent Rights as necessary to fully perfect its rights and title therein in accordance with governing law and regulations in each respective jurisdiction. The Patent Rights are free and clear of all liens, claims, mortgages, security interests or other encumbrances, and restrictions. There are no actions, suits, investigations, claims or proceedings threatened, pending or in progress relating in any way to the Patent Rights. There are no existing contracts, agreements, options, commitments, proposals, bids, offers, or rights with, to, or in any person to acquire any of the Patent Rights.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

Assignor will, at the reasonable request of Assignee and without demanding any further consideration therefore, do all things necessary, proper, or advisable, including without limitation, the execution, acknowledgment, and recordation of specific assignments, oaths, declarations, and other documents on a country-by-country basis, to assist Assignee in obtaining, perfecting, sustaining, and/or enforcing the Patent Rights. The terms and conditions of this Assignment of Patent Rights will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed at Costa Mesa, California on March 16, 2009.

ASSIGNOR:

Irvine Sensors Corporation

By: _____
Name: John J. Stuart, Jr.
Title: Sr. VP & Chief Financial Officer
(Signature MUST be attested)

ATTESTATION OF SIGNATURE PURSUANT TO 28 U.S.C. § 1746

The undersigned witnessed the signature of John J. Stuart, Jr. to the above Assignment of Patent Rights on behalf of Irvine Sensors Corporation and makes the following statements:

1. I am over the age of 18 and competent to testify as to the facts in this Attestation block if called upon to do so.

2. John J. Stuart, JR is personally known to me (or proved to me on the basis of satisfactory evidence) and appeared before me on 16 march, 2009 to execute the above Assignment of Patent Rights on behalf of Irvine Sensors Corporation.

3. John J. Stuart, JR subscribed to the above Assignment of Patent Rights on behalf of Irvine Sensors Corporation.

I declare under penalty of perjury under the laws of the United States of America that the statements made in the three (3) numbered paragraphs immediately above are true and correct.

EXECUTED on 16 march, 2009 (date)

Print Name: John C. Carson