PATENT ASSIGNMENT

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Simtek Corporation	10/30/2008

RECEIVING PARTY DATA

Name:	Cypress Semiconductor Corporation
Street Address:	198 Champion Court
City:	San Jose
State/Country:	CALIFORNIA
Postal Code:	95134

PROPERTY NUMBERS Total: 8

Property Type	Number
Patent Number:	5563839
Patent Number:	5602776
Patent Number:	5828599
Patent Number:	6026018
Patent Number:	6097629
Patent Number:	6414873
Patent Number:	6512694
Patent Number:	7385857

CH $320.00 5563839

CORRESPONDENCE DATA

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NAME OF SUBMITTER:	Andrew J. Bateman

Total Attachments: 7
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CORPORATE ASSIGNMENT

SIMTEK CORPORATION, a corporation duly organized under and pursuant to the laws of DELAWARE and having its principal place of business at **4250 BUCKINGHAM DRIVE, SUITE 100, COLORADO SPRINGS, COLORADO 80907** (hereafter referred to as the "Assignor"), is the owner by respective assignment of the Issued Patents and Pending Patent Applications set forth in SCHEDULE A, attached hereto (hereafter referred to as the "Patents and Applications").

CYPRESS SEMICONDUCTOR CORPORATION, a corporation duly organized under and pursuant to the laws of DELAWARE and having its principal place of business at **198 CHAMPION COURT, SAN JOSE, CALIFORNIA 95134** (hereafter referred to as the "Assignee"), desires to acquire the entire right, title, and interest in and to the Patents and Applications.

THEREFORE, in consideration of the sum of One Dollar ($1.00) and other good and sufficient consideration, the receipt of which is hereby acknowledged, the Assignor hereby sells, assigns, transfers, and sets over to the Assignee, its successors, legal representatives and assigns the entire right, title and interest in and to the Patents and Applications and all inventions described and claimed therein, the right to file applications on the inventions, and the entire right, title and interest in and to any applications for Letters Patent of the United States or other countries claiming priority to the Patents and Applications, including divisionals, continuations, and continuations-in-part of the Patents and Applications, and reissues, reexaminations, renewals and extensions of the Patents or Letters Patents, and any and all Letters Patent or Patents of the United States of America and all foreign countries that may be granted therefor and thereon, and all rights under the International Convention for the Protection of Industrial Property, the same to be held and enjoyed by the Assignee, for its own use and behalf and the use and behalf of its successors, legal representatives, and assigns, to the full end of the term or terms for which the Patents and Applications have been granted, and for which Letters Patent or Patents may be granted, as fully and entirely as the same would have been held and enjoyed by the Assignor had the present sale and assignment not been made.

By its undersigned representative, the Assignor agrees:

a. to execute all papers necessary in connection with the Patents and Applications and any continuations, continuations-in-part, divisionals, reissues, reexaminations or corresponding applications thereof in any country, and also to execute separate assignments in connection with such application as the Assignee may deem necessary or expedient;

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b. to execute all papers necessary in connection with any interference that may be declared concerning the Patents and Applications or any continuations, continuations-in-part, divisionals, reissues or reexaminations thereof, and to cooperate with the Assignee in every way possible in obtaining evidence and going forward with such interference; and

c. to perform all affirmative acts and take all lawful oaths that may be necessary or required to obtain a grant of a valid patent to the Assignee on the Patents and Applications and on any continuations, continuations-in-part, divisionals, reissues or reexaminations of the Patents and Applications in any country, and for the procurement, maintenance, enforcement, and defense of Letters Patent or Patents for the inventions described and claimed therein, without charge to the Assignee, its successors, legal representatives, and assigns, but at the cost and expense of the Assignee, its successors, legal representatives, and assigns.

The Assignor hereby covenants that, at the time of execution and delivery of the present assignment, the Assignor is the sole and lawful owner of the entire right, title, and interest in and to the inventions set forth in the Patents and Applications identified above, and has the full and complete right, title, and interest to convey the entire interest herein assigned, and that it has not executed, and will not execute, any agreement in conflict therewith.

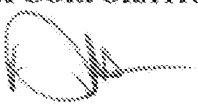
The undersigned has reviewed the documents in the Patents and Applications identified above, and, to the best of undersigned's knowledge and belief, title is in the Assignor identified above.

The undersigned is empowered to sign this assignment on behalf of the Assignor.

I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under Section 1001, Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the Patents and Applications, corresponding applications or any patents issuing thereon.

IN WITNESS WHEREOF, executed by the Assignor's undersigned representative on the date following the undersigned's name.

SIMTEK CORPORATION

By: 

Brian Alleman

Title: Chief Financial Officer

Date: 10/30/08

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ASSIGNMENT
SCHEDULE A

Application No.	Publication No.	Title	Filing Date	Pub. Date
10/598,205	US20080150080	Protective diode for protecting semiconductor switching circuits from electrostatic discharge	11-Sep-07	26-Jun-08
11/615,683	US20080150002	Simultaneous formation of a top oxide layer in a silicon-oxide-nitride-oxide-silicon (SONOS) transistor and a gate oxide in a metal oxide semiconductor (MOS)	22-Dec-06	26-Jun-08
11/644,165	US20080151654	Method and Apparatus to Implement a Reset Function in a Non-Volatile Static Random Access Memory	22-Dec-06	26-Jun-08
11/644,447	US20080151643	Method and apparatus to create an erase disturb on a non-volatile static random access memory cell	22-Dec-06	26-Jun-08
11/644,641	US20080155186	Method and apparatus to program and erase a non-volatile static random access memory from the bit lines	22-Dec-06	26-Jun-08
11/644,789	US20080151624	Combination SRAM and NVSRAM semiconductor memory array	22-Dec-06	26-Jun-08
11/644,819	US20080151616	Method and apparatus to program both sides of a non-volatile static random access memory	22-Dec-06	26-Jun-08
11/647,017	US20080158981	Method and apparatus for on chip sensing of SONOS VT window in non-volatile static random access memory	27-Dec-06	3-Jul-08
11/906,153	N/A	Program memory test access collar	28-Sep-07	N/A
11/999,684	N/A	Combined volatile/non-volatile array	5-Dec-07	N/A
12/006,224	N/A	Dummy cell for memory circuits	31-Dec-07	N/A
12/006,225	N/A	Read and volatile NV standby disturb	31-Dec-07	N/A
12/006,226	N/A	Architecture of NVDRAM array and its sense regime	31-Dec-07	N/A
12/006,227	N/A	3T-high density NVDRAM cell	31-Dec-07	N/A
12/006,228	N/A	Current controlled recall schema	31-Dec-07	N/A

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Application No.	Publication No.	Title	Filing Date	Pub. Date
12/006,270	N/A	5T-High Density NVDRAM cell	31-Dec-07	N/A
60/877,775	N/A	Method and apparatus to power on/off NVSRAM	29-Dec-06	N/A
60/877,933	N/A	Block Protection for NVSRAM	28-Dec-06	N/A
60/877,934	N/A	High to Low Voltage Converter Using High Voltage Transistors	28-Dec-06	N/A
60/919,372	N/A	New recall schema	29-Dec-06	N/A
60/967,508	N/A	Simple and quick retention screening tests by DC bias acceleration at room temperature	4-Sep-07	N/A
60/995,793	N/A	Control circuitry for flexible common or separate control of a number of consumer circuits (NVSRAM store/recall voltage control)	28-Sep-07	N/A

Application No.	Publication No.	Country	Title	Filing Date	Pub. Date
AT20050729533T	AT390710T	Austria	Protective diode for protecting semiconductor switching circuits from electrostatic discharge	16-Feb-05	15-Apr-08
DE20031039343	DE10339343	Germany	Method and arrangement for the production of a memory chip having different data bit widths	4-May-05	25-Aug-03
DE200410008803	DE200410008803	Germany	Protective diode for protecting semiconductor switching circuits from electrostatic discharge	20-Feb-04	27-Oct-05
DE200410042130	DE102004042130	Germany	Circuit arrangement for preparing core voltage from higher working voltage, includes p-channel FET connected between operating voltage terminal and core voltage terminal	28-Apr-05	30-Aug-04
EP20040762556	EP1661138	EPO	Method and arrangement for the production of a memory chip having different data bit widths	31-May-06	30-Jul-04
EP20050729533	EP1719174	EPO	Protective diode for protecting semiconductor switching circuits from electrostatic discharge	16-Feb-05	8-Nov-06
PCT/DE2004/001711	WO2005022542	PCT	Method and arrangement for the production of a memory chip having different data bit widths	10-Mar-05	30-Jul-04
PCT/US90/04555	UNK	PCT	Single ended sense amplifier with improved data recall for variable bit line current	UNK	UNK
WO2005DE00268	WO2005081308	PCT	Protective diode for protecting semiconductor switching circuits from electrostatic discharge	16-Feb-05	1-Sep-05

Patent No.	TITLE	Issue Date
5,013,943	Single ended sense amplifier with improved data recall for variable bit line current	7-May-91
5,055,720	Current mirror sense amplifier with reduced current consumption and enhanced output signal	8-Oct-91
5,065,362	Non-volatile RAM with integrated compact static RAM load configuration	12-Nov-91
5,309,047	Differential sense amplifier with cross connected reference circuits	3-May-94
5,563,839	Semiconductor memory device having a sleep mode	9-Oct-96
5,602,776	Non-volatile, static random access memory with current limiting	11-Feb-97
5,828,599	Memory with electrically erasable and programmable redundancy	27-Oct-98
6,026,018	Non-volatile, static random access memory with store disturb immunity	15-Feb-00
6,097,629	Non-volatile, static random access memory with high speed store capability	1-Aug-00
6,154,311	UV reflective photocatalytic dielectric combiner having indices of refraction greater than 2.0	28-Nov-00
6,163,568	Broadband, low power FM/FSK transceiver for wireless communications systems	19-Dec-00
6,185,124	Storage circuit apparatus	6-Feb-01
6,343,071	Wireless desktop area network system	29-Jan-02
6,346,826	Programmable gate array device	12-Feb-02
6,414,873	nvSRAM with multiple non-volatile memory cells for each SRAM memory cell	2-Jul-02
6,512,694	NAND stack EEPROM with random programming capability	28-Jan-03
7,385,857	Non-volatile, static random access memory with regulated erase saturation and program window	10-Jun-08
DE10052292	Electronic data storage method for semiconductor memory with data memory and electrically-erasable and programmable array-logic coupled to host computer	12-Jan-06

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