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4. Application or patent number(s):	I has document is being thed together with a new oppression.
	B. Patent No.(s)
A. Patent Application No.(s)	B. Patent No.(s)
6016539 6178482 6308254	
04 10000	
5923894 6216218 6505291 5940626 6438679 6677786	
CACTEA1 6327632	
Additional numbers	attached? 💹 Yes 🔀 No
5. Name and address of party to whom correspondence	6. Total number of applications and patents involved: 11
concerning document should be mailed:	
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PATENT REEL: 022973 FRAME: 0706

RELEASE OF SECURITY AGREEMENT COVERING INTERESTS IN PATENTS

Silicon Valley Bank ("Secured Party"), hereby releases its security interest in the interests of Brecis Communications Corporation. ("Assignor") in the patented works set forth in that certain Intellectual Property Security Agreement dated February 27, 2004, executed by Assignor in favor of Secured Party recorded with the United States Department of Commerce, Patent and Trademark Office on February 27, 2004, Reel 015116. Frame(s) 0913.

Date: July 14, 2009

SILICON VALLEY BANK

By: Wargaret Fuj

Title: Operations Manager

PATENT REEL: 022973 FRAME: 0707



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Patent Assignment Details

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Reel/Frame: 015116/0913

Pages: 11

Recorded: 02/27/2004

Conveyance: SECURITY INTEREST (SEE DOCUMENT FOR DETAILS).

Total properties: 11

1 Patent #: 6016539 Issue Dt: 01/18/2000 Application #: 08963345 Filing Dt: 11/03/1997
Title: DATAPATH CONTROL LOGIC FOR PROCESSORS HAVING INSTRUCTION SET ARCHITECTURES IMPLEMENTED

WITH HIERARCHICALLY ORGANIZED PRIMITIVE OPERATIONS

Title: ADAPTABLE INPUT/OUTPUT PIN CONTROL

3 Patent #: 5940626 Issue Dt: 08/17/1999 Application #: 08963387 Filing Dt: 11/03/1997

Title: PROCESSOR HAVING AN INSTRUCTION SET ARCHITECTURE IMPLEMENTED WITH HIERARCHICALLY ORGANIZED

PRIMITIVE OPERATIONS

4 Patent #: <u>6067601</u> Issue Dt: 05/23/2000 Application #: 08963389 Filing Dt: 11/03/1997

Title: CACHE MEMORY BASED INSTRUCTION EXECUTION

5 Patent #: 6178482 Issue Dt 01/23/2001 Application #: 08963391 Filing Dt: 11/03/1997

Title: VIRTUAL REGISTER SETS

6 Patent #: 6216218 Issue Dt: 04/10/2001 Application #: 09120041 Filing Dt: 07/21/1998

Title: PROCESSOR HAVING A DATAPATH AND CONTROL LOGIC CONSTITUTED WITH BASIS EXECUTION BLOCKS

7 Patent #: 6438679 Issue Dt: 08/20/2002 Application #: 09120043 Filing Dt: 07/21/1998

Publication #: US20020053013 Pub Dt: 05/02/2002

Title: MULTIPLE ISA SUPPORT BY A PROCESSOR USING PRIMITIVE OPERATIONS

8 Patent #: 6327632 Issue Dt: 12/04/2001 Application #: 09231942 Filing Dt: 01/14/1999

Title: ADAPTABLE I/O PINS MANIFESTING I/O CHARACTERISTICS RESPONSIVE TO BIT VALUES STORED IN SELECTED ADDRESSABLE STORGE LOCATIONS, EACH PIN COUPLED TO THREE CORRESONDING ADDRESSABLE STORAGE

LOCATIONS

9 Patent #: 6308254 Issue Dt: 10/23/2001 Application #: 09442848 Filing Dt: 11/18/1999

Title: PROCESSING INSTRUCTIONS OF AN INSTRUCTION SET ARCHITECTURE BY EXECUTING HIERARCHICALLY

ORGANIZED SNIPPETS OF ATOMIC UNITS OF PRIMITIVE OPERATIONS

10 Patent #: 6505291 Issue Dt: 01/07/2003 Application #: 09697911 Filing Dt: 10/26/2000 Title: PROCESSOR HAVING A DATAPATH AND CONTROL LOGIC CONSTITUTED WITH BASIS EXECUTION BLOCKS

11 Patent #: 6672786 Issue Dt: 01/13/2004 Application #: 10086500 Filing Dt: 02/28/2002

Publication #: U\$20030042506 Pub Dt: 03/06/2003
Title: MULTI-SERVICE PROCESSOR CLOCKING SYSTEM

Assignor

1 BRECIS COMMUNICATIONS CORPPRATION

Exec Ot: 02/27/2004

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REEL: 022973 FRAME: 0708

Correspondence name and address

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