

PATENT ASSIGNMENT

Electronic Version v1.1  
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT
CONVEYING PARTY DATA	
Name	Execution Date
Crosstek Capital, LLC	08/12/2009
RECEIVING PARTY DATA	
Name:	Chung Cheng Holdings, LLC
Street Address:	2711 Centerville Road, Suite 400
City:	Wilmington
State/Country:	DELAWARE
Postal Code:	19808
PROPERTY NUMBERS Total: 76	
Property Type	Number
Patent Number:	5236076
Patent Number:	5270257
Patent Number:	5304779
Patent Number:	5314298
Patent Number:	5319158
Patent Number:	5480296
Patent Number:	5518963
Patent Number:	5534459
Patent Number:	5572117
Patent Number:	5573974
Patent Number:	5648298
Patent Number:	5668043
Patent Number:	5668064
Patent Number:	5670427
Patent Number:	5679592

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PATENT  
REEL: 023085 FRAME: 0877

Patent Number:	5743695
Patent Number:	5758830
Patent Number:	5759914
Patent Number:	5770474
Patent Number:	5786229
Patent Number:	5789275
Patent Number:	5789287
Patent Number:	6015742
Patent Number:	6020597
Patent Number:	6028000
Patent Number:	6034435
Patent Number:	6080615
Patent Number:	6083833
Patent Number:	6090652
Patent Number:	6127197
Patent Number:	6146999
Patent Number:	6195217
Patent Number:	6204100
Patent Number:	6207495
Patent Number:	6268249
Patent Number:	6278161
Patent Number:	6340541
Patent Number:	6352877
Patent Number:	6372615
Patent Number:	6399986
Patent Number:	6441497
Patent Number:	6593184
Patent Number:	6686289
Patent Number:	6693040
Patent Number:	6720653
Patent Number:	6730528
Patent Number:	6740572
Patent Number:	6743711
Patent Number:	6746911
Patent Number:	6815305

Patent Number:	6818095
Patent Number:	6831007
Patent Number:	6833303
Patent Number:	6845443
Patent Number:	6855600
Patent Number:	6858490
Patent Number:	6869871
Patent Number:	6878617
Patent Number:	6912770
Patent Number:	6913995
Patent Number:	6927142
Patent Number:	6969665
Patent Number:	6977216
Patent Number:	6991992
Patent Number:	7056790
Application Number:	11265852
Application Number:	08581958
Application Number:	07983957
Patent Number:	5858872
Patent Number:	6462565
Patent Number:	6531742
Patent Number:	6544866
Application Number:	10793743
Application Number:	10801407
Patent Number:	5364807
Patent Number:	6566717

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**Total Attachments: 13**

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## EXHIBIT A

### Patents to Be Assigned

Patent No. or Appln. No.	Country	Title	Inventor	Filing Date
KR10-0339433	KR	Metal Layer Of Semiconductor Device And Method For Forming The Same	Yang, Dae Geun	12/30/1999
6,352,877	US	Metal Layer In Semiconductor Device And Method For Fabricating The Same	Yang, Dae Gun	10/26/2000
6,720,653	US	Metal Layer In Semiconductor Device Including A Planar Stuffed Layer And An Insulating Film With A Projection And Method For Fabricating The Same	Yang, Dae Gun	11/15/2001
KR10-0137815	KR	Mosfet Fabrication	Kang, Ho-Young	12/16/1994
5,679,592	US	Process For Formation Of Ldd Mosfet Wing Photoresist	Kang, Ho-Young	12/18/1995
JP3098942	JP	Preparation Of Mos Transistor	Kang, Ho-Young	9/1/1995
KR10-0347138	KR	Method For Processing Data Of Processor	Jin, Seong Ae	12/30/1999
6,845,443	US	Method Of Processing A Repeat Block Efficiently In A Processor Wherein The Repeat Count Is Not Decrementd In A Specific Case To Prevent Error In Execution	Jin, Seong Ae	12/29/2000
KR10-0386622	KR	Method For Forming Dual Damascene Wiring	Kim, Kil Ho	6/27/2001
6,743,711	US	Method For Forming Dual Damascene Line Structure	Kim, Kil Ho	2/5/2002
JP2002-168322	JP	Method For Forming Dual Damascene Wiring	Kim, Kil Ho	6/10/2002
KR10-0538633	KR	Method Of Forming Metal Wiring In Semiconductor Device	Choi, Kyeong Keun	11/13/2003
6,869,871	US	Method Of Forming Metal Line In Semiconductor Device Including Forming First And Second Zirconium Films	Choi, Kyeong Keun	12/23/2003
CN200410056565.8	CN	Method Of Forming Metal Line In Semiconductor Device	Choi, Kyeong Keun	8/10/2004
TW093119264	TW	Method Of Forming Metal Line In Semiconductor Device	Choi, Kyeong Keun	6/30/2004
JP2004-234089	JP	Method For Forming Metal Wiring For Semiconductor Device	Choi, Kyeong Keun	8/11/2004
KR10-0538380	KR	Method Of Forming Metal Wiring In Semiconductor Device	Kim, Hyung Jun	11/13/2003
JP2004-190770	JP	Method Of Forming Metal Wiring Of Semiconductor Device	Kim, Hyung-Joon	6/29/2004
6,977,216	US	Method For Forming Metal Wire In Semiconductor Device	Kim, Hyung Jun	6/29/2004
CN200410056569.6	CN	Method For Forming Metal Wire In Semiconductor Device	Kim, Hyung Jun	8/10/2004
KR10-0407998	KR	METHOD OF CLEANING CONTACT REGION OF METALLIC WIRE	Kim, Dong Joon	10/09/2001
6,693,040	US	METHOD FOR CLEANING THE CONTACT AREA OF A METAL LINE	Kim, Dong Joon	4/11/2002
JP4109061	JP	METHOD OF WASHING CONTACT REGION OF METAL WIRING	Kim, Dong Joon	09/10/2002

Patent No. or Appln. No.	Country	Title	Inventor	Filing Date
KR10-0537552	KR	Semiconductor Device And Method Of Manufacturing The Same	Han, IL-Seok	7/31/2000
6,593,184	US	Semiconductor device with stacked memory and logic substrates and method for fabricating the same	Han, IL-Suk	7/27/2001
JP2001-229163	JP	Semiconductor Element And Its Manufacturing Method	Han, IL-Suk	7/30/2001
6,746,911	US	Semiconductor Device With Stacked Memory And Logic Substrates And Method For Fabricating The Same	Han, IL-Suk	5/22/2003
KR10-0523138	KR	Method For Manufacturing Inductor In Semiconductor Device	Kim, Young Keun	8/12/2003
6,991,992	US	Method For Forming Inductor In Semiconductor Device	Kim, Young Keun	6/28/2004
KR10-0504194	KR	DRAM cell including MOS capacitor and method formanufacturing the same	Kim, Hak-Yun	12/16/2002
JP2003-415912	JP	DRAM Cell Having MOS Capacitor And Manufacturing Method Therefor	Kim, Hak-Yun	12/15/2003
TW092135540	TW	DRAM CELL HAVING MOS CAPACITOR AND METHOD FOR MANUFACTURING THE SAME	Kim, Hak-Yun	12/16/2003
7,056,790	US	DRAM Cell Having MOS Capacitor And Method For Manufacturing The Same	Kim, Hak-yun	12/16/2003
11/265,852	US	DRAM Cell Having MOS Capacitor	Kim, Hak-yun	11/3/2005
KR20-1995-0024230	KR	Hard Disk Equipped With A Memory For Storing File Allocation Table Information	Park, Jeong Joo	9/6/1995
08/581,958	US	Hard Disk Equipped With A Memory For Storing File Allocation Table Information	Park, Jeong Joo	1/2/1996
JPH08-000927	JP	Hard Disk Equipped With A Memory For Storing File Allocation Table Information	Park, Jeong Joo	1/8/1996
TW109339	TW	Hard Disk Drive Equipped With FAT Memory	Park, Jeong Joo	12/23/1995
6,195,217	US	Hard Disk Equipped With A Memory For Storing File Allocation Table (FAT) Information	Park, Jeong Joo	5/22/1998
KR20-0088084	KR	Apparatus For Automatically Unloading Device In Handler	Song, Yong-Kyu	9/13/1991
5,236,076	US	Apparatus For Automatically Unloading Device In Handler	Sung, Yong G.	9/8/1992
DE4230175	DE	Testing And Sorting Device For Electronic Components, e.g. IC Chips - Simultaneously Controls Blocking Pins For Several Channels Of Multi-Channel Component Discharge System	Sung, Yong Gyoo	9/9/1992
TW082237	TW	Apparatus For Automatically Unloading Device In Handler	Sung, Yong Gyoo	1992/8/28
JP2788381	JP	Automatic Device Delivery Device For Handler	Sung, Yong Gyoo	4/9/1992
KR10-1991-0007881	KR	Manufacturing Method Of Semiconductor Device Having Recess Gate	Sin, Hyung-Soon	5/15/1991
5,270,257	US	Method Of Making Metal Oxide Semiconductor Field Effect Transistors With A Lightly Doped Drain Structure Having A Recess Type Gate	Shin, Hyung S.	5/15/1992

Patent No. or Appln. No.	Country	Title	Inventor	Filing Date
DE4212829	DE	Method Of Making Metal Oxide Semiconductor Field Effect Transistors With A Lightly Doped Drain Structure Having A Recess Type Gate	Shin, Hyung S.	4/16/1992
TW057479	TW	Method Of Making Metal Oxide Semiconductor Field Effect Transistors With A Lightly Doped Drain Structure Having A Recess Type Gate	Shin, Hyung S.	1/6/1992
JP2826924	JP	Method Of Making Metal Oxide Semiconductor Field Effect Transistors With A Lightly Doped Drain Structure Having A Recess Type Gate	Shin, Hyung S.	3/4/1992
KR10-0085742	KR	Heating System For Instruments Measuring Performance Of Semiconductor Devices	Seong, Yong-Gyu	5/13/1991
5,304,779	US	Semiconductor Preheater With Inclined Rotary Feed	Sung, Yong G.	5/11/1992
DE4216487	DE	Semiconductor Preheater With Inclined Rotary Feed	Sung, Yong Gyoo	5/12/1992
TW058872	TW	Semiconductor Preheater With Inclined Rotary Feed	Sung, Yong Gyoo	5/12/1992
JP3305751	JP	Semiconductor Preheater With Inclined Rotary Feed	Sung, Yong Gyu	5/13/1992
KR10-0076462	KR	Automatic Lead Frame Feeder For To-220 Semiconductor Manufacturer	Kim, Yeol	5/23/1991
5,314,298	US	Automatic Lead Frame Feeding Device For A TO-220 Semiconductor Manufacturing Apparatus	Kim, Youl	5/22/1992
DE4217085	DE	Automatic Conductor Frame Feeding Device For Transistor Outline Semiconductor MFG - Has Successive Loading, Transfer And Feeding Sections And Does Not Require Separate Storage Magazine	Kim, Youl	5/22/1992
TW058431	TW	Automatic Lead Frame Feeding Device For A TO-220 Semiconductor Manufacturing Apparatus	Kim, Youl	5/15/1992
JP2991857	JP	Lead-Frame Automatic Feeder For To-220 Semiconductor Manufacturing Machine	Kim, Youl	5/22/1992
KR10-0080304	KR	Semiconductor Device Integrated With Coil	Lee, Gyeong-Su ; Kim, Hong-Sik	7/11/1991
5,319,158	US	Coil integrated Semi-Conductor Device And Method Of Making The Same	Lee, Kyung S. ; Kim, Heung S.	7/10/1992
DE4222791.7	DE	Coil With Metallic Core Integrated In Semiconductor Device - Uses 3 Metallisation Layers Which Are Selectively Interconnected	Lee, Kyung Su ; Kim, Heung Sik	7/10/1992
TW075570	TW	Coil integrated Semi-Conductor Device And Method Of Making The Same	Lee, Kyung Su ; Kim, Heung Sik	7/3/1992
JP3338897	JP	Coil integrated Semi-Conductor Device And Method Of Making The Same	Lee, Kyung Su ; Kim, Heung Sik	7/13/1992
KR20-1992-0002222	KR	Transfer Molding Die	Jang, Keun Y.	2/15/1992
07/983,957	US	Transfer Molding Die	Jang, Keun Y.	12/1/1992
5,480,296	US	Transfer Molding Apparatus For Encapsulating An Electrical Element In Resin	Jang, Keun Y.	6/22/1994
JP2583480	JP	Transfer Molding Die	Jang, Keun Y.	12/8/1992

Patent No. or Appln. No.	Country	Title	Inventor	Filing Date
KR10-0120497	KR	Method Of Forming Metal Line Of Semiconductor Device	Park, Sang Hoon	7/7/1994
5,518,963	US	Method For Forming Metal Interconnection Of Semiconductor Device	Park, Sang H.	7/7/1995
ZL95109442.4	CN	Method For Forming Metal Interconnection Of Semiconductor Device	Park, Sang Hoon	7/7/1995
KR10-1994-0013740	KR	Method For Manufacturing Silicon-On-Insulator Structure	Kim, Seong Su	6/17/1994
5,534,459	US	Method For Forming Silicon On Insulator Structured	Kim, Sung S.	6/7/1995
JP2660682	JP	Preparation Of Silicon On Insulator (SOI)	Kim, Sung Su	7/6/1995
KR10-0094958	KR	Multi-Meter	Yun, Hee-Yong	9/16/1993
5,572,117	US	Multi-Meter	Yoon, Hee Y.	9/13/1994
JP3526917	JP	Multi-Meter	Yoon, Hee Yong	9/14/1994
KR10-0161112	KR	Method For Isolating Semiconductor Devices	Hwang, Hyun Sang	1/11/1995
5,573,974	US	Method For Isolating Semiconductor Elements	Hwang, Hyunsang	5/16/1995
JP2875972	JP	Method For Isolating Semiconductor Elements	Hwang, Hyun Sang	8/30/1995
KR10-0144227	KR	Method For Forming Contact OF Semiconductor Devices	Cho, Gyung Su	3/4/1995
KR10-0148326	KR	Method For Fabricating Semiconductor Device	Choe, Jae Seong ; Jo, Gyung Su	3/4/1995
TW084277	TW	Method For Forming A Contact In A Semiconductor Device	Cho, Gyun-Su	3/4/1996
ZL96104049.1	CN	Methods For Forming Contact In Semiconductor Device	Cho, Gyun-Su	3/4/1996
5,648,298	US	Methods For Forming A Contact In A Semiconductor Device	Cho, Gyung-Su	3/4/1996
KR10-0190367	KR	Method For Forming Isolation Layer Of Semiconductor Device	Park, Sang Hun	2/24/1995
5,668,043	US	Method For Forming Isolated Regions In A Semiconductor Device	Park, Sang Hoon	2/22/1996
ZL96101498.9	CN	Method For Forming Isolated Regions In A Semiconductor Device	Park, Sang Hoon	2/24/1996
TW085206	TW	Method For Forming Isolated Regions In A Semiconductor Device	Park, Sang Hoon	2/24/1996
JP2788889	JP	Separate Formation In Semiconductor Device	Park, Sang Hoon	2/26/1996
KR10-0187666	KR	Method For Forming Tungsten Plug Of Semiconductor Device	Kim, Dong Seok ; Lee, Ju Il ; Park, Sang Hun	2/24/1995
TW099799	TW	Method of forming a tungsten plug in a semiconductor device	Park, Sang Hoon ; Kim, Dong Sauk ; Lee, Ju Il	2/23/1996
5,668,064	US	Method Of Forming A Tungsten Plug In A Semiconductor Device	Park, Sang Hoon ; Kim, Dong Sauk ; Lee, Ju Il	2/23/1996
ZL96105584.7	CN	Method Of Forming A Tungsten Plug In A Semiconductor Device	Park, Sang Hoon ; Kim, Dong Sauk ; Lee, Ju Il	2/24/1996
KR10-0172255	KR	Method For Forming Metal Wiring Of Semiconductor Device	Cho, Gyeong Su	3/4/1995



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5,670,427	US	Method For Forming Metal Contacts In Semiconductor Devices	Cho, Gyung-Su	3/4/1996
DE19608211	DE	Method For Forming Metal Contacts In Semiconductor Devices	Cho, Gyung-Su	3/4/1996
TW084276	TW	Method For Forming Metal Contacts In Semiconductor Devices	Cho, Gyung-Su	3/4/1996
GB2298738	GB	Method For Forming Metal Contacts In Semiconductor Devices	Cho, Gyung-Su	3/4/1996
KR10-0147403	KR	Device Of Automatic Chip Loading	Yu, Do-Hyun ; Lim, Byung-Taek ; Choe, Won-Wook ; Jang, Inn-Kwon ; Kim, Won-Nam	6/24/1994
5,743,695	US	Automatic Chip-Loading Apparatus	Ryu, Do Hyun	6/23/1995
ZL95109131.X	CN	Automatic Chip-Loading Apparatus	Ryu, Do Hyun	6/24/1995
JP2808259	JP	Chip Automatic Loading Device	Ryu, Do Hyun	6/26/1995
KR10-0141942	KR	Controller For Photoresist Supplying Quantity	Kim, Myung-Ho	11/3/1994
5,758,830	US	Apparatus For Controlling Supply Amount Of Photoresist	Kim, Myoung Ho	10/31/1995
JP2839863	JP	Jet Solution Adjustment Device Of Photoregister	Kim, Myoung Ho	11/2/1995
KR10-0185298	KR	Forming Method Of Plug For Contact Hole	Park, Sang-Hoon	12/30/1995
5,759,914	US	Method For Forming Interconnection In Semiconductor Device	Park, Sang-Hoon	12/11/1996
DE19653614	DE	Connection Or Interconnection Formation Method For Semiconductor Component	Park, Sang-Hoon	12/20/1996
JP2916905	JP	Wiring Formattion Of Semiconductor Element	Park, Sang-Hoon	12/24/1996
GB2309824	GB	Forming Interconnections In Semiconductor Devices	Park, Sang-Hoon	12/27/1996
KR10-0203307	KR	Method Of Manufacturing Laser Diode	Kim, Ang-Seok	6/29/1996
JPH09-180663	JP	Manufacture Of Laser Diode	Kim, Ang-Seo	6/20/1997
5,770,474	US	Method Of Fabricating Laser Diode	Kim, Ang-Seo	6/25/1997
KR10-0167599	KR	Element Isolation Method Of Semiconductor Apparatus	Park, Sang-Hun	12/30/1994
KR10-0140655	KR	Device Isolation Method Of Semiconductor Apparatus	Pak, Sang-Hun	12/30/1994
JP2686735	JP	Element Separation Method Of Semiconductor Device	Park, Sang-Hoon	12/20/1995
5,786,229	US	Method For Providing Isolation Between Semiconductor Devices Using Epitaxial Growth And Polishing	Park, Sang-Hoon	12/28/1995
DE19549155	DE	Method Of Separating Two Semiconductor Devices	Park, Sang-Hoon	12/29/1995
TW082088	TW	Method For Providing Isolation Between Semiconductor Devices	Park, Sang-Hoon	12/23/1995
ZL95118829.1	CN	Method For Providing Isolation Between Semiconductor Devices	Park, Sang-Hoon	12/30/1995
KR10-1995-0066039	KR	Method For Fabricating A Laser Diode	Lee, Soo Won ; Cho, Gyu Seog ; Kim, Tae Jin ; Oh, Kyung Seok	12/29/1995

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5,789,275	US	Method For Fabricating A Laser Diode	Lee, Soo Won ; Cho, Gyu Seog ; Kim, Tae Jin ; Oh, Kyung Seok	11/26/1996
JP2828628	JP	Fabrication Of Laser Diode	Lee, Soo Won ; Cho, Gyu Seog ; Kim, Tae Jin ; Oh, Kyung Seok	12/26/1996
KR10-0146528	KR	Method For Manufacturing Semiconductor Device	Lee, Chang-Kwon	4/11/1995
5,789,287	US	Method Of Forming Field Isolation In Manufacturing A Semiconductor Device	Lee, Chang Kwon	4/10/1996
TW092137	TW	A Field Isolation Method In Semiconductor Devices	Lee, Chang Kwon	4/11/1996
ZL96107230.X	CN	Method Of Manufacturing Semiconductor Device	Lee, Chang Kwon	4/11/1996
KR10-0268906	KR	Method For Forming Inductor Of Semiconductor Device	Ju, Jae-II	9/29/1997
6,015,742	US	Method For Fabricating Inductor Of Semiconductor Device	Ju, Jae II	4/2/1998
JP3015781	JP	Manufacture Of Inductor For Semiconductor Device	Ju, Jae II	6/26/1998
DE19830161	DE	Induction Coil Integration Process For A Semiconductor Device Esecially An ULSI Chip	Ju, Jae II	7/6/1998
KR10-0214560	KR	Semiconductor Multi Chip Module	Kwak, Duk-Joo	3/5/1997
DE19806017	DE	Semiconducting Multi-Chip Module	Kwak, Duk Joo	2/13/1998
JP2847516	JP	Semiconductor Multi-Chip Module	Kwak, Duk Joo	3/2/1998
6,020,597	US	A Repairable Multichip Module	Kwak, Duk Joo	3/4/1998
KR10-0214852	KR	Forming Method For Metal Wiring In Semiconductor Device	Cho, Kyong-Soo	11/2/1996
6,028,000	US	Method Of Forming Contact Plugs In Semiconductor Device Having Different Sized Contact Holes	Cho, Gyung-Su	10/30/1997
TW119581	TW	Method Of Forming Contact Plugs In Semiconductor Device Having Different Sized Contact Holes	Cho, Gyung-Su	10/30/1997
JP3182608	JP	Method Of Forming Contact Plugs Of Semiconductor Device Having Contact Holes Different In Size	Cho, Gyung-Su	10/31/1997
KR10-0171069	KR	Method Of Forming Metal Contact Of Semiconductor Device	Kim, Hyun-Sook	10/27/1994
JP3510939	JP	Formation Method And Structure For Metal-Interconnection Contact Part In Semiconductor Device	Kim, Hyun Sook	8/2/1995
5,858,872	US	Metal Contact Structure In Semiconductor Device, And A Method Of Forming The Same	Kim, Hyun Sook	8/4/1995
6,034,435	US	Metal Contact Structure In Semiconductor Device	Kim, Hyun Sook	9/30/1998
KR10-0198663	KR	Forming Method Of IC For Communication	Lee, Chang-Jae ; Kim, Jun-Ki	3/17/1997
6,080,615	US	Method For Forming A Semiconductor Device Incorporating A Dummy Gate Electrode	Lee, Chang-Jae ; Kim, Jun-Ki	1/5/1998

Patent No. or Appln. No.	Country	Title	Inventor	Filing Date
JP3740272	JP	Manufacture Of IC For Communication Device	Lee, Chang Jae ; Kim, Jun Ki	3/17/1998
KR10-0244484	KR	Method For Fabricating A Semiconductor Device	An, Min-Soo	7/2/1997
6,083,833	US	Method For Forming Conductive Film For Semiconductor Device	Ahn, Min Su	6/16/1998
JPH10-175610	JP	Formation Of Conductive Film	An, Min-Soo	6/23/1998
KR10-0220252	KR	Method Of Manufacturing Semiconductor Device	Kim, Jae-Gap	12/28/1996
6,090,652	US	Method Of Manufacturing A Semiconductor Device Including Implanting Threshold Voltage Adjustment Lons	Kim, Jae-Kap	12/22/1997
TW102256	TW	Manufacturing Method Of A Semiconductor Device	Kim, Jae Kap	11/19/1997
JP2964232	JP	Manufacture Of Semiconductor Device	Kim, Jae-Kap	12/25/1997
KR10-0272659	KR	Pattern For Measuring Line Width Of A Metal Line Of A Semiconductor Device And Method For Measuring The Same	Kim, Gil Ho ; Shin, Gang Sup ; Kim, Jong Il	6/28/1997
TW110327	TW	Measuring-Pattern And Measuring Method For Width Of Wire In Semiconductor Device	Kim, Kil-Ho ; Shin, Kang-Sup ; Kim, Jong-II	6/22/1998
GB2326721	GB	Wire Width Measurement	Kim, Kil Ho ; Shin, Kang Sup ; Kim, Jong Il	6/24/1998
6,127,197	US	Method For Measuring Width Of Wire In Semiconductor Device Using Measuring-Pattern	Kim, Kil Ho ; Shin, Kang Sup ; Kim, Jong Il	6/25/1998
6,462,565	US	Measuring Pattern For Measuring Width Of Wire In Semiconductor Device	Kim, Kil Ho ; Shin, Kang Sup ; Kim, Jong Il	8/24/2000
JP3636600	JP	Line Width Measurement For Wiring Pattern Of Semiconductor Element And Line Width Measuring Method Using The Same	Kim, Kil Ho ; Shin, Kang Sup ; Kim, Jong Il	6/26/1998
KR10-0236076	KR	Method For Forming Metal Wiring In Semiconductor Device	Kang, Dong-Man ; Kang, Jung-Ho	8/14/1997
6,146,999	US	Method For Forming Metal Line Of Semiconductor Device	Kang, Dong Man ; Kang, Jung Ho	10/23/1997
JP2942231	JP	Method For Forming Wiring Of Semiconductor Element	Kang, Dong Man ; Kang, Jung Ho	1/22/1998
KR10-0331844	KR	Complementary Metal Oxide Semiconductor Device	Kim, Sang Yeon	2/12/1998
ZL98123955.2	CN	CMOS Device And Method For Fabricating The Same	Kim, Sang Yeon	11/6/1998
6,204,100	US	CMOS Device And Method For Fabricating The Same	Kim, Sang Yeon	2/12/1999
6,531,742	US	Method Of Forming CMOS Device	Kim, Sang Yeon	12/26/2000
KR10-0309644	KR	Method For Fabricating Capacitor	Choi, Seong Uk	8/23/1999
6,207,495	US	Method Of Fabricating Capacitors	Choi, Sung-Wook	8/11/2000

Patent No. or Appln. No.	Country	Title	Inventor	Filing Date
KR10-0292056	KR	Semiconductor Device And Method For Fabricating The Same	Ha, Jong-Bong	9/14/1998
DE19931916.2	DE	Single Chip Semiconductor Component With Different Gate Oxide Thicknesses, Useful For Multimedia Systems, Has Vertical Channel Regions, Impurity Regions Overlapping At A Trench Bottom And Transistor Gates Buried In Trenches	Ha, Jong-Bong	7/8/1999
6,268,249	US	Semiconductor Device And Method Of Fabricating The Same	Ha, Jong-Bong	8/6/1999
6,399,986	US	Semiconductor Device And Method Of Fabricating The Same	Ha, Jong-Bong	6/28/2001
KR10-0319610	KR	Transistor Of Semiconductor Device And Method Thereof	Baek, Yeong Geum ; Jung, Yeon U	3/18/1999
6,278,161	US	Transistor	Back, Young-Kum ; Cheong, Yeon-Woo	8/13/1999
6,372,615	US	MOSFET And Fabrication Method Thereof	Back, Young-Kum ; Cheong, Yeon-Woo	6/4/2001
KR10-0253381	KR	Recycling Mask And Method For Manufacturing And Recycling The Same	Yoo, Seung Seok	12/17/1997
TW110176	TW	Mask For Recycling And Fabrication Method Thereof	Yoo, Seung Seok	5/6/1998
GB2332534	GB	A Mask For Fabricating A Semiconductor Device And Method Thereof	Yoo, Seung Seok	11/9/1998
6,340,541	US	Mask For Recycling And Fabrication Method Thereof	Yoo, Seung Seok	8/26/1998
KR10-0384834	KR	Semiconductor Device Formed On Multiple Substrate And Fabricating Method Thereof	Han, Il Seok	3/30/2001
6,441,497	US	Semiconductor Device Fabricated On Multiple Substrates And Method For Fabricating The Same	Han, Il-Seok	10/16/2001
6,544,866	US	Semiconductor Device Fabricated On Multiple Substrate	Han, Il-Seok	5/31/2002
KR10-0393976	KR	Method For Minimizing Change In Etching Rate Of Semiconductor Wafer Depending On Mask Pattern Density	Baek, Gye Hyeon	6/9/2001
JP2001-381103	JP	Method For Minimizing Change In Etching Rate Of Semiconductor Wafer	Bae, Kil Hyun	12/14/2001
6,686,289	US	Method For Minimizing Variation In Etch Rate Of Semiconductor Wafer Caused By Variation In Mask Pattern Density	Baek, Kye Hyun	1/9/2002
KR10-0223272	KR	Overlap Measuring Marks And Method For Compensating Overlap Using The Same	Park, Gi Yeop	12/28/1996
6,730,528	US	Mask Set For Measuring An Overlapping Error And Method Of Measuring An Overlapping Error Using The Same	Park, Ki Yeop	12/22/1997
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Patent No. or Appln. No.	Country	Title	Inventor	Filing Date
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6,740,572	US	Method For Fabricating CMOS Transistor Of A Semiconductor Device	Cha, Jae-Han	12/30/2002
KR10-0487412	KR	Method For Fabricating Semiconductor Devices	Cha, Jae Han	9/24/2002
6,815,305	US	Method For Fabricating BICMOS Semiconductor Devices	Cha, Jae Han	12/13/2002
KR10-0504941	KR	DistributionApparatus for chemical mechanical polishing	Kim, Hyeong Jun	5/9/2003
6,818,095	US	Chemical Mechanical Polishing Apparatus	Kim, Hyung Jun	11/24/2003
JP2003-390731	JP	Chemical Mechanical Polishing Device	Kim, Hyung Jun	11/20/2003
KR10-0374228	KR	Method For Forming Metal Interconnection	Kim, Gil Ho	3/28/2001
6,831,007	US	Method For Forming Metal Line Of Al/Cu Structure	Kim, Kil Ho	3/14/2002
KR10-0449251	KR	Method For Forming Semiconductor Device	Jung, Eun-Yeong	7/12/2002
6,833,303	US	Method For Forming Semiconductor Device	Chung, Eun-Young	7/8/2003
KR10-0449253	KR	Method For Manufacture The Capacitor	Park, Won-Gyu	7/16/2002
JP2002-381168	JP	Method Of Manufacturing Capacitor	Park, Won-Kyu	12/27/2002
6,855,600	US	Method For Manufacturing Capacitor	Park, Won-kyu	3/5/2003
KR10-0505390	KR	Method For Manufacturing Merged DRAM And Logic Device	Kim, Hyeong Sik	12/26/2002
6,858,490	US	Method For Manufacturing Merged DRAM With Logic Device	Kim, Hyung Sik	6/30/2003
JP2003-270806	JP	Method For Manufacturing Merged DRAM With Logic Device	Kim, Hyung Sik	7/3/2003
KR10-0480891	KR	Method For Forming Copper Line in Semiconductor Device	Lee, Byeong Ju ; Kim, Hyeon Yong	5/16/2002
6,878,617	US	Method Of Forming Copper Wire On Semiconductor Device	Lee, Byung Zu ; Kim, Hyun Yong	12/30/2002
TW091137968	TW	METHOD OF FORMING COPPER WIRE ON SEMICONDUCTOR DEVICE	Lee, Byung Zu ; Kim, Hyun Yong	12/31/2002
CN03101493.3	CN	Method Of Forming Copper Wire On Semiconductor Module	Lee, Byung Choo ; Kim, Hyon Lyong	1/22/2003
KR10-0447971	KR	Method For Fabricating Magnetic Sensor Of Multilayered Structure	Lee, Deok Won ; Kim, Dong Jun	12/18/2001
6,912,770	US	Method For Fabricating Magnetic Field Sensor	Lee, Dok Won ; Kim, Dong Joon	12/11/2002
KR10-0465058	KR	Method Of Forming A Barrier Metal In A Semiconductor Device	Ko, Chang Jin	12/26/2002
6,913,995	US	Method Of Forming A Barrier Metal In A Semiconductor Device	Ko, Chang Jin	7/14/2003
TW092119123	TW	METHOD OF FORMING A BARRIER METAL IN A SEMICONDUCTOR DEVICE	Ko, Chang Jin	7/14/2003
CN200310123508.2	CN	Method Of Forming Barrier Metal In Semiconductor Device	Ko, Chang Jin	12/24/2003
KR10-0532937	KR	Method Of Forming Capacitor Of Semiconductor Device	Lee, Joon Hyeon ; Han, Seung Hee	7/15/2003
TW092131158	TW	METHOD FOR FABRICATING CAPACITOR IN SEMICONDUCTOR DEVICE	Lee, Joon Hyeon ;	11/7/2003

Patent No. or Appin. No.	Country	Title	Inventor	Filing Date
6,927,142	US	Method For Fabricating Capacitor In Semiconductor Device	Han, Seung Hee Lee, Joon Hyeon ; Han, Seung Hee	11/10/2003
KR10-0474859	KR	Method Of Forming An Isolation Layer In A Semiconductor Device	Cha, Jae Han	11/5/2002
6,969,665	US	Method Of Forming An Isolation Film In A Semiconductor Device	Cha, Jae Han	7/3/2003
KR10-0504204	KR	Method For Manufacturing Bipolar Transistor Using CMOS Process	Hong, Dae Uk	4/1/2003
10/801,407	US	Method For Manufacturing A Bipolar Transistor Using A CMOS Process	Hong, Dae-Wook	3/16/2004
JP2004-099707	JP	Manufacturing Method Of Bipolar Transistor Using CMOS Process	Hong, Dae-Wook	3/30/2004
CN200410032153.0	CN	Method Of Manufacturing Bipolar Transistor Using Complementary Metallic Oxide Semiconductor Technology	Hong, Dae-Wook	2004/4/1
TW093109000	TW	Method For Manufacturing A Bipolar Transistor By Using A CMOS Process	Hong, Dae-Wook	4/1/2004
KR10-0112316	KR	Method Of Manufacturing Transistor	Hwang, Hyun-Sang	5/14/1993
5,364,807	US	Method For Fabricating LDD Transistor Utilizing Halo Implant	Hwang, Hyun-Sang	10/12/1993
JP3640406	JP	Manufacture Of Transistor	Hwang, Hyun-Sang	11/17/1993
DE4344285	DE	Method For Fabricating LDD Transistor Utilizing Halo Implant	Hwang, Hyun-Sang	12/23/1993
KR10-0369361	KR	Integrated Circuit With Silicide Electro Static Discharge Protection Transistor	Jung, Jong-Chuck	3/30/2001
6,566,717	US	Integrated Circuit With Silicided ESD Protection Transistors	Jung, Jong-Chuck	9/7/2001
JP2001-273668	JP	Silicide Static Discharge Protective Circuit, Semiconductor Integrated Circuit And Silicide Static Discharge Protective Circuit Therefor	Jung, Jong-Chuck	9/10/2001
TW183613	TW	Integrated Circuit With Silicided ESD Protection Transistors	Jung, Jong-Chuck	1/15/2002
DE10211133.2	DE	Integrated Circuit With Silicided ESD Protection Transistors	Jung, Jong-Chuck	3/14/2002

## EXHIBIT B

### ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, Crosstek Capital, LLC, a limited liability company duly organized and existing under the laws of the State of Delaware, United States of America with an office at 2711 Centerville Road, Suite 400, Wilmington, DE 19808, U.S.A. ("**Assignor**"), does hereby sell, assign, transfer, and convey unto Chung Cheng Holdings, LLC, a limited liability company duly organized and existing under the laws of the State of Delaware, United States of America with an office at 2711 Centerville Road, Suite 400, Wilmington, DE 19808 ("**Assignee**"), or its designees, all right, title, and interest that exist today and may exist in the future in and to all of the following (collectively, the "**Patent Rights**"), including:

(a) the provisional patent applications, patent applications and patents listed in the attached Exhibit A to the Patent Purchase Agreement between Assignor and Assignee dated August 12, 2009 ("**Listed Patents**"),

(b) all patents or patent applications (i) to which any of the foregoing claim priority directly or indirectly, and (ii) for which any of the foregoing directly or indirectly forms a basis for priority, and (iii) that are reissues, reexaminations, extensions, continuations, continuations in part, continuing prosecution applications, or divisions of any of the foregoing, and/or (iv) that are foreign patents, patent applications and counterparts to any of the foregoing, including certificates of invention, utility models, industrial design protection, design patent protection, and other governmental grants or issuances and (v) any of the foregoing in (i)-(iv) whether or not expressly listed as Listed Patents below and whether or not abandoned, rejected, or the like;

(c) inventions, invention disclosures, and discoveries described in any of the Listed Patents and /or any of the foregoing category (b) to the extent that any such inventions, invention disclosures, and discoveries (i) are included in any claim in the Listed Patents and /or any of the foregoing category (b), (ii) are subject matter capable of being reduced to a patent claim in any reissue or reexamination proceedings brought on any of the Listed Patents and /or any of the foregoing category (b), and/or (iii) could have been and/or could be included as a claim in any continuations, continuations in part, continuing prosecution applications, requests for continuing examinations and/or divisions of the Listed Patents and /or any of the foregoing category (b);

(d) rights to apply in any or all countries of the world for patents, certificates of invention, utility models, industrial design protections, design patent protections or other governmental grants or issuances of any type related to the any of the foregoing categories (a), (b) and/or (c), including, without limitation, under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement or understanding;

(e) causes of action (whether currently pending, filed, or otherwise) and other enforcement rights, including, without limitation, all rights under the Listed Patents and/or under or on account of any of the foregoing categories (b), (c) and/or (d) to

- (i) damages,
- (ii) injunctive relief and
- (iii) other remedies of any kind

for past, current and future infringement; and

(f) all rights to collect royalties and other payments under or on account of any of the Listed Patents or any of the foregoing categories (b) through (e).

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

The terms and conditions of this Assignment of Patent Rights will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.



IN WITNESS WHEREOF this Assignment of Patent Rights is executed at Taipei, Taiwan on August 12, 2009.

ASSIGNOR

CROSSTEK CAPITAL, LLC

By: 

Name: Guy L. Proulx

Title: Managing Director

*(Signature MUST be attested)*

#### ATTESTATION OF SIGNATURE

The undersigned witnessed the signature of Guy L. Proulx to the above Assignment of Patent Rights on behalf of Crosstek Capital, LLC and makes the following statements:

1. I am over the age of 18 and competent to testify as to the facts in this Attestation block if called upon to do so.
2. Guy L. Proulx is personally known to me (or proved to me on the basis of satisfactory evidence) and appeared before me on August 12, 2009 to execute the above Assignment of Patent Rights on behalf of Crosstek Capital, LLC.
3. Guy L. Proulx subscribed to the above Assignment of Patent Rights on behalf of Crosstek Capital, LLC.

I declare that the statements made in the three (3) numbered paragraphs immediately above are true and correct.

EXECUTED on August 12, 2009 (date)

By: 

Print Name: Rebecca Tu