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U.S. DEPARTMENT OF COMMERCE
United States Patent and Trademark

ORDATION FORM COVER SHEET

PATENTS ONLY

To the Director of the U.S. Patent and Trademark Office: Please record the attached documents or the new address(es) below.

1. Name of conveying party(ies):
Unity Semiconductor Corporation
255 Santa Ana Court
Sunnyvale, CA 94085
Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies):
Name: **Gold Hill Capital**
Internal Address:
Street Address: **One Almaden Blvd. Suite 630**
City: **Sunnyvale**
State: **CA**
Country: USA Zip: **95113**
Additional name(s) & address(es) attached? ☒ Yes ☐ No

3. Nature of conveyance/Execution Date(s):
Execution Date: **April 7, 2009**
☐ Assignment ☐ Merger
☒ **Security Agreement** ☐ Change of Name
☐ Joint Research Agreement
☐ Government Interest Assignment
☐ Executive Order 9424, Confirmatory License
☐ Other _____

4. Application or patent number(s):
☐ This document is being filed together with a new application.

A. Patent Application No.(s)	B. Patent No.(s)
	Please See Exhibit A

Additional numbers attached? ☐ Yes ☒ No

5. Name and address of party to whom correspondence concerning document should be mailed:
Name: **UCC Direct Services**
Internal Address: **Attn: 14080632**
Street Address: **187 Wolf Road, Suite 101**
City: **Albany**
State: **NY** Zip: **12205**
Phone Number: **1-800-342-3676 X 4065**
Fax Number: **800-962-7049**
Email Address: **Cls-Udsalbany@wolterskluwer.com**

6. Total number of applications and patents involved: 138

7. Total fee (37 CFR 1.21 (h) & 3.41) **$ 5,520.00**
☒ Authorized to be charged by credit card fee Paid
☐ Authorized to be charged to deposit account
☐ Enclosed
☐ None required (government interest not affecting title)

8. Payment Information
a. Credit Card Last 4 Numbers
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9. Signature: Joseph D Boryman 4/8/09
Signature Date
Joseph D Boryman
Name of Person Signing
Total number of pages including cover sheet, attachments, and documents:

Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to:
Mail Stop Assignment Recordation Services, Director of the USPTO, P.O. Box 1450, Alexandria, V.A. 22313-1450

Intellectual Property Schedule

Patents

Title		Issue Date	Patent No.
Cross Point Memory Array Using Multiple Thin Films	US	22-Jun-04	6753561
Multi-Output Multiplexor	US	28-Sep-04	6798685
Cross Point Memory Array using Distinct Voltages	US	14-Dec-04	6831854
Cross Point Memory Array using Multiple Modes of Operation	US	21-Dec-04	6834008
Line Drivers that Fit within a Specified Line Pitch	US	28-Dec-04	6836421
Cross Point Memory Array with Memory Plugs Exhibiting a Characteristic Hysteresis	US	1-Feb-05	6850429
Multiplexor Having A Reference Voltage on Unselected Lines	US	1-Feb-05	6850455
Non-Volatile Memory with a Single Transistor and Resistive Memory Element	US	15-Feb-05	6856536
Memory Array of a Non-Volatile RAM	US	22-Feb-05	6859382
Rewritable Memory with Non-Linear Memory Element	US	22-Mar-05	6870755
Re-Writable Memory with Multiple Memory Layers	US	14-Jun-05	6906939
Multiple Modes of Operation in a Cross Point Array	US	21-Jun-05	6909632
High-Density NVRAM	US	12-Jul-05	6917539
An Adaptive Programming Technique for a Re-Writable Conductive Memory Device	US	6-Sep-05	6940744
Multi-Layer Conductive Memory Device	US	15-Nov-05	6965137
Providing A Reference Voltage To A Cross Point Memory Array	US	29-Nov-05	6970375
Memory Element Having Islands	US	6-Dec-05	6972985
Cross Point Memory Array with Memory Plugs Exhibiting a Characteristic Hysteresis	US	31-Jan-06	6992922
Conductive Memory Stack with Non-Uniform Width	US	21-Oct-08	7439082
Conductive Memory Stack with Non-Uniform Width	US	7-Mar-06	7009235
Line Drivers That Use Minimal Metal Layers	US	7-Mar-06	7009909
Discharge of Conductive Array Lines in Fast Memory	US	28-Mar-06	7020006

Cross Point Array using Distinct Voltages	US	28-Mar-06	7020012
A 2-Terminal Trapped Charge Memory Device with Voltage Switchable Multi-Level Resistance	US	2-May-06	7038935
Memory Array with High Temperature Wiring	US	9-May-06	7042035
An Adaptive Programming Technique for a Re-Writable Conductive Memory Device	US	30-May-06	7054183
Cross Point Memory Array With Fast Access Time	US	6-Jun-06	7057914
Low Temperature Deposition of Complex Metal Oxides (CMO) Memory Materials for Non-Volatile Memory Integrated Circuits	US	20-Jun-06	7063984
Conductive Memory Device with Conductive Oxide Electrodes	US	27-Jun-06	7067862
Multi-Resistive State Material That uses Dopants	US	4-Jul-06	7071008
Two terminal memory array having reference cells	US	11-Jul-06	7075817
Layout of Driver Sets in a Cross Point Memory Array	US	18-Jul-06	7079442
Multi-Resistive State Element With Reactive Metal	US	25-Jul-06	7082052
Re-Writable Memory with Multiple Memory Layers	US	22-Aug-06	7095643
Conductive Memory Array Having Page Mode and Burst Mode Read Capability	US	22-Aug-06	7095644
Conductive Memory Array Having Page Mode and Burst Mode Write Capability	US	29-Aug-06	7099179
Non-Volatile Memory with a Single Transistor and Resistive Memory Element	US	24-Oct-06	7126841
Providing A Reference Voltage To A Cross Point Memory Array	US	12-Dec-06	7149107
Memory Array of a Non-Volatile RAM	US	12-Dec-06	7149108
Line Drivers that Fit within a Specified Line Pitch	US	2-Jan-07	7158397
High-Density NVRAM	US	20-Feb-07	7180772
Conductive Memory Stack with Sidewall	US	6-Mar-07	7186569
Cross Point Memory Array With Fast Access Time	US	5-Jun-07	7227767
Two terminal memory array having reference cells	US	5-Jun-07	7227775
Laser Annealing of Complex Metal Oxides (CMO) Memory Materials for Non-Volatile Memory Integrated Circuits	US	18-Dec-07	7309616
Resistive Memory Device with a Treated Interface	US	5-Feb-08	7326979

Storage Controller Using Vertical Memory	US	5-Feb-08	7327600
Providing A Reference Voltage To A Cross Point Memory Array	US	5-Feb-08	7327601
Enhanced Functionality in a Two Terminal Memory Array	US	12-Feb-08	7330370
Two-Cycle Sensing In A Two-Terminal Memory Array Having Leakage Current	US	13-May-08	7372753
Method For Two-Cycle Sensing In A Two-Terminal Memory Array Having Leakage Current	US	14-Oct-08	7436723
Sensing A Signal In A Two-Terminal Memory Array Having Leakage Current	US	27-May-08	7379364
Two Terminal Memory Array Having Reference Cells	US	3-Jun-08	7382644
Two Terminal Memory Array Having Reference Cells	US	25-Nov-08	7457147
Two Terminal Memory Array Having Reference Cells	US	3-Jun-08	7382645
Multi-Resistive State Element With Reactive Metal	US	1-Jul-08	7394679
Conductive Memory Device with Barrier Electrodes	US	15-Jul-08	7400006
Method For Sensing A Signal In A Two-Terminal Memory Array Having Leakage Current	US	17-Mar-09	7505347

Patent Applications

Title		Filing Date	Serial No
Selection Device for Re-Writable Memory	US	11-Sep-08	12283339
Non-Volatile Programmable Memory	WO	3-May-04	PCTUS0413836
Non-Volatile Programmable Memory	CN	3-May-04	2.0048E+12
Non-Volatile Programmable Memory	EP	3-May-04	48220560
Non-Volatile Programmable Memory	JP	3-May-04	2007511326
Non-Volatile Programmable Memory	KR	3-May-04	20067023140
Memory Using Variable Tunnel Barrier Widths	US	3-Sep-04	10934951
Serial Memory Interface	US	8-Jun-06	11449105
Performing Data Operations Using Non-Volatile Third Dimension Memory	US	28-Jun-06	11478163
Memory Power Management	US	18-Aug-06	11506385
Movable Terminal In A Two Terminal Memory Array	US	18-Jan-05	11037971
Memory Using Mixed Valence Conductive Oxides	US	30-Mar-05	11095026
Securing Data In Memory Device	US	10-Jan-08	12008345

N/A

Scaleable Memory Systems Using Third Dimension Memory	US	5-Oct-06	11543502
Fast Data Access Through Page Manipulation	US	19-Jan-07	11655599
Memory Using Mixed Valence Conductive Oxide	WO	2-Sep-05	PCTUS2005031913
Memory Using Mixed Valence Conductive Oxide	CN	2-Sep-05	2005800380245
Memory Using Mixed Valence Conductive Oxide	EP	2-Sep-05	57949307
Memory Using Mixed Valence Conductive Oxide	JP	2-Sep-05	
Memory Using Mixed Valence Conductive Oxide	KR	2-Sep-05	
Buffering Systems Methods For Accessing Multiple Layers Of Memory In Integrated Circuits	US	9-Jan-08	12008212
Multiple-Type Memory	US	16-Jul-07	11893644
Circuitry And Method For Indicating A Memory	US	16-Aug-07	11893647
Memory Emulation In An Image Capture Device	US	30-Aug-07	11897726
Buffering Systems For Accessing Multiple Layers Of Memory In Integrated Circuits	US	8-Jan-08	12006970
Memory Emulation In An Electronic Organizer	US	30-Aug-07	11897909
Memory Emulation In A Cellular Telephone	US	17-Oct-07	11974034
Combined Memories In Integrated Circuits	US	19-Dec-07	12004292
Emulation Of A NAND Memory System	US	20-Dec-07	12004192
Oxygen Depleted Etching Process	US	20-Oct-06	11584876
Programmable Logic Device Structure Using Third Dimensional Memory	US	7-Jan-08	12008077
Conductive Memory Stack With Sidewall	US	5-Mar-07	11714555
Continuous Plane Of Thin-Film Materials For A Two-Terminal Cross-Point Memory	US	26-Jul-07	11881496
Low Read Current Architecture For Memory	US	26-Jul-07	11881500
Multi-Selective Etch Process For Cross-Point Memory	US	26-Jul-07	11881475
Continuous Plane Of Thin-Film Materials For A Two-Terminal Cross-Point Memory	US	26-Jul-07	11881474
Memory Emulation Using Resistivity-Sensitive Memory	US	17-Oct-07	11975275
Planar Third Dimensional Memory With Multi-Port Access	US	4-Dec-07	11999376
Integrated Circuits And Methods to Compensate For Defective Memory In Multiple Layers Of Memory	US	10-Dec-07	12001335
Disturb Control Circuits And Methods To Control Memory Disturbs Among Multiple Layers Of Memory	US	12-Dec-07	12001952

N/A

Media Player With Non-Volatile Memory	US	21-Dec-07	12004737
Non-Volatile Register	US	5-Feb-08	12012641
Method and System for Accessing Non-Volatile Memory	US	22-Dec-07	12004768
Non-Volatile Memory Compiler	US	23-Dec-07	12004740
Memory Access Protection	US	24-Dec-07	12004734
Memory Sanitization	US	26-Dec-07	12005259
Non-Volatile Memories In Interactive Entertainment Systems	US	27-Dec-07	12005687
Non-Volatile Processor Register	US	28-Dec-07	12005685
Field Programmable Gate Arrays Using Resistivity Sensitive Memories	US	29-Dec-07	12006006
State Machines Using Resistivity-Sensitive Memories	US	30-Dec-07	12006199
Radio Frequency Identification Transponder Memory	US	31-Dec-07	12006187
Integrated Circuits To Control Access To Multiple Layers Of Memory	US	6-Feb-08	12012945
Integrated Circuits And Methods To Control Access To Multiple Layers Of Memory	US	7-Feb-08	12069105
Data Retention Structure for Non-Volatile Memory	US	7-Mar-08	12075017
Method For Fabricating Multi-Resistive State Memory Devices	US	30-Jun-08	12215958
Preservation Circuit And Methods To Maintain Values Representing Data In One Or More Layers Of Memory	US	31-Jul-08	12221136
Memory Cell Formation Using Unetched Conductive Metal Oxide	US	19-Dec-08	61/203,912
Conductive Metal Oxide Structures In Non-Volatile Re-Writable Memory Devices	US	19-Dec-08	61/203,163
Modulated Oxide Structure In A Non-Volatile Re-Writeable Memory	US	19-Dec-08	61/203,160
Memory Access Circuits And Layout Of The Same For Cross-Point Memory Arrays	US	19-Dec-08	61/203,191
Memory Device With Dual Depletion Control	US	19-Dec-08	61/203,159
Cooperative Modification of Conductivity for Oxide Structures in Non-Volatile Re-Writable Memory Cells	US	19-Dec-08	61/203,184
CONDUCTIVE OXIDE ELECTRODES	US	19-Dec-08	61/203,153
High Voltage Switching Circuitry For A Cross Point Array	US	19-Dec-08	61/203,229
Device Fabrication	US	19-Dec-08	61/203,187

Manipulation Of Pattern Density And Temperature Using Dummy Structures To Effect Oxide Growth In Semiconductor Memory Structures	US	19-Dec-08	61/203,230
Manipulation Of Pattern Density And Temperature Using Dummy Structures To Effect Oxide Growth In Semiconductor Memory	US	19-Dec-08	61/203,234
Memory Stack Cladding	US	19-Dec-08	61/203,158
Memory Element With Band Gap Control	US	19-Dec-08	61/203,154
Array Operation Using A Schottky Diode As A Non-Ohmic Isolation Device	US	19-Dec-08	61/203,189
Protecting Integrity Of Data In Multi-Layered Memory With Data Redundancy	US	19-Dec-08	61/203,166
Method For Creating Two Layers In A Damascene Trench	US	19-Dec-08	61/203,223
Third Dimensional Memory With Compress Engine	US	19-Dec-08	61/203,190
Hierarchical Array Architecture For Multi-Layer Memory	US	19-Dec-08	61/203,236
Configurable Memory Interface To Provide Serial And Parallel Access To Memories	US	19-Dec-08	61/203,203
Signal Margin Improvement In A Cross-Point Memory Array	US	19-Dec-08	61/203,212
Bi-Polar Inversion MOS Non-Ohmic Device	US	19-Dec-08	61/203,162
Bi-Polar Varistor Non-Ohmic Device	US	19-Dec-08	61/203,214
No-Etch Isolation Of A Semiconductor Crystallization Non-Ohmic Device	US	19-Dec-08	61/203,164
Mobile Trivalent Ion Non-Volatile Re-Writeable Memory Devices	US	19-Dec-08	61/203,233
Array Architecture For Multi-Layer Chalcogenide Memory	US	19-Dec-08	61/203,149
Data Storage System With Non-Volatile Memory Using Both Page Write And Block Program And Block Erase	US	22-Dec-08	61/203,440
Multi-Structured Memory	US	22-Dec-08	61/203,430
Digital Potentiometer Using Third Dimensional Memory	US	22-Dec-08	61/203,446
Memory Scrubbing In Third Dimension Memory	US	22-Dec-08	61/203,456
Data Storage System With Refresh In Place	US	30-Jan-09	61/206,397
Multiple Layers Of Memory Implemented As Different Memory Technology	US	30-Jan-09	61/206,395

Fuse Elements Based On Two-Terminal Re-Writeable Non-Volatile Memory	US	30-Jan-09	61/206,446	
Non-Volatile Dual Port Third Dimensional Memory	US	30-Jan-09	61/206,447	
Non-Volatile FIFO With Third Dimension Memory	US	2-Mar-09	61/208,933	
Columnar Replacement Of Defective Memory Cells	US	13-Mar-09	TBD	MA

INTELLECTUAL PROPERTY SECURITY AGREEMENT

This Intellectual Property Security Agreement is entered into as of the March 27, 2009 by and between SILICON VALLEY BANK, as Agent ("Bank") and Unity Semiconductor Corporation ("Grantor").

RECITALS

A. Bank and its co-lender have made certain advances of money and extended certain financial accommodation to Grantor (the "Loans") in the amounts and manner set forth in that certain Loan and Security Agreement by and between Bank, Gold Hill Venture Lending 03, LP and Grantor dated the Effective Date (as the same may be amended, modified or supplemented from time to time, the "Loan Agreement"; capitalized terms used herein are used as defined in the Loan Agreement). Bank and its co-lender are willing to make certain accommodations to Grantor, but only upon the condition, among others, that Grantor shall grant to Bank a security interest in certain copyrights, trademarks, patents, and mask works to secure the obligations of Grantor under the Loan Agreement.

B. Pursuant to the terms of the Loan Agreement, Grantor has granted to Bank a security interest in all of Grantor's right, title and interest, whether presently existing or hereafter acquired, in, to and under all of the Collateral.

NOW, THEREFORE, for good and valuable consideration, receipt of which is hereby acknowledged, and intending to be legally bound, as collateral security for the prompt and complete payment when due of its obligations under the Loan Agreement, Grantor hereby represents, warrants, covenants and agrees as follows:

AGREEMENT

To secure its obligations under the Loan Agreement, Grantor grants and pledges to Bank a security interest in all of Grantor's right, title and interest in, to and under its intellectual property (including without limitation those copyrights, patents, trademarks and mask works listed on Schedules A, B, C, and D hereto), and including without limitation all proceeds thereof (such as, by way of example but not by way of limitation, license royalties and proceeds of infringement suits), the right to sue for past, present and future infringements, all rights corresponding thereto throughout the world and all re-issues, divisions continuations, renewals, extensions and continuations-in-part thereof.

This security interest is granted in conjunction with the security interest granted to Bank under the Loan Agreement. The rights and remedies of Bank with respect to the security interest granted hereby are in addition to those set forth in the Loan Agreement and the other Loan Documents, and those which are now or hereafter available to Bank as a matter of law or equity. Each right, power and remedy of Bank provided for herein or in the Loan Agreement or any of the Loan Documents, or now or hereafter existing at law or in equity shall be cumulative and concurrent and shall be in addition to every right, power or remedy provided for herein and the exercise by Bank of any one or more of the rights, powers or remedies provided for in this Intellectual Property Security Agreement, the Loan Agreement or any of the other Loan Documents, or now or hereafter existing at law or in equity, shall not preclude the simultaneous or later exercise by any person, including Bank, of any or all other rights, powers or remedies.

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

UNITY SEMICONDUCTOR CORPORATION

By: David R

Title: CEO

Address of Grantor:

230 North Wolfe Road
Sunnyvale, CA 94086

Attn: _____

BANK:

SILICON VALLEY BANK, Individually and as Agent

Address of Bank:

2400 Hanover Street
Palo Alto, CA 94304

Attn: Matthew Wright

By: _____

Title: _____

IN WITNESS WHEREOF, the parties have caused this Intellectual Property Security Agreement to be duly executed by its officers thereunto duly authorized as of the first date written above.

GRANTOR:

UNITY SEMICONDUCTOR CORPORATION

By:_____

Title:_____

Address of Grantor:

250 North Wolfe Road
Sunnyvale, CA 94085

Attn: _____

BANK:

SILICON VALLEY BANK, Individually and as Agent

By: Matthew Wright

Title: RM

Address of Bank:

2400 Hanover Street
Palo Alto, CA 94304

Attn: Matthew Wright

EXHIBIT A

Copyrights

Description	Registration/ Application Number	Registration/ Application Date
None registered		

EXHIBIT B

Patents

Description	Registration/ Application Number	Registration/ Application Date
See attached		

EXHIBIT C

Trademarks

Description	Registration/ Application Number	Registration/ Application Date
See attached		

EXHIBIT D

Mask Works

Description	Registration/ Application Number	Registration/ Application Date
None registered		