PATENT ASSIGNMENT

Electronic Version v1.1
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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Inovys Corporation	10/06/2009

RECEIVING PARTY DATA

Name:	Verigy (Singapore) Pte. Ltd.
Street Address:	No. 1 Yishun Avenue 7
Internal Address:	Lot 1937C, 1935X, 1975P
City:	Singapore
State/Country:	SINGAPORE
Postal Code:	768923

PROPERTY NUMBERS Total: 27

Property Type	Number
Patent Number:	7032145
Patent Number:	6839648
Patent Number:	6900621
Patent Number:	7047463
Patent Number:	7013417
Patent Number:	6859157
Patent Number:	7154253
Application Number:	11563612
Application Number:	11565616
Application Number:	11609899
Application Number:	11680134
Application Number:	11682314
Application Number:	29281959
Application Number:	11850342

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Application Number:	11931847
Application Number:	11941026
Application Number:	60829317
Application Number:	60895984
Patent Number:	6880137
Patent Number:	6591213
Patent Number:	6750797
Patent Number:	7114114
Application Number:	10741110
Application Number:	60981915
Application Number:	12074015
Application Number:	12058768
PCT Number:	US0882088

CORRESPONDENCE DATA

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ATTORNEY DOCKET NUMBER:	INOVYS ASSIGNMENTS
NAME OF SUBMITTER:	Gregory W. Osterloth

Total Attachments: 5

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ASSIGNMENT OF PATENTS

Whereas Inovys Corporation, a California corporation having its principal place of business at 6940 Koll Center Parkway, Pleasanton, California 94566, USA (hereinafter "***Assignor***") is the sole and exclusive owner of certain patents and patent applications set forth in Attachment A of this Assignment (collectively referred to as the "***Patents***");

Whereas Verigy (Singapore) Pte. Ltd., a Singapore corporation having its principal place of business at No. 1 Yishun Avenue 7, Lot 1937C, 1935X, 1975P, Singapore 768923 (hereinafter "***Assignee***") is desirous of acquiring the entire right, title and interest in, to and under the Patents;

Now, Therefore, For good and valuable consideration, the receipt of which is hereby acknowledged, Assignor does hereby sell, assign, transfer and set over to Assignee the entire right, title and interest in, to and under the Patents set forth in Attachment A of this Assignment, including any international or foreign counterpart patent or patent application owned or controlled by Assignor, and the right to file or request same; any continuation, continuation-in-part, divisional, renewal, reexamination, reissue, national phase filing, or substitute for any of the Patents, and the right to file or request same; and the right to claim and obtain a patent on any invention described in the Patents (whether now claimed or yet to be claimed); the same to be held and enjoyed by Assignee for its own use and enjoyment, and for the use and enjoyment of its successors, assigns or other legal representatives, to the end of the term or terms for which said Patents are or may be granted, reissued or extended, as fully and entirely as the same would have been held and enjoyed by Assignor if this assignment and sale had not been made; together with all claims for damages by reason of past or future infringement of one or more of the Patents, with the right to sue for and collect the same for Assignor's own use and behalf, and for the use and behalf of its successors, assigns or other legal representatives.

Assignor hereby authorizes and requests the Commissioner of Patents and Trademarks, or an equivalent officer in any jurisdiction in which said Patents have issued or may issue, to issue any and all Patents to Assignee as assignee of the entire right, title and interest in and to such Patents. Assignor also hereby covenants that Assignor has full right to convey the entire interest herein assigned, and that, except as otherwise provided between the parties, Assignor has not executed, and will not execute, any agreements in conflict therewith.

This Assignment may be executed simultaneously in two or more counterparts, each of which shall be deemed an original, but all of which together shall constitute one and the same instrument.

In Witness Whereof, the parties, by their duly authorized representatives, have executed this Assignment.

Inovys Corporation

By: _____

Print Name: Larry D. Bathke

Print Title: President

Date: Oct 6, 2009

Verigy (Singapore) Pte. Ltd.

By: _____

Print Name: Kenneth M. Siegel

Print Title: Director

Date: Oct 6, 2009

ATTACHMENT A
SCHEDULE OF ASSIGNED PATENTS & PATENT APPLICATIONS

TITLE	COUNTRY OF FILING	REGISTRATION NO./ SERIAL NO.	FILE DATE	GRANT DATE
System for dynamic re-allocation of test pattern data for parallel and serial test data patterns	USA	7,032,145	2002-06-14	2006-04-18
Systems for providing zero latency, non-modulo looping and branching of test pattern data for automated test equipment	USA	6,839,648	2003-05-01	2005-01-04
Digitally controlled modular power supply for automated test equipment	USA	6,900,621	2003-07-03	2005-05-31
Method and system for automatically determining a testing order when executing a test flow	USA	7,047,463	2003-08-15	2006-05-16
Dynamically reconfigurable precision signal delay test system for automatic test equipment	USA	7,013,417	2004-01-09	2006-03-14
Programmable precision current controlling apparatus	USA	6,859,157	2004-06-02	2005-02-22
Digitally controlled modular power supply for automated test equipment	USA	7,154,253	2005-03-22	2006-12-26
System and Method for Device Performance Characterization in Physical and Logical Domains with AC SCAN Testing	USA	11/563,612	2006-11-27	
Process for improving design limited yield by efficiently capturing and storing production test data for analysis using checksums, hash values, or digital fault signatures	USA	11/565,616	2006-11-30	
Process for identifying the location of a break in a scan chain in real time	USA	11/609,899	2006-12-12	
Apparatus for locating a defect in a	USA	11/680,134	2007-02-28	

TITLE	COUNTRY OF FILING	REGISTRATION NO./ SERIAL NO.	FILE DATE	GRANT DATE
scan chain while testing digital logic				
Process for Improving Design-Limited Yield by Localizing Potential Faults from Production Test Data	USA	11/682,314	2007-03-06	
Fault Viewer Display	USA	29/281,959	2007-07-07	
Method for operating a secure semiconductor IP server to support failure analysis	USA	11/850,342	2007-09-05	
Locating hold time violations in scan chains by generating patterns on ATE	USA	11/931,847	2007-10-31	
Dynamic Mask Memory For Serial Scan Testing	USA	11/941,026	2007-11-15	
System and method for device performance characterization in physical and logical domains with AC SCAN testing	USA	11/563,612	2006-11-27	
Process for improving design limited quality by filtering production test data through a yield monitoring system to localize electrical faults on semiconductor wafers	USA	60/829,317	2006-10-13	
Logging a Category of Defect in Semiconductor test	USA	60/895,984	2007-03-21	
Dynamically reconfigurable precision signal delay test system for automatic test equipment	USA	6,880,137	2002-08-02	2005-04-12
Systems for providing zero latency, non-modulo looping and branching of test pattern data for automatic test equipment	USA	6,591,213	2001-02-27	2003-07-08
Programmable precision current controlling apparatus	USA	6,750,797	2003-01-31	2004-06-15
Dynamically reconfigurable precision signal delay test system for automatic test equipment	USA	7114114	8/12/2004	2006-09-26
Method and system for delay defect location when testing digital semiconductor devices	USA	2005/0203716	2003-12-19	
Locating Hold Time Violations in Scan Chains by Generating Patterns	USA	60/981,915	2007-10-23	

TITLE	COUNTRY OF FILING	REGISTRA-TION NO./ SERIAL NO.	FILE DATE	GRANT DATE
on ATE				
Methods and Apparatus for Estimating a Position of a Stuck-At Defect in a Scan Chain of a Device Under Test	USA	12/074,015	2008-02-28	
Methods for Analyzing Scan Chains, and for Determining Numbers or Locations of Hold Time Faults in Scan Chains	USA	12/058,768	2008-03-31	
Methods for Analyzing Scan Chains, and for Determining Numbers or Locations of Hold Time Faults in Scan Chains	Taiwan	97141777	2008-10-30	
Methods for Analyzing Scan Chains, and for Determining Numbers or Locations of Hold Time Faults in Scan Chains	PCT	PCT/US2008/ 082088	2008-10-31	