PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Infineon Technologies AG	09/05/2006

RECEIVING PARTY DATA

Name:	Qimonda AG
Street Address:	Gustav-Heinemann-Ring 212
City:	Munich
State/Country:	GERMANY

PROPERTY NUMBERS Total: 25

Property Type	Number
Patent Number:	5308783
Patent Number:	5444398
Patent Number:	5932919
Patent Number:	5847591
Patent Number:	5979244
Patent Number:	6706616
Patent Number:	6529031
Patent Number:	6556492
Patent Number:	6750671
Patent Number:	6724181
Patent Number:	6970006
Patent Number:	6614243
Patent Number:	6853206
Patent Number:	6762611
Patent Number:	6731552
Patent Number:	6677745

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Patent Number:	6784683
Patent Number:	6586978
Patent Number:	6773934
Patent Number:	6614248
Patent Number:	6703844
Patent Number:	6558883
Patent Number:	6781398
Patent Number:	6850448
Patent Number:	6973008

CORRESPONDENCE DATA

Fax Number: (613)591-8148
Correspondence will be sent via US Mail when the fax attempt is unsuccessful.
Phone: 613-599-9539
Email: ipadmin@mosaid.com
Correspondent Name: Mosaid Technologies Incorporated
Address Line 1: 11 Hines Road
Address Line 2: Suite 203
Address Line 4: Ottawa, CANADA K2K 2X1

ATTORNEY DOCKET NUMBER:	INFINEON ASSIGNMENTS
NAME OF SUBMITTER:	Victoria Donnelly

Total Attachments: 3
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ASSIGNMENT

Infineon Technologies AG, a corporation organized and existing under the laws of Germany, having a place of business in Munich, Bavaria, Germany, hereinafter referred to as Assignor, hereby assigns and transfers to Qimonda AG, a German corporation, having a place of business in Munich, Bavaria, Germany, hereinafter referred to as Assignee,

the entire right, title and interest in and to any and all inventions disclosed and/or claimed in the United States identified on Schedule A to this assignment ("the Patents")." All rights held by the Assignee as a result of this assignment have been and are granted, extended and transferred to Assignee as fully and entirely as they would have been held and enjoyed by the Assignor if this assignment had not been made.

Assignor represents and covenants that no assignment, grant, mortgage, license or other agreement affecting the rights and property herein conveyed has been made to any other party by Assignee.

Assignor:
Infineon Technologies AG

i.V. _____ i.V. _____

Dr. Dieter Joseph Joe Villella

Senior Principal Vice President

Dated: Munich, 5th September 2006

Schedule A

US patents:

Patent Number	Date of Grant	Filing No	Filing Date	Title
US 5308783	03.05.1994	07/991,776	16.12.1992	Process For The Manufacture Of A High Density Cell Array Of Gain Memory Cells
US 5444398	22.08.1995	07/995,639	17.12.1992	A Decoded-Source Sense Amplifier with Special Column Select Driver Voltage
US 5847591	08.12.1998	08/829,256	31.03.1997	Voltage Detection Circuit and Internal Voltage Clamp Circuit
US 5932919	03.08.1999	08/856,336	14.05.1997	Mosfets With Improved Short Channel Effects And Method
US 5979244	09.11.1999	09/034,517	04.03.1998	Method And Apparatus For Evaluating Internal Film Stress At High Lateral Resolution
US 6529031	04.03.2003	09/876,706	07.06.2001	Integrated circuit configuration for testing transistors
US 6556492	29.04.2003	09/907,695	18.07.2001	System for testing fast synchronous semiconductor circuits
US 6558883	06.05.2003	09/801,413	08.03.2001	Relaxation of Mask Manufacturing by Adjusted Stage Synchronization
US 6586978	01.07.2003	10/177,945	20.06.2002	Delay locked loop
US 6614243	02.09.2003	09/947,295	05.09.2001	Measurement probe for detecting electrical signals in an integrated semiconductor circuit
US 6614248	02.09.2003	10/186,659	01.07.2002	Tester apparatus for electronic components
US 6677745	13.01.2004	10/134,132	29.04.2002	Test apparatus for parallel testing a number of electronic components and a method for calibrating the test apparatus
US 6703844	09.03.2004	10/223,899	20.08.2002	Method for determining the transit time of electrical signals on printed circuit boards using automatic standard test equipment
US 6706616	16.03.2004	09/914,749	02.03.2000	Method for improving thermal process steps
US 6724181	20.04.2004	09/992,290	16.11.2001	Method of calibrating a test system for semiconductor components, and test substrate
US 6731552	04.05.2004	10/206,299	26.07.2002	Integrated dynamic memory and operating method

Patent Number	Date of Grant	Filing No	Filing Date	Title
US 6750671	15.06.2004	09/915,984	25.07.2001	Apparatus for testing semiconductor devices
US 6762611	13.07.2004	10/010,504	05.12.2001	Test configuration and test method for testing a plurality of integrated circuits in parallel
US 6773934	10.08.2004	10/105,590	25.03.2002	Method for releasable contact-connection of a plurality of integrated semiconductor modules on a wafer
US 6781398	24.08.2004	10/208,252	30.07.2002	Circuit for testing an integrated circuit
US 6784683	31.08.2004	10/131,374	24.04.2002	Circuit configuration for selectively transmitting information items from a measuring device to chips on a wafer during chip fabrication
US 6850448	01.02.2005	10/386,148	11.03.2003	Temperature-dependent refresh cycle for DRAM
US 6853206	08.02.2005	10/736,356	05.12.2001	Method and probe card configuration for testing a plurality of integrated circuits in parallel
US 6970006	29.11.2005	10/965,513	16.08.2001	Apparatus for the automated testing, calibration and characterization of test adapters
US 6973008	06.12.2005	10/834,416	29.04.2004	Apparatus for flexible deactivation of word lines of dynamic memory modules and method therefor