# PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

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| SUBMISSION TYPE: | NEW ASSIGNMENT |
| NATURE OF CONVEYANCE: | ASSIGNMENT |

CONVEYING PARTY DATA

| Name | Execution Date |
|---|---|
| Impinj, Inc. | 06/26/2009 |

RECEIVING PARTY DATA

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| Name: | Virage Logic Corporation |
| Street Address: | 47100 Bayside Parkway |
| City: | Fremont |
| State/Country: | CALIFORNIA |
| Postal Code: | 94538 |

PROPERTY NUMBERS Total: 1

| Property Type | Number |
|---|---|
| Application Number: | 12403333 |

CH $40.00 12403333

CORRESPONDENCE DATA

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| ATTORNEY DOCKET NUMBER: | VIRP-0212CON (468188-099) |
| NAME OF SUBMITTER: | David B. Ritchie |

Total Attachments: 10
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## PATENT ASSIGNMENT

WHEREAS, IMPINJ, INC., organized and existing under the laws of the State of Delaware, and having a place of business at 701 N. 34th Street, Suite 300, Seattle, Washington 98103 ("Assignor"), is the assignee of the inventions listed in Schedule A for which certain patent applications have been filed, certain of which have issued as Letters Patents of the United States;

and WHEREAS, VIRAGE LOGIC CORPORATION, organized and existing under the laws of the State of Delaware, and having a place of business at 47100 Bayside Parkway, Fremont, California 94538 ("Assignee"), is desirous of obtaining the entire right, title and interest in, to and under the said inventions and the said applications and Letters Patents listed in Schedule A (hereinafter, the "Properties"):

NOW, THEREFORE, in consideration of the sum of One Dollar ($1.00) to it in hand paid, and other good and valuable consideration, the receipt of which is hereby acknowledged, the said Assignor has sold, assigned, transferred and set over, and by these presents does hereby sell, assign, transfer and set over, unto the said Assignee, its successors, legal representatives and assigns, Assignor's entire right, title and interest in, to and under the Properties and all divisions, renewals, continuations, and continuations-in-part thereof, and all Letters Patent of the United States which may be granted thereon and all reissues, re-examined patents, and extensions thereof, to the full end of the term thereof, as fully and entirely as the same would have been held by Assignor had this assignment and sale not been made, including all rights to recover damages for any and all past infringement, and all applications for Letters Patent which may hereafter be filed for said Properties in any country or countries foreign to the United States, and all Letters Patent which may be granted for said Properties in any country or countries foreign to the United States and all extensions, renewals and reissues thereof and all rights of priority in any such country or countries based upon the filing of applications for said Properties for Letters Patent of the United States which are created by any law, treaty or international convention; and Assignors hereby authorize and request the Commissioner of Patents of the United States, and any Official of any country or countries foreign to the United States, whose duty it is to issue patents on applications as aforesaid, to issue all Letters Patent for said Properties to the said Assignee, its successors, legal representatives and assigns, in accordance with the terms of this instrument.

AND ASSIGNOR HEREBY covenants that it has full right to convey the entire interest herein assigned, and that it has not executed, and will not execute, any agreement in conflict herewith.

AND ASSIGNOR HEREBY further covenants and agrees that it will communicate to the said Assignee, its successors, legal representatives and assigns, any facts known to Assignor

respecting said Properties, and testify in any legal proceeding, sign all lawful papers, execute all divisional, continuing, reissue and foreign applications, make all rightful oaths, and generally do everything possible to aid the said Assignee, its successors, legal representatives and assigns, to obtain and enforce proper protection for said Properties in all countries.

**[Signature Pages Follow]**

**IN TESTIMONY WHEREOF**, the undersigned officers and individuals of Assignor and Assignee, with authority to do so, have hereunto set their hands and seals on the dates set forth below.

ASSIGNOR:

IMPINJ, INC.

Date: 6/26, 2008

By: _____
Name: William T. Colleran
Title: President & CEO

State of WA )
) SS.:
County of King )

On June 26, 2008, before me, Stacy L. Jones, personally appeared William Colleran, who proved to me on the basis of satisfactory evidence to be the person(s) whose name(s) is subscribed to the within instrument and acknowledged to me that he/she/they executed the same in his/her/their authorized capacity(ies), and that by his/her/their signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of Washington that the foregoing paragraph is true and correct.

WITNESS my hand and official seal

_____

STACY L JONES
NOTARY PUBLIC
STATE OF WASHINGTON
COMMISSION EXPIRES
MARCH 17, 2010

**IN TESTIMONY WHEREOF**, the undersigned officers and individuals of Assignor and Assignee, with authority to do so, have hereunto set their hands and seals on the dates set forth below.

ASSIGNEE:

VIRAGE LOGIC CORPORATION

Date: June 26, 2008

By: _____

Name: Christine Russell

Title: Chief Financial Officer

State of California )
) SS.:
County of Alameda )

On June 26, 2008, before me, Chau B. Ho Notary Public, personally appeared Christine Russell, who proved to me on the basis of satisfactory evidence to be the person~~(s)~~ whose name~~(s)~~ is subscribed to the within instrument and acknowledged to me that ~~he/she/they~~ executed the same in ~~his/her/their~~ authorized capacity~~(ies)~~; and that by ~~his/her/their~~ signature~~(s)~~ on the instrument the person~~(s)~~, or the entity upon behalf of which the person~~(s)~~ acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.

WITNESS my hand and official seal

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CHAU B. HO
Commission # 1717044
Notary Public - California
Alameda County
My Comm. Expires Jan 16, 2011

SCHEDULE A

| Title | Application Number | Filing Date | Publ'n Number | Publ'n Date | Patent Number | Issue Date |
|---|---|---|---|---|---|---|
| METHOD AND APPARATUS FOR TRIMMING HIGH-RESOLUTION DIGITAL-TO-ANALOG CONVERTER | 10/661,037 | 9/12/2003 | | | | |
| VARIABLE DELAY CIRCUIT AND METHOD HAVING CONTINUOUSLY VARIABLE DELAY RESOLUTION | 10/666,789 | 9/17/2003 | | | | |
| METHOD AND APPARATUS FOR PROGRAMMING SINGLE-POLY PFET-BASED NONVOLATILE MEMORY CELLS | 11/528,069 | 9/26/2006 | 20070019475 | 1/25/2007 | | |
| METHOD AND APPARATUS FOR PROGRAMMING SINGLE-POLY PFET-BASED NONVOLATILE MEMORY CELLS | 11/528,262 | 9/26/2006 | 20070019477 | 1/25/2007 | | |
| METHOD AND APPARATUS FOR PROGRAMMING SINGLE-POLY PFET-BASED NONVOLATILE MEMORY CELLS | 11/528,150 | 9/26/2006 | 20070019476 | 1/25/2007 | | |
| PMOS MEMORY CELL | 10/936,283 | 9/7/2004 | 20050030827 | 2/10/2005 | | |
| A HIGH-VOLTAGE LDMOSFET AND APPLICATIONS THEREFOR IN STANDARD CMOS | 10/952,708 | 9/28/2004 | 20050258461 | 11/24/2005 | | |
| GAIN-ENHANCED INVERTER DEVICE | 11/207,388 | 8/18/2005 | | | | |
| REDUNDANT NON-VOLATILE MEMORY CELL | 11/106,982 | 4/15/2005 | 20060221715 | 10/5/2006 | | |
| SCHOTTKY JUNCTION DIODE DEVICES IN CMOS | 11/387,603 | 3/22/2006 | 20060223247 | 10/5/2006 | | |
| SCHOTTKY JUNCTION DIODE DEVICES IN CMOS WITH MULTIPLE WELLS | 11/387,515 | 3/22/2006 | 20060223246 | 10/5/2006 | | |
| TUNNELING-ENHANCED FLOATING GATE SEMICONDUCTOR DEVICE | 11/133,718 | 5/19/2005 | 20060220096 | 10/5/2006 | | |

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| FAULT TOLERANT NON VOLATILE MEMORIES AND METHODS | 11/372,438 | 3/9/2006 | 20060220639 | 10/5/2006 |
| PSEUDO-NONVOLATILE DIRECT-TUNNELING FLOATING-GATE DEVICE | 11/224,743 | 9/12/2005 | | |
| REDUCED AREA HIGH VOLTAGE SWITCH FOR NVM | 11/513,597 | 8/30/2006 | 20060291319 | 12/28/2006 |
| GRADED JUNCTION HIGH VOLTAGE SEMICONDUCTOR DEVICE | 11/490,407 | 7/19/2006 | 20070093028 | 4/26/2007 |
| NON-VOLATILE MEMORY DEVICES HAVING FLOATING -GATE FETS WITH DIFFERENT SOURCE-GATE AND DRAIN-GATE BORDER LENGTHS | 11/701,710 | 2/2/2007 | | |
| MEMORY MANAGEMENT UNIT (MMU) TO MAKE ONLY ONE TIME PROGRAMMABLE (OTP) MEMORY APPEAR MULTIPLE TIMES PROGAMMABLE (MTP) | 11/818,757 | 6/15/2007 | | |
| ONE TIME PROGRAMMABLE MEMORY TEST STRUCTURES AND METHODS | 11/768,974 | 6/27/2007 | | |
| NON-VOLATILE MEMORY WITH PROGRAMMING THROUGH BAND-TO-BAND TUNNELING AND IMPACT IONIZATION GATE CURRENT | 11/601,474 | 11/16/2006 | | |
| NON-VOLATILE MEMORY CELL CIRCUIT WITH PROGRAMMING THROUGH BAND-TO-BAND TUNNELING AND IMPACT IONIZATION GATE CURRENT | 11/601,305 | 11/16/2006 | | |
| COUNTERACTING OVERTUNNELING IN NONVOLATILE MEMORY CELLS | 11/731,228 | 3/29/2007 | 20070171724 | 7/26/2007 |
| INVERTER NON-VOLATILE MEMORY CELL AND ARRAY SYSTEM | 11/748,541 | 5/15/2007 | 20070263456 | 11/15/2007 |
| INVERTER NON-VOLATILE MEMORY CELL AND ARRAY SYSTEM | 11/842,862 | 8/21/2007 | | |
| ELECTROSTATIC DISCHARGE MANAGEMENT APPARATUS, | 11/837,810 | 8/13/2007 | | |

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| SYSTEMS, AND METHODS | | |
| HYBRID NON-VOLATILE MEMORY | 11/829,370 | 7/27/2007 |
| CONFIGURABLE SINGLE BIT/DUAL BITS MEMORY | 11/981,056 | 10/30/2007 |
| ADAPTIVE PROGRAMMING OF MEMORY CIRCUIT | 11/982,277 | 10/31/2007 |
| IMPROVED PFET NONVOLATILE MEMORY | 11/865,777 | 10/2/2007 |
| MULTI-LEVEL NON-VOLATILE MEMORY CELL WITH HIGH-VT ENHANCED BTBT DEVICE | 12/080,127 | 3/31/2008 |
| METHODS FOR ADAPTIVE PROGRAMMING OF MEMORY CIRCUIT | 11/982,278 | 10/31/2007 |
| NON VOLATILE MEMORY CIRCUIT WITH TAILORED RELIABILITY | 12/114,574 | 5/2/2008 |
| HIGH VOLTAGE SWITCH USING THREE FETS | 12/143,133 | 6/20/2008 |
| RFID TAG WITH REDUNDANT NON-VOLATILE MEMORY CELL | 12/020,522 | 1/26/2008 |
| RFID TAG HAVING NON-VOLATILE MEMORY DEVICE HAVING FLOATING-GATE FETS WITH DIFFERENT SOURCE-GATE AND DRAIN-GATE BORDER LENGTHS | 12/006,330 | 12/31/2007 |
| RFID TAG SEMICONDUCTOR CHIP WITH MEMORY MANAGMENT UNIT (MMU) TO MAKE ONLY ONE TIME PROGRAMMABLE (OTP) MEMORY APPEAR MULTIPLE TIMES PROGRAMMABLE (MTP) | 12/006,321 | 12/31/2007 |
| RADIO FREQUENCY IDENTIFICATION DEVICE POWER-ON RESET MANAGEMENT | 11/965,359 | 12/27/2007 |
| RADIO FREQUENCY IDENTIFICATION DEVICE ELECTROSTATIC DISCHARGE MANAGEMENT | 11/965,307 | 12/27/2007 |

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| RADIO FREQUENCY (RFID) TAG INCLUDING CONFIGURABLE SINGLE BIT/DUAL BITS MEMORY | 12/012,910 | 2/5/2008 | | | | |
| LEAKAGE TOLERANT NVM CELL AND ARRAY | 11/124,695 | 5/9/2005 | | | | |
| USE OF ANALOG-VALUED FLOATING-GATE TRANSISTORS TO MATCH THE ELECTRICAL CHARACTERISTICS OF INTERLEAVED AND PIPELINED CIRCUITS | 11/403,464 | 4/12/2006 | | | | |
| DETECTING LACK OF PRIOR PROGRAMMING IN NVM CELLS BY DIFFERENTIAL READOUT | 11/502,658 | 8/11/2006 | | | | |
| REWRITEABLE ELECTRONIC FUSES | PCT/US2005/010431 | 3/30/2004 | | | | |
| REWRITEABLE ELECTRONIC FUSES | PCT/US2005/010432 | 3/30/2004 | | | | |
| FLOATING-GATE SEMICONDUCTOR STRUCTURES | PCT/US03/21677 | 7/9/2003 | 2004006340 | 1/15/2004 | | |
| FLOATING-GATE SEMICONDUCTOR STRUCTURES | 3763467.2 | 7/9/2003 | 1522105 | 4/13/2005 | | |
| FLOATING-GATE SEMICONDUCTOR STRUCTURES | 2004-520129 | 7/9/2003 | | | | |
| METHOD AND APPARATUS FOR TRIMMING HIGH-RESOLUTION DIGITAL-TO-ANALOG CONVERTER | 09/929,652 | 8/31/2001 | | | 6,664,909 | 2003 |
| USE OF ANALOG-VALUED FLOATING-GATE TRANSISTORS TO MATCH THE ELECTRICAL CHARACTERISTICS OF INTERLEAVED AND PIPELINED CIRCUITS | 10/681,577 | 10/7/2003 | 20040124892 | 7/1/2004 | 7,049,872 | 5/23/2006 |

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| METHOD AND APPARATUS FOR PREVENTING OVERTUNNELING IN PFET-BASED NONVOLATILE MEMORY CELLS | 10/245,183 | 9/16/2002 | 20040052113 | 3/18/2004 | 6,853,583 | 2/8/2005 |
| REWRITEABLE ELECTRONIC FUSES | 10/813,907 | 3/30/2004 | 20050219931 | 10/6/2005 | 7,242,614 | 7/10/2007 |
| REWRITEABLE ELECTRONIC FUSES | 10/814,866 | 3/30/2004 | 20050219932 | 10/6/2005 | 7,388,420 | 6/17/2008 |
| REWRITEABLE ELECTRONIC FUSES | 10/814,868 | 3/30/2004 | 20050237840 | 10/27/2005 | 7,177,182 | 2/13/2007 |
| METHOD AND APPARATUS FOR PROGRAMMING SINGLE-POLY PFET-BASED NONVOLATILE MEMORY CELLS | 10/936,282 | 9/7/2004 | 20050030826 | 2/10/2005 | 7,149,118 | 12/12/2006 |
| HIGH-VOLTAGE SWITCHES IN SINGLE-WELL CMOS PROCESSES | 10/814,867 | 3/30/2004 | 20050052201 | 3/10/2005 | 7,145,370 | 12/5/2006 |
| DIFFERENTIAL FLOATING GATE NONVOLATILE MEMORIES | 10/437,262 | 5/12/2004 | 20040037127 | 2/26/2004 | 6,950,342 | 9/27/2005 |
| HIGH-VOLTAGE CMOS-COMPATIBLE CAPACITORS | 10/635,247 | 8/5/2003 | | | 6,842,327 | 1/11/2005 |
| PFET NONVOLATILE MEMORY | 10/839,985 | 5/5/2004 | 20050063235 | 3/24/2005 | 7,221,596 | 5/22/2007 |
| NATIVE HIGH-VOLTAGE N-CHANNEL LDMOSFET IN STANDARD LOGIC CMOS | 10/884,236 | 7/2/2004 | 20060001087 | 1/5/2006 | 7,315,067 | 1/1/2008 |
| HIGH VOLTAGE FET GATE STRUCTURE | 11/138,888 | 5/26/2005 | 20060001050 | 1/5/2006 | 7,375,398 | 5/20/2008 |
| GRADED-JUNCTION HIGH-VOLTAGE MOSFET IN STANDARD LOGIC CMOS | 10/884,326 | 7/2/2004 | 20050236666 | 10/27/2005 | 7,145,203 | 12/5/2006 |
| COUNTERACTING OVERTUNNELING IN NONVOLATILE MEMORY CELLS | 10/830,280 | 4/21/2004 | 20040195593 | 10/7/2004 | 7,212,446 | 5/1/2007 |
| HYBRID NON-VOLATILE MEMORY | 11/237,099 | 9/28/2005 | 20060023550 | 2/2/2006 | 7,283,390 | 10/16/2007 |
| CAPACITIVE LEVEL SHIFTING FOR ANALOG SIGNAL PROCESSING | 11/313,549 | 12/20/2005 | 20070139244 | 6/21/2007 | 7,233,274 | 6/19/2007 |
| HIGH-VOLTAGE CMOS-COMPATIBLE CAPACITORS | 10/931,583 | 9/1/2004 | 20050093094 | 5/5/2005 | 7,071,507 | 7/4/2006 |

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| HIGH-VOLTAGE CMOS-COMPATIBLE CAPACITORS | 10/931,582 | 9/1/2004 | 20050030702 | 2/10/2005 | 7,042,701 | 5/9/2006 |
| INVERTER NON-VOLATILE MEMORY CELL AND ARRAY SYSTEM | 11/084,214 | 3/17/2005 | 20060209598 | 9/21/2006 | 7,257,033 | 8/14/2007 |
| COMPACT NON-VOLATILE MEMORY CELL AND ARRAY SYSTEM | 11/084,213 | 3/17/2005 | 20060209597 | 9/21/2006 | 7,263,001 | 8/28/2007 |
| MTP NVM ELEMENTS BY-PASSED FOR PROGRAMMING | 11/335,185 | 1/18/2006 | 20060181927 | 8/17/2006 | 7,289,358 | 10/30/2007 |
| HIGH-VOLTAGE CMOS-COMPATIBLE CAPACITORS | 11/326,243 | 1/4/2006 | 20060120013 | 6/8/2006 | 7,262,092 | 8/28/2007 |