PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
AmberWave Systems Corporation	11/22/2009

RECEIVING PARTY DATA

Name:	Taiwan Semiconductor Manufacturing Company, Ltd.
Street Address:	No. 8, Li-Hsin Rd. 6
Internal Address:	Science-Based Industrial Park
City:	Hsin-Chu
State/Country:	TAIWAN
Postal Code:	300-77

PROPERTY NUMBERS Total: 83

Property Type	Number
Patent Number:	6680496
Patent Number:	7217603
Patent Number:	6982474
Patent Number:	7138310
Patent Number:	7566606
Patent Number:	7439164
Patent Number:	7122449
Patent Number:	6946371
Patent Number:	7615829
Patent Number:	7138649
Patent Number:	7109516
Patent Number:	7074623
Patent Number:	7420201
Patent Number:	7414259

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Patent Number:	7259388
Patent Number:	6995430
Patent Number:	7297612
Patent Number:	7588994
Patent Number:	7335545
Patent Number:	7307273
Patent Number:	7410861
Patent Number:	7408214
Patent Number:	6891209
Patent Number:	6838728
Patent Number:	6974735
Patent Number:	7465619
Patent Number:	6831292
Patent Number:	6933518
Patent Number:	7259108
Patent Number:	7060632
Patent Number:	7041170
Patent Number:	6518644
Patent Number:	6864115
Patent Number:	6503773
Patent Number:	6703144
Patent Number:	6602613
Patent Number:	6750130
Patent Number:	6969875
Patent Number:	6555839
Patent Number:	6593191
Patent Number:	6645829
Patent Number:	6677655
Patent Number:	6680495
Patent Number:	7217668
Patent Number:	6846715
Patent Number:	6583015
Patent Number:	6649480
Patent Number:	6881632
Patent Number:	6594293

Patent Number:	6589335
Patent Number:	6724008
Patent Number:	6677192
Patent Number:	6703688
Patent Number:	7501351
Patent Number:	7256142
Patent Number:	6723661
Patent Number:	6646322
Patent Number:	6900103
Patent Number:	6593641
Patent Number:	6830976
Patent Number:	6849508
Patent Number:	7172935
Patent Number:	6900094
Patent Number:	7049627
Patent Number:	7368308
Patent Number:	7375385
Patent Number:	6991972
Patent Number:	7074655
Patent Number:	7326599
Patent Number:	7494881
Patent Number:	7071014
Patent Number:	7208332
Patent Number:	7416909
Patent Number:	7202121
Patent Number:	7541208
Patent Number:	7594967
Patent Number:	7332417
Patent Number:	6960781
Patent Number:	7504704
Patent Number:	7393733
Patent Number:	7432139
Patent Number:	7626246
Patent Number:	7638842

CORRESPONDENCE DATA

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NAME OF SUBMITTER:	Natalie Swider

Total Attachments: 16
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EXHIBIT B

PATENT ASSIGNMENT

THIS ASSIGNMENT (the "Assignment"), effective as of November 22, 2009 is made by and between by and between Taiwan Semiconductor Manufacturing Company, Ltd., a Taiwan, Republic of China corporation ("Assignee"), and AmberWave Systems Corporation, a Delaware corporation (the "Assignor"). Assignee and Assignor are referred to herein as the "Parties" and each individually as a "Party."

WITNESSETH:

WHEREAS, the Parties entered into that certain Asset Purchase Agreement, dated as of November 22, 2009, by and among, Assignor and Assignee (the "Purchase Agreement");

WHEREAS, pursuant to the Purchase Agreement, Assignor agreed to transfer to Assignee all of the right, title and interest of Assignor in and to certain assets, properties, rights and interests, including without limitation, certain Patent Rights (as defined in the Purchase Agreement);

WHEREAS, Assignee is desirous of acquiring (and Assignor is desirous of assigning to Assignee) the entire right, title and interest in and to the Patent Rights and the inventions disclosed and/or claimed in the Patent Rights, and in and to any and all Letters Patents worldwide which may be obtained therefor;

NOW, THEREFORE, for and in consideration of the sum of one dollar ($1.00) and other good and valuable consideration, the receipt of which is hereby acknowledged:

1. Assignor does hereby sell, assign, transfer, and convey to Assignee free and clear of all liens or other encumbrances[, except for those Encumbrances (as such term is defined in the Purchase Agreement) listed in Exhibit D to the Purchase Agreement], and to the maximum extent provided under law, all of Assignor's entire worldwide right, title and interest in, to, and under the Patent Rights, the same to be held and enjoyed by Assignee for its own use and enjoyment and the use and enjoyment of its successors, assigns or other legal representatives, as fully and entirely as the same would have been held and enjoyed by Assignor if this assignment and sale had not been made, as assignee of its entire right, title and interest therein and in and to all income, royalties, damages and payments now or hereafter due or payable with respect thereto in and to all causes of action (either in law or in equity) and the right to sue, counterclaim, and recover for past, present and future infringement of the rights assigned or to be assigned under this Assignment.

2. Assignor hereby covenants and agrees that Assignor will not execute any writing or do any act whatsoever conflicting with this Assignment, and that Assignor will, at any time upon request, without further or additional consideration but at the expense of Assignee, execute such additional assignments and other writings and do such additional acts as Assignee

may deem necessary or desirable to perfect Assignee's enjoyment of this grant, and render all necessary or desirable assistance in making application for and obtaining original, divisional, continuations, continuation-in-part, reexamined, reissued, or extended letters patent or of any and all foreign countries on said inventions, and in enforcing any rights or causes of action accruing as a result of such applications or patents, by giving testimony in any proceedings or transactions involving such applications or patents, and/or by executing preliminary statements and other affidavits.

3. The Parties authorize and request that the Commissioner of Patents and Trademarks of the United States, and the corresponding entities or agencies in any applicable foreign countries, record Assignee as the owner of record for the Patent Rights and issue the patent for the pending Patent Rights to the Assignee upon issuance.

4. All disputes, claims or controversies arising out of this Assignment, or the negotiation, validity or performance of this Assignment, or the transactions contemplated hereby shall be governed by and construed in accordance with the laws of the State of Delaware without regard to its rules of conflict of laws.

5. This Assignment shall be binding upon and inure to the benefit of the Parties and their respective successors and assigns.

6. If any provision of this Assignment or the application of any such provision to any person or circumstance shall be held invalid, illegal or unenforceable in any respect by a court of competent jurisdiction, such invalidity, illegality or unenforceability shall not affect any other provision hereof.

7. This Assignment may be executed in two (2) counterparts, each of which when so executed and delivered shall be deemed an original, and such counterparts together shall constitute one and the same instrument.

IN WITNESS WHEREOF, Assignor and Assignee have caused this Assignment to be duly executed in duplicate originals by their duly authorized representative as of the day and year first above written.

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AMBERWAVE SYSTEMS CORPORATION
(as Assignor)

By: _____
Name: Richard Faubert
Title: CEO and Chairman

Sworn to and subscribed before me
this 23 day of November, 2009.

_____
Notary Public
My Commission Expires: May 28, 2011

OFFICIAL SEAL
EMILY KIRTLEY
NOTARY PUBLIC - OREGON
COMMISSION NO. 417831
MY COMMISSION EXPIRES MAY 28, 2011

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.
(as Assignee)

By: _____
Name: Richard Thurston
Title: Vice President and General Counsel

Sworn to and subscribed before me
this _____ day of November, 2009.

_____
Notary Public
My Commission Expires: _____

Exhibit A

Patent Rights

Technology	Docket #	Docket Suffix	Patent #	App. #	Title	Country	Grant back
Strain	001		6680496	10-191006	Back-biasing to populate strained layer quantum wells	US	No
Strain	002	D1	7217603	11-073976	Methods of forming reacted conductive gate electrodes	US	No
Strain	002		6982474	10-179079	Reacted conductive gate electrodes	US	No
Strain	002	C1		10-944618	Reacted conductive gate electrodes	US	No
Strain	003		7138310	10-456926	Semiconductor devices having strained dual channel layers	US	No
Strain	003	D1	7566606	11-544245	Semiconductor devices having strained dual channel layers	US	No
Strain	004	C2	7439164	11-489787	Methods of fabricating semiconductor structures having epitaxially grown source and drain elements	US	No
Strain	004	C1	7122449	11-103681	Methods of fabricating semiconductor structures having epitaxially grown source and drain elements	US	No
Strain	004		6946371	10-458544	Methods of fabricating semiconductor structures having epitaxially grown source and drain elements	US	No
Strain	005		7615829	10-164988	Elevated source and drain elements for strained channel heterojunction field-effect transistors	US	No
Strain	006		7138649	10-164665	Dual-channel CMOS transistors with differentially strained channels	US	No
Strain	006	C1		11-498521	Methods for forming semiconductor structures with differential surface layer thicknesses	US	Applies
Strain	008	D1		11-073780	METHODS OF FORMING STRAINED-SEMICONDUCTOR-ON-INSULATOR DEVICE STRUCTURES	US	No
Strain	008B	D1	7109516	11-211933	Strained-semiconductor-on-insulator finFET device structures	US	No

Technology	Docket #	Docket Suffix	Patent #	App. #	Title	Country	Grant back
Strain	008B		7074623	10-456708	Methods of forming strained-semiconductor-on-insulator finFET device structures	US	No
Strain	008C	C1	7420201	11-125507	Strained-semiconductor-on-insulator device structures with elevated source/drain regions	US	Applies
Strain	008C	C3	7414259	11-126550	Strained germanium-on-insulator device structures	US	Applies
Strain	008C	C2	7259388	11-120675	Strained-semiconductor-on-insulator device structures	US	Applies
Strain	008C		6995430	10-456103	Strained-semiconductor-on-insulator device structures	US	Applies
Strain	008C	D1C1		11-943188	METHODS FOR FORMING III-V SEMICONDUCTOR DEVICE STRUCTURES	US	Applies
Strain	008C	D1	7297612	11-127508	Methods for forming strained-semiconductor-on-insulator device structures by use of cleave planes	US	Applies
Strain	008C	D2	7588994	11-128628	Methods for forming strained-semiconductor-on-insulator device structures by mechanically inducing strain	US	Applies
Strain	008CCPCPB		7335545	11-227529	Control of strain in device layers by prevention of relaxation	US	No
Strain	008CCPCPA		7307273	11-227472	Control of strain in device layers by selective relaxation	US	No
Strain	013	C2	7410861	10-966959	Methods of forming dynamic random access memory trench capacitors	US	No
Strain	013	C1	7408214	10-947909	Dynamic random access memory trench capacitors	US	No
Strain	013		6891209	10-218007	Dynamic random access memory trench capacitors	US	No
Strain	013	C3		12-167828	METHODS OF FORMING DYNAMIC RANDOM ACCESS MEMORY TRENCH CAPACITORS	US	No
Strain	014		6838728	10-216091	Buried-channel devices and substrates for fabrication of semiconductor-based devices	US	Applies

Technology	Docket #	Docket Suffix	Patent #	App. #	Title	Country	Grant back
Strain	014	RX		95-000174	BURIED-CHANNEL DEVICES AND SUBSTRATES FOR FABRICATION OF SEMICONDUCTOR-BASED DEVICES	US	Applies
Strain	015		6974735	10-216085	Dual layer Semiconductor Devices	US	No
Strain	015	C1	7465619	11-130575	Methods of fabricating dual layer semiconductor devices	US	No
Strain	015	JP		2003-3519990	Dual layer Semiconductor Devices	JP	No
Strain	017		6831292	10-251424	Semiconductor structures employing strained material layers with defined impurity gradients and methods for fabricating same	US	Applies
Strain	017	C1		10-972578	Semiconductor structures employing strained material layers with defined impurity gradients and methods for fabricating same	US	Applies
Strain	017	CD1		11-847721	SEMICONDUCTOR STRUCTURES EMPLOYING STRAINED MATERIAL LAYERS WITH DEFINED IMPURITY GRADIENTS AND METHODS FOR FABRICATING SAME	US	Applies
Strain	017	JP D1		2009-15096	Semiconductor structures employing strained material layers with defined impurity gradients and methods for fabricating same	JP	Applies
Strain	017	CDC1		11-848642	SEMICONDUCTOR STRUCTURES EMPLOYING STRAINED MATERIAL LAYERS WITH DEFINED IMPURITY GRADIENTS AND METHODS FOR FABRICATING SAME	US	Applies
Strain	018		6933518	10-253361	RF circuits including transistors having strained material layers	US	Applies
Strain	018	C1		11-032413	RF circuits including transistors having strained material layers	US	Applies
Strain	019	C1	7259108	11-362892	Methods for fabricating	US	Applies

Technology	Docket #	Docket Suffix	Patent #	App. #	Title	Country	Grant back
					strained layers on semiconductor substrates		
Strain	019		7060632	10-389003	Methods for fabricating strained layers on semiconductor substrates	US	Applies
Strain	028	CP1	7041170	10-392338	METHOD OF PRODUCING HIGH QUALITY RELAXED SILICON GERMANIUM LAYERS	US	Applies
Strain	028	CP1C1		11-371442	Method of producing high quality relaxed silicon germanium layers	US	Applies
Strain	028	CPEP		4757731.7	Methods for fabricating strained layers on semiconductor substrates	EP	Applies
Strain	029		6518644	09-761508	LOW THREADING-DISLOCATION DENSITY RELAXED MISMATCHED EPI LAYERS WITHOUT HIGH TEMPERATURE GROWTH	US	No
Strain	029	RX		95-000158	LOW THREADING-DISLOCATION DENSITY RELAXED MISMATCHED EPI LAYERS WITHOUT HIGH TEMPERATURE GROWTH	US	No
Strain	030	C1	6864115	10-268025	Low threading dislocation density relaxed mismatched epilayers without high temperature growth	US	Applies
Strain	030		6503773	09-761497	Low threading dislocation density relaxed mismatched epilayers without high temperature growth	US	Applies
Strain	030	C1RX		95-000177	LOW THREADING DISLOCATION DENSITY RELAXED MISMATCHED EPILAYERS WITHOUT HIGH TEMPERATURE GROWTH	US	Applies
Strain	030	RX		95-000149	LOW THREADING DISLOCATION DENSITY RELAXED MISMATCHED EPILAYERS WITHOUT HIGH TEMPERATURE GROWTH	US	Applies
Strain	031	C1	6703144	10-391086	Heterointegration of materials using deposition	US	Applies

Technology	Docket #	Docket Suffix	Patent #	App. #	Title	Country	Grant back
					and bonding		
Strain	031		6602613	09-764182	Heterointegration of materials using deposition and bonding	US	Applies
Strain	031	C1RX	6703144	95-000170	HETEROINTEGRATION OF MATERIALS USING DEPOSITION AND BONDING	US	Applies
Strain	032		6750130	09-764177	Heterointegration of materials using deposition and bonding	US	Applies
Strain	032	RX	6750130	95-000180	HETEROINTEGRATION OF MATERIALS USING DEPOSITION AND BONDING	US	Applies
Strain	034		6969875	09-859139	Buried channel strained silicon FET using a supply layer created through ion implantation	US	No
Strain	035		6555839	09-859138	Buried channel strained silicon FET using a supply layer created through ion implantation	US	No
Strain	036		6593191	09-859137	Buried channel strained silicon FET using a supply layer created through ion implantation	US	No
Strain	037	DE	60124766	1956069.7	Silicon wafer with embedded optoelectronic material for monolithic	DE	Applies
Strain	037	EP	1350290	1956069.7	Silicon wafer with embedded optoelectronic material for monolithic OEIC	EP	Applies
Strain	037	FR	1350290	1956069.7	Silicon wafer with embedded optoelectronic material for monolithic OEIC	FR	Applies
Strain	037	GP	1350290	1956069.7	Silicon wafer with embedded optoelectronic material for monolithic OEIC	GP	Applies
Strain	037	IT	1350290	1956069.7	Silicon wafer with embedded optoelectronic material for monolithic OEIC	IT	Applies
Strain	037	JP		2002-518590	Silicon wafer with embedded optoelectronic material for monolithic OEIC	JP	Applies
Strain	038		6645829	09-920520	Silicon wafer with embedded optoelectronic material for monolithic OEIC	US	Applies

Technology	Docket #	Docket Suffix	Patent #	App. #	Title	Country	Grant back
Strain	039		6677655	09-920075	Silicon wafer with embedded optoelectronic material for monolithic OEIC	US	Applies
Strain	040		6680495	09-920519	Silicon wafer with embedded optoelectronic material for monolithic OEIC	US	Applies
Strain	042	C2	7217668	11-013838	Gate technology for strained surface channel and strained buried channel MOSFET devices	US	Applies
Strain	042	C1	6846715	10-421154	Gate technology for strained surface channel and strained buried channel MOSFET devices	US	Applies
Strain	042		6583015	09-923207	Gate technology for strained surface channel and strained buried channel MOSFET devices	US	Applies
Strain	042	C1RX	6846715	95-000150	Gate technology for strained surface channel and strained buried channel MOSFET devices	US	Applies
Strain	044		6649480	09-884172	Method of fabricating CMOS inverter and integrated circuits utilizing strained silicon surface channel MOSFETs	US	No
Strain	044	RX	6649480	95-000194	Method of fabricating CMOS inverter and integrated circuits utilizing strained silicon surface channel MOSFETs	US	No
Strain	044	C1	6881632	10-611739	Method of fabricating CMOS inverter and integrated circuits utilizing strained surface channel MOSFETS	US	No
Strain	044	C2		10-953260	Method of fabricating CMOS inverter and integrated circuits utilizing strained surface channel MOSFETs	US	No
Strain	044	C4		12-573,589	Method of fabricating CMOS inverter and integrated circuits utilizing strained surface channel MOSFETs	US	No
Strain	045		6594293	09-779917	Relaxed InxGa1-xAs layers integrated with Si	US	Applies
Strain	046		6589335	09-779915	Relaxed InxGa1-xAs layers integrated with Si	US	Applies

Technology	Docket #	Docket Suffix	Patent #	App. #	Title	Country	Grant back
Strain	047		6724008	09-906551	Relaxed silicon germanium platform for high speed CMOS electronics and high speed analog circuits	US	Applies
Strain	048		6677192	09-906545	Method of fabricating a relaxed silicon germanium platform having planarizing for high speed CMOS electronics and high speed analog circuits	US	Applies
Strain	049		6703688	09-906200	Relaxed silicon germanium platform for high speed CMOS electronics and high speed analog circuits	US	Applies
Strain	049	C1	7501351	10-774890	Relaxed SiGe platform for high speed CMOS electronics and high speed analog circuits	US	Applies
Strain	049	C2	7256142	10-967998	Relaxed SiGe platform for high speed CMOS electronics and high speed analog circuits	US	Applies
Strain	049	RX		90-008159	Relaxed silicon germanium platform for high speed CMOS electronics and high speed analog circuits	US	Applies
Strain	050		6723661	09-906201	Relaxed silicon germanium platform for high speed CMOS electronics and high speed analog circuits	US	Applies
Strain	051		6646322	09-906438	Relaxed silicon germanium platform for high speed CMOS electronics and high speed analog circuits	US	Applies
Strain	052		6900103	09-906533	Relaxed silicon germanium platform for high speed CMOS electronics and high speed analog circuits	US	Applies
Strain	053		6593641	09-906550	Relaxed silicon germanium platform for high speed CMOS electronics and high speed analog circuits	US	Applies
Strain	054		6830976	09-906534	Relaxed silicon germanium platform for high speed CMOS electronics and high speed analog circuits	US	Applies

Technology	Docket #	Docket Suffix	Patent #	App. #	Title	Country	Grant back
Strain	054	C2		11-412262	Methods of fabricating contact regions for FET incorporating SiGe	US	Applies
Strain	054	C1		10-854556	Methods of fabricating contact regions for FET incorporating SiGe	US	Applies
Strain	055		6849508	10-165014	Method of forming multiple gate insulators on a strained semiconductor heterostructure	US	No
Strain	055	C1	7172935	11-015266	Method of forming multiple gate insulators on a strained semiconductor heterostructure	US	No
Strain	057		6900094	10-172542	Method of selective removal of SiGe alloys	US	Applies
Strain	057	RX		95-000175	Method of selective removal of SiGe alloys	US	Applies
Strain	058A		7049627	10-647074	Semiconductor heterostructures and related methods	US	Applies
Strain	058A	C1	7368308	11-227770	Methods of fabricating semiconductor heterostructures	US	Applies
Strain	058B		7375385	10-646353	Semiconductor heterostructures having reduced dislocation pile-ups	US	Applies
Strain	058B	C1		11-941629	SEMICONDUCTOR HETEROSTRUCTURES HAVING REDUCED DISLOCATION PILE-UPS AND RELATED METHODS	US	Applies
Strain	058	EP		3759202.9	SEMICONDUCTOR HETEROSTRUCTURES HAVING REDUCED DISLOCATION PILE-UPS AND RELATED METHODS	EP	Applies
Strain	058	JP		2004-529920	SEMICONDUCTOR HETEROSTRUCTURES HAVING REDUCED DISLOCATION PILE-UPS AND RELATED METHODS	JP	Applies
Strain	060		6991972	10-691007	Gate material for semiconductor device fabrication	US	No
Strain	060	C1	7074655	11-237175	Gate material for semiconductor device fabrication	US	No
Strain	060	C1RX		90-008153	Gate material for semiconductor device	US	No

Technology	Docket #	Docket Suffix	Patent #	App. #	Title	Country	Grant back
					fabrication		
Strain	060	C2	7326599	11-436281	Gate material for semiconductor device fabrication	US	No
Strain	060	EP		3809619.4	Gate material for semiconductor device fabrication	EP	No
Strain	060	JP		2004-547063	Gate material for semiconductor device fabrication	JP	No
Strain	061	D1	7494881	11-945130	Methods for Selective Placement of Dislocation Arrays	US	Applies
Strain	063		7071014	10-696994	Methods for preserving strained semiconductor substrate layers during CMOS processing	US	No
Strain	063	D1	7208332	11-132856	Methods for preserving strained semiconductor substrate layers during CMOS processing	US	No
Strain	063	D1C1	7416909	11-702825	Methods for preserving strained semiconductor substrate layers during CMOS processing	US	No
Strain	063	D2	7202121	11-371687	Methods for preserving strained semiconductor substrate layers during CMOS processing	US	No
Strain	063	D2C1	7541208	11-704464	Methods for preserving strained semiconductor substrate layers during CMOS processing	US	No
Strain	063	JP		2004-571905	Methods for preserving strained semiconductor substrate layers during CMOS processing	JP	No
Strain	065		7594967	10-268425	Reduction of dislocation pile-up formation during relaxed lattice-mismatched epitaxy	US	Applies
Strain	066		7332417	10-765372	Semiconductor structures with structural homogeneity	US	Applies
Strain	066	EP		47056994	SEMICONDUCTOR STRUCTURES WITH STRUCTURAL HOMOGENEITY	EP	Applies
Strain	066	JP		2006-503082	SEMICONDUCTOR STRUCTURES WITH STRUCTURAL HOMOGENEITY	JP	Applies

Technology	Docket #	Docket Suffix	Patent #	App. #	Title	Country	Grant back
Strain	071		6960781	10-794010	Shallow trench isolation process	US	No
Strain	071	C1	7504704	11-130584	Shallow trench isolation process	US	No
Strain	071	CN	ZL200480010 1670	2004-80101670	Shallow trench isolation process	CN	No
Strain	071	EP		4718094.8	Shallow trench isolation process	EP	No
Strain	071	HK		6111860.8	Shallow trench isolation process	HK	No
Strain	071	JP		2006-509191	Shallow trench isolation process	JP	No
Strain	071	KR	728173	1020057016595	Shallow trench isolation process	KR	No
Strain	085B		7393733	11-001166	Methods of forming hybrid fin field-effect transistor structures	US	No
Strain	085B	C1		12-125308	HYBRID FIN FIELD-EFFECT TRANSISTOR STRUCTURES AND RELATED METHODS	US	No
Strain	088A		7432139	11-170250	Methods for forming dielectrics and metal electrodes	US	No
Strain	098			11-861931	TRI-GATE FIELD-EFFECT TRANSISTORS FORMED BY ASPECT RATIO TRAPPING	US	No
Strain	102			11-952514	Inducement of Strain in a Semiconductor Layer	US	No
ART	ASC-30 01			12-476460	Improved Epitaxial Growth of Crystalline Material	US	Applies
ART	ASC-30 02			12-495161	Reduction of Edge Effects from Aspect Ratio Trapping	US	Applies
ART	ASC-30 03			12-503597	Polishing of Small Composite Semiconductor Materials	US	Applies
ART	ASC-30 04			12-562206	Improved Fabrication and Structures of Crystalline Materials	US	Applies
ART	ASC-30 05			12-565863	Improved Semiconductor Sensor Structures with Reduced Dislocation Defect Densities and Related Methods for the Same	US	Applies
ART	ASC-30 06	PC		PCT/US09/57493	FORMATION OF DEVICES BY EPITAXIAL LAYER OVERGROWTH	PCT	Applies

Technology	Docket #	Docket Suffix	Patent #	App #	Title	Country	Grant back
ART	AMD-107	PR		61-166184	DEVICES FORMED FROM A NON-POLAR PLANE OF A CRYSTALLING MATERIAL AND METHOD OF MAKING THE SAME	US	Applies
ART	AMD-108	PR		61-143589	DIODE-BASED DEVICES AND METHODS FOR MAKING THE SAME	US	Applies
ART	AMD-109	PR		61-143602	Semiconductor Diodes Fabricated by Aspect Ratio Trapping with Coalesced Films	US	Applies
ART	086A	CP1		12-180254	Lattice-mismatched semiconductor structures with reduced dislocation defect densities and related methods for device fabrication	US	Applies
ART	086B			11-436062	Lattice-mismatched semiconductor structures with reduced dislocation defect densities and related methods for device fabrication	US	Applies
ART	086	EP		6770525.1	Lattice-mismatched semiconductor structures with reduced dislocation defect densities and related methods for device fabrication	EP	Applies
ART	086	JP		2008-512484	Lattice-mismatched semiconductor structures with reduced dislocation defect densities and related methods for device fabrication	JP	Applies
ART	086	KR		10-2007-7029364	Lattice-mismatched semiconductor structures with reduced dislocation defect densities and related methods for device fabrication	KR	Applies
ART	086	CN		200680023212.5	Lattice-mismatched semiconductor structures with reduced dislocation defect densities and related methods for device fabrication	CN	Applies
ART	090			11-493365	Solutions for integrated circuit integration of alternative active area materials	US	Applies

Technology	Docket #	Docket Suffix	Patent #	App. #	Title	Country	Grant back
ART	090	EP		6800414.2	Solutions for integrated circuit integration of alternative active area materials	EP	Applies
ART	091B			11-220482	Lattice-mismatched semiconductor structures on insulators	US	Applies
ART	094			11-728032	Lattice-mismatched semiconductor structures and related methods for device fabrication	US	Applies
ART	099			11-862850	QUANTUM TUNNELING DEVICES AND CIRCUITS WITH LATTICE-MISMATCHED SEMICONDUCTOR STRUCTURES	US	Applies
ART	101			11-875381	Light-Emitter-Based Devices with Lattice-Mismatched Semiconductor Structures	US	Applies
ART	104			11-852078	Defect Reduction Using Aspect Ratio Trapping	US	Applies
ART	104	EP		7837902.1	Defect Reduction Using Aspect Ratio Trapping	EP	Applies
ART	105			12-031338	NITRIDE-BASED MULTI-JUNCTION SOLAR CELL MODULES AND METHODS FOR MAKING THE SAME	US	Applies
ART	106			12-100131	PHOTOVOLTAICS ON SILICON	US	Applies
ART	107			12-139010	IN-P-BASED TRANSISTOR FABRICATION	US	Applies
ART	110			12-147027	MULTI-JUNCTION SOLAR CELLS	US	Applies
ART	090	JP		2008-524,156	Solutions for integrated circuit integration of alternative active area materials	JP	Applies
ART	090	KR		10-2008-7004519	Solutions for integrated circuit integration of alternative active area materials	KR	Applies
ART	104	HK		T.B.D.	Defect Reduction Using Aspect Ratio Trapping	HK	Applies
Strain	028	CPEP		1604391(A1)	Method of producing high quality relaxed silicon germanium layers	EP	Applies
Strain	028	CPJP		2006523380(T)	Method of producing high quality relaxed silicon germanium layers	JP	Applies

Technology	Docket #	Docket Suffix	Patent #	App. #	Title	Country	Grant back
ART	090	CN		101268547(A)	Solutions for integrated circuit integration of alternative active area materials	CN	Applies
ART	110	PCT		US08/68377	MULTI-JUNCTION SOLAR CELLS	PCT	Applies
Strain	015	EP		02761307.4	Dual layer Semiconductor Devices	EP	No

All foreign counter-parts of the above listed applications and/or patents, whether explicity listed here or not, are included in the Patent Rights.