# PATENT ASSIGNMENT

Electronic Version v1.1
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| SUBMISSION TYPE: | NEW ASSIGNMENT |
| NATURE OF CONVEYANCE: | SECURITY AGREEMENT |

CONVEYING PARTY DATA

| Name | Execution Date |
|---|---|
| CALIFORNIA MICRO DEVICES CORPORATION | 02/25/2010 |

RECEIVING PARTY DATA

| | |
|---|---|
| Name: | JPMORGAN CHASE BANK, N.A., as collateral agent |
| Street Address: | 270 Park Avenue |
| City: | New York |
| State/Country: | NEW YORK |
| Postal Code: | 10017 |

PROPERTY NUMBERS Total: 54

| Property Type | Number |
|---|---|
| Patent Number: | 6642550 |
| Patent Number: | 6121669 |
| Patent Number: | 5706163 |
| Patent Number: | 5652460 |
| Patent Number: | 5760662 |
| Patent Number: | 6262434 |
| Patent Number: | 5998275 |
| Patent Number: | 6281564 |
| Patent Number: | RE38550 |
| Patent Number: | 6307395 |
| Patent Number: | 6100713 |
| Patent Number: | 6326805 |
| Patent Number: | 6331787 |
| Patent Number: | 6329837 |
| Patent Number: | 6331786 |

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|---|---|
| Patent Number: | 6323676 |
| Patent Number: | 6326804 |
| Patent Number: | 6323675 |
| Patent Number: | 6285246 |
| Patent Number: | 6452478 |
| Patent Number: | 6031423 |
| Patent Number: | 6285091 |
| Patent Number: | 6201679 |
| Patent Number: | 6512393 |
| Patent Number: | 6556040 |
| Patent Number: | 6008665 |
| Patent Number: | 6747476 |
| Patent Number: | 5514612 |
| Patent Number: | 5355014 |
| Patent Number: | 5788854 |
| Patent Number: | 5370766 |
| Patent Number: | 5770886 |
| Patent Number: | 5291074 |
| Patent Number: | 5450263 |
| Patent Number: | 7412870 |
| Patent Number: | 7002387 |
| Patent Number: | 7446565 |
| Patent Number: | 7321241 |
| Patent Number: | 7479680 |
| Patent Number: | 6707280 |
| Patent Number: | 7541251 |
| Patent Number: | 7576370 |
| Patent Number: | 7057310 |
| Application Number: | 11206667 |
| Application Number: | 11371175 |
| Application Number: | 12476847 |
| Application Number: | 11566022 |
| Application Number: | 11564241 |
| Application Number: | 11738176 |
| Application Number: | 11685085 |

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|---|---|
| Application Number: | 12180440 |
| Application Number: | 12014725 |
| Application Number: | 12332159 |
| Application Number: | 12434805 |

CORRESPONDENCE DATA


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|---|---|
| ATTORNEY DOCKET NUMBER: | 35496 |
| NAME OF SUBMITTER: | Penelope J.A. Agodoa |

Total Attachments: 9

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PATENT SECURITY AGREEMENT, dated as of February 25, 2010, between CALIFORNIA MICRO DEVICES CORPORATION, a Delaware corporation and JPMORGAN CHASE BANK, N.A., a national banking association as collateral agent (the "Collateral Agent").

Reference is made to the Security Agreement dated as of August 4, 1999, as amended and restated as of March 3, 2003 (as amended, supplemented or otherwise modified from time to time, the "Security Agreement"), among Semiconductor Components Industries, LLC, a Delaware limited liability company, ON Semiconductor Corporation, a Delaware corporation, the Subsidiary Loan Parties and the Collateral Agent. The Lenders have agreed to extend credit to the Borrower subject to the terms and conditions set forth in the Credit Agreement dated as of August 4, 1999, as amended and restated as of March 6, 2007 (as amended, supplemented or otherwise modified from time to time (the "Credit Agreement")). The obligations of the Lenders to continue to extend such credit are conditioned upon, among other things, the execution and delivery of this Patent Security Agreement (this "Agreement"). Accordingly, the parties hereto agree as follows:

SECTION 1. Terms. Capitalized terms used in this Agreement and not otherwise defined herein have the meanings specified in the Security Agreement. The rules of construction specified in Section 1.03 of the Security Agreement also apply to this Agreement.

SECTION 2. Grant of Security Interest. As security for the payment or performance, as the case may be, in full of the Obligations, each Grantor, pursuant to the Security Agreement, did and hereby does grant to the Collateral Agent, its successors and assigns, for the benefit of the Secured Parties, a security interest in, all right, title or interest in or to any and all of the following assets and properties now owned or at any time hereafter acquired by such Grantor or in which such Grantor now has or at any time in the future may acquire any right, title or interest (collectively, the "Patent Collateral"):

(a) all letters patent of the United States or any other country, all registrations and recordings thereof, and all applications for letters patent of the United States or any other country, including registrations, recordings and pending applications in the United States Patent and Trademark Office or any similar offices in any other country, including those listed on Schedule 1 (the "Patents"), and all reissues, continuations, divisions, continuations-in-part, renewals or extensions thereof, and the inventions disclosed or claimed therein, including the right to make, use and/or sell the inventions disclosed or claimed therein.

SECTION 3. Termination. This Agreement is made to secure the satisfactory performance and payment of the Obligations. Upon termination of the Security Agreement or release of a Grantor's obligations thereunder, this Agreement shall automatically terminate as to such Grantor.

SECTION 4. Security Agreement. The security interests granted to the Collateral Agent herein are granted in furtherance, and not in limitation of, the security interests granted to the Collateral Agent pursuant to the Security Agreement. Each Grantor hereby acknowledges and affirms that the rights and remedies of the Collateral Agent with respect to the Patent Collateral are more fully set forth in the Security Agreement, the terms and provisions of which are hereby incorporated herein by reference as if fully set forth herein. In the event of any conflict between the terms of this Agreement and the Security Agreement, the terms of the Security Agreement shall govern.

IN WITNESS WHEREOF, the parties hereto have duly executed this Agreement as of the day and year first above written.

CALIFORNIA MICRO DEVICES CORPORATION

by

Name: Donald A. Colvin
Title: Director & Treasurer

JPMORGAN CHASE BANK, N.A., as Collateral Agent,

by

Name:
Title:

IN WITNESS WHEREOF, the parties hereto have duly executed this Agreement as of the day and year first above written.

CALIFORNIA MICRO DEVICES CORPORATION

by

_____

Name:
Title:

JPMORGAN CHASE BANK, N.A., as Collateral Agent,

by

_____

Name:
Title: Ann B. Kerns
Vice President

[[NYCORP:3199335]]

## SCHEDULE 1

Patents and Trademarks

I. Registered U.S. Trademarks.

| *Mark* | *Registration No.* | *Registration Date* |
|---|---|---|
| C.MD DESIGN | 3617486 | 05-05-2009 |
| PICOGUARD | 3548014 | 12-16-2008 |
| PRAETORIAN | 3136826 | 08-29-2006 |
| XTREMEESD | 3555054 | 12-30-2008 |
| LUXGUARD | 3741111 | 01-19-2010 |

II. U.S. Trademarks Applied For and Registration Pending.

| *Description* | *Application No.* | *Filing Date* |
|---|---|---|
| LUXGUARD | 77/695150 | 03-19-2009 |

III. Trademark Licenses. See **Annex 1** attached hereto.

IV. Registered U.S. Patents.

| *Description* | *Patent No.* | *Issue Date* |
|---|---|---|
| Silicon Sub Mount Capable of Single Wire Bonding and of Providing ESD Protection for Light Emitting Diode Devices | 6642550 | 11/4/2003 |
| ESD Protected Thin Film Capacitor Structures | 6121669 | 9/19/2000 |
| ESD Protected Thin Film Capacitor Structures | 5706163 | 1/6/1998 |
| Integrated Resistor Networks Having Reduced Cross Talk | 5652460 | 7/29/1997 |
| Methods and Apparatus for Improving Frequency Response of Integrated RC Filters with Additional Ground Pins | 5760662 | 6/2/1998 |
| Integrated Circuit Structures and Methods to Facilitate Accurate Measurement of the IC Devices | 6262434 | 7/17/2001 |
| Method for Programmable Integrated Passive Devices | 5998275 (reissued) | 12/7/1999 |
| Programmable Integrated Passive Devices | 6281564 And RE38550 | 8/28/2001 7/6/2004 |
| Termination Circuits and Methods for Bused and Networked Devices | 6307395 | 10/23/2001 |
| Termination Circuits and Methods for Memory Buses and Devices | 6100713 | 8/8/2000 |
| Termination Circuits and Methods therefore | 6326805 | 12/4/2001 |
| Termination Circuits and Methods therefore | 6331787 | 12/18/2001 |

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|---|---|---|
| Termination Circuits and Methods therefore | 6329837 | 12/11/2001 |
| Termination Circuits and Methods therefore | 6331786 | 12/18/2001 |
| Termination Circuits and Methods therefore | 6323676 | 11/27/2001 |
| Termination Circuits and Methods therefore | 6326804 | 12/4/2001 |
| Termination Circuits and Methods therefore | 6323675 | 11/27/2001 |
| Low Drop Out Regulator Capable of Functioning in Linear and Saturated Regions of Output Driver | 6285246 | 9/4/2001 |
| Voltage Trimmable Resistor | 6452478 | 9/17/2002 |
| Input Stage for Rail to Rail Input Amp | 6031423 | 2/29/2000 |
| Voltage Source Switching Circuit at Reduced Voltage Drop Levels | 6285091 | 9/4/2001 |
| Integrated Electrical Overload Protection Device and Method of Formation | 6201679 | 3/13/2001 |
| Method and Apparatus for Non Linear Termination of a Transmission Line | 6512393 | 1/28/2003 |
| Method and Apparatus for Non Linear Termination of a Transmission Line | 6556040 | 4/29/2003 |
| Termination Circuits and Methods Therefor | 6008665 | 12/28/1999 |
| Method and Apparatus for Non Linear Termination of a Transmission Line | 6747476 | 6/8/2004 |
| Method of Making a Semiconductor Device with Integrated RC Network and Schottky Diode | 5514612 | 5/7/1996 |
| Method of Making a Semiconductor Device with Integrated RC Network and Schottky Diode | 5355014 | 10/11/1994 |
| Methods for Fabrication of Thin Film Inductors, Inductor Networks, Inductor/Capacitor Filters, and Integration with Other Passive and Active Devices and the Resultant Devices | 5788854 | 8/4/1998 |
| Methods for Fabrication of Thin Film Inductors, Inductor Networks and Integration with Other Passive and Active Devices | 5370766 | 12/6/1994 |
| Semiconductor Device with Integrated RC Network and Schottky Diode | 5770886 | 6/23/1998 |
| BICMOS Track and Hold Amplifier | 5291074 | 3/1/1994 |
| Thin Film Inductors, Inductor Network and Integration with Other Passive and Active Devices | 5450263 | 9/12/1995 |
| Method and Apparatus for Dynamic Impact Testing | 7412870 | 8/19/2008 |
| System and Method for Startup Bootstrap for Internal Regulators | 7002387 | 2/21/2006 |
| Apparatus and Method that Provides Active Pull Up and Logic Translation from one Signal Mode to Another Signal Mode | 7446565 | 11/4/2008 |
| Bidirectional Buffer with Slew Rate Control and Method of Bidirectionally Transmitting Signals with Slew Rate control | 7321241 | 1/22/2008 |
| Method and Apparatus that Provides Differential Connections with Improved ESD Protection and Routing | 7479680 | 1/20/2009 |
| Regulator for DDR DRAM Termination Voltage | 6707280 | 3/16/2004 |
| Wire Bond and Redistribution Layer Process | 7541251 | 6/2/2009 |
| Low Operating voltage Electrostatic Discharge Device and Method | 7576370 | 8/18/2009 |

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| Dual-Output Voltage Regulator | 7057310 | 6/6/2006 |

V. U.S. Patents Applied For and Registration Pending.

| *Description* | *Application No.* | *Filing Date* |
|---|---|---|
| Integrated Passive Filter Incorporating Inductors and ESD Protectors | 11/206,667 | 8/17/2005 |
| Low Capacitance Solder bump Interface Structure | 11/371,175 | 3/8/2006 |
| Wire Bond and Redistribution Layer Process | 12/476,847 | 6/2/2009 |
| Slaving Video Presentation | 11/566,022 | 12/1/2006 |
| High Density Inductor | 11/564,241 | 11/28/06 |
| A High Current Steering ESD Protection Zener Diode and Method | 11/738,176 | 4/20/07 |
| Method of Making Reliable Wafer Level Chip Scale Packaging Semiconductor Devices | 11/685,085 | 3/12/07 |
| Method and Apparatus for Providing 2-Stage ESD Protection for High Speed Interfaces | 12/180,440 | 7/25/08 |
| Low Pass Filter Incorporating Coupled Inductors to Enhance Stop Band Attenuation | 12/014,725 | 1/15/08 |
| Impedance Compensated ESD Circuit for Protection for High-Speed Interfaces and Method of Using the Same | 12/332,159 | 12/10/2008 |
| Method of ESD Structure Layout Using Circular Patterns | 12/434805 | 5/12/2009 |

VI. Patent Licenses. See **Annex 1** attached hereto.

VII. Registered U.S. Mask Work.

| *Title* | *Registration No.* | *Registration Date* |
|---|---|---|
| CSPEMI1306 | MW0000016904 | 05-20-2003 |

## ANNEX 1 TO SCHEDULE 1

Intellectual Property License Agreements

1. Arasan Chip Systems License Agreement between the New Grantor and Arasan Chip Systems, Inc., dated August 29, 2007. [Copyright]
2. License Agreement between the New Grantor and Mixel, Inc., dated April 22, 2009. [Patent and Copyright]
3. License Agreement between the New Grantor and True Circuits, Inc., dated August 15, 2007. [Patent and Copyright].
4. Development, Technical Support and Limited Use Agreement between the New Grantor and QUALCOMM Incorporated, dated April 29, 2009. [Copyright]
5. UMC FDK License Agreement between the New Grantor and United Microelectronics Corporation, dated June 29, 2009. [Patent and Copyright]
6. Development, Technical Support and Limited Use Agreement between the New Grantor and QUALCOMM Incorporated, dated December 17, 2004. [Patent and Copyright]
7. Specific Purpose License Agreement between the New Grantor and Cadence Design Systems, Inc., dated August 12, 2009. [Patent and Copyright]
8. End User Software License and Maintenance Agreement between the New Grantor and Synopsys, Inc., dated August 26, 2004. [Patent and Copyright]
9. Restricted Use License Agreement between the New Grantor and Intel Corporation, dated February 6, 1998.
10. Private Label Agreement between the New Grantor and Littelfuse, Inc., dated March 28, 2001. [Trademark]
11. Oracle License and Services Agreement between the New Grantor and Oracle Corporation, dated May 31, 2004, as amended by the Amendment One, dated May 31, 2004. [Patent and Copyright]
12. Settlement Agreement between the New Grantor and Advanced Micro Devices, Inc., dated November 21, 2008. [Trademark]
13. License Agreement between the New Grantor and Syndia Corporation, dated January __, 2003. [Patent]
14. Reseller Agreement between the New Grantor and GDA Technologies, Inc., dated September 11, 2009. [Patent]