PATENT ASSIGNMENT

Electronic Version v1.1
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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
LogicVision, Inc.	09/10/2009

RECEIVING PARTY DATA

Name:	Mentor Graphics Corporation
Street Address:	8005 SW Boeckman Road
City:	Wilsonville
State/Country:	OREGON
Postal Code:	97070-7777

PROPERTY NUMBERS Total: 58

Property Type	Number
Patent Number:	5349587
Patent Number:	5659312
Patent Number:	5900753
Patent Number:	6046946
Patent Number:	6115827
Patent Number:	6145105
Patent Number:	6204694
Patent Number:	6211803
Patent Number:	6327684
Patent Number:	6330681
Patent Number:	6363520
Patent Number:	6396889
Patent Number:	6442722
Patent Number:	6457161
Patent Number:	6487688

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Patent Number:	6492798
Patent Number:	6510534
Patent Number:	6536008
Patent Number:	6567971
Patent Number:	6586921
Patent Number:	6590412
Patent Number:	6614263
Patent Number:	6615392
Patent Number:	6671839
Patent Number:	6678875
Patent Number:	6691269
Patent Number:	6703820
Patent Number:	6717415
Patent Number:	6720194
Patent Number:	6725435
Patent Number:	6738938
Patent Number:	6745359
Patent Number:	6760874
Patent Number:	6763489
Patent Number:	6829730
Patent Number:	6834361
Patent Number:	6862717
Patent Number:	6868532
Patent Number:	6883134
Patent Number:	6885213
Patent Number:	6895535
Patent Number:	6961871
Patent Number:	7103860
Patent Number:	7139946
Patent Number:	7155651
Patent Number:	7158899
Patent Number:	7159159
Patent Number:	7188274
Patent Number:	7191374
Patent Number:	7194669

Patent Number:	7219282
Patent Number:	7257733
Patent Number:	7370251
Patent Number:	7424656
Patent Number:	7453255
Application Number:	11439497
Application Number:	11853383
Application Number:	61101219

CORRESPONDENCE DATA

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NAME OF SUBMITTER:	Danielle M. Duggan

Total Attachments: 6
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PATENT ASSIGNMENT

WHEREAS, LogicVision, Inc. (hereinafter Assignor), a corporation organized under the laws of Delaware, having offices at 25 Metro Drive # 300, San Jose, California 95110 warrants and states it is the sole and exclusive owner of the following patents and applications (hereinafter called the Patent Properties):

Patents				
Title		Country Code	Publication Date (Issue Date)	Publication Number (Patent Number)
1	Multiple Clock Rate Test Apparatus For Testing Digital Systems	US	20 Sept 1994	5,349,587
2	Method And Apparatus For Testing Digital To Analog And Analog To Digital Converters	US	19 Aug 1997	5,659,312
3	Asynchronous Interface	US	04 May 1999	5,900,753
4	Method And Apparatus For Testing Multi-Port Memory Using Shadow Read	US	04 April 2000	6,046,946
5	Clock Skew Management Method And Apparatus	US	05 Sept 2000	6,115,827
6	Method And Apparatus For Scan Testing Digital Circuits	US	07 Nov 2000	6,145,105
7	Programmable Clock Signal Generation Circuits And Methods For Generating Accurate, High Frequency, Clock Signals	US	30 March 2001	6,204,694
8	Test Circuit And Method For Measuring Switching Point Voltages And Integral Non-Linearity (INL) Of Analog To Digital Converters	US	03 April 2001	6,211,803
9	Method Of Testing At-Speed Circuits Having Asynchronous Clocks And Controller For Use Therewith	US	04 Dec 2001	6,327,684
10	Method And Apparatus For Controlling Power Level During BIST	US	11 Dec 2001	6,330,681
11	Method For Testability Analysis And Test Point Insertion At The Rt-Level Of A Hardware Development Language (HDL) Specification	US	26 March 2002	6,363,520
12	Method And Circuit For Built In Self Test Of Phase Locked Loops	US	28 May 2002	6,396,889
13	Method And Apparatus For Testing Circuits With Multiple Clocks	US	27 August 2002	6,442,722

14	Method And Program Product For Modeling Circuits With Latch Based Design	US	24 Sept 2002	6,457,161
15	Method For Testing Circuits With Tri-State Drivers And Circuit For Use Therewith	US	26 Nov 2002	6,487,688
16	Method And Circuit For Testing High Frequency Mixed Signal Circuits With Frequency Signals	US	10 Dec 2002	6,492,798
17	Method And Apparatus For Testing High Performance Circuits	US	21 Jan 2003	6,510,534
18	Fault Insertion Method, Boundary Scan Cells, And Integrated Circuit For Use Therewith	US	18 March 2003	6,536,008
19	Circuit Synthesis Method Using Technology Parameters Extracting Circuit	US	20 May 2003	6,567,971
20	Method And Circuit For Testing DC Parameters Of Circuit Input And Output Nodes	US	01 July 2003	6,586,921
21	Circuit And Method For Detecting Transient Voltages On A DC Power Supply Rail	US	08 July 2003	6,590,412
22	Method And Circuitry For Controlling Clocks Of Embedded Blocks During Logic BIST Test Mode	US	02 Sept 2003	6,614,263
23	Hierarchical Design And Test Method And System, Program Product Embodying The Method And Integrated Circuit Produced Thereby	US	02 Sept 2003	6,615,392
24	Scan Test Method For Providing Real Time Identification Of Failing Test Patterns And Test BIST Controller For Use Therewith	US	30 Dec 2003	6,671,839
25	Self-Contained Embedded Test Design Environment And Environment Setup Utility	US	13 Jan 2004	6,678,875
26	Method For Scan Controlled Sequential Sampling Of Analog Signals And Circuit For Use Therewith	US	10 Feb 2004	6,691,269
27	Method And Circuit For Testing High Frequency Mixed Signal Circuits With Low Frequency Signals	US	09 March 2004	6,703,820
28	Circuit And Method For Determining The Location Of Defect In A Circuit	US	06 April 2004	6,717,415
29	*Semiconductor Characterization And Production Information System*	*US*	*13 April 2004*	*6,720,194*
30	Method And Program Product For Completing A Circuit Design Having Embedded Test Structures	US	20 April 2004	6,725,435

31	Method For Collecting Failure Information For A Memory Using An Embedded Test Controller	US	18 May 2004	6,738,938
32	Method Of Masking Corrupt Bits During Signature Analysis And Circuit For Use Therewith	US	01 June 2004	6,745,359
33	Test Access Circuit And Method Of Accessing Embedded Test Controllers In Integrated Circuit Modules	US	06 July 2004	6,760,874
34	Method For Scan Testing Of Digital Circuit, Digital Circuit For Use Therewith And Program Product For Incorporating Test Methodology Into Circuit Description	US	13 July 2004	6,763,489
35	Method Of Designing Circuit Having Multiple Test Access Ports, Circuit Produced Thereby And Method Of Using Same	US	07 Dec 2004	6,829,730
36	Method Of Testing Embedded Memory Array And Embedded Memory Controller For Use Therewith	US	21 Dec 2004	6,834,361
37	Method And Program Product For Designing Hierarchical Circuit For Quiescent Current Testing	US	01 March 2005	6,862,717
38	Method And Program Product For Designing Hierarchical Circuit For Quiescent Current Testing And Circuit Produced Thereby	US	15 March 2005	6,868,532
39	Method And Program Product For Detecting Bus Conflict And Floating Bus Conditions In Circuit Designs	US	19 April 2005	6,883,134
40	Circuit And Method For Accurately Applying A Voltage To A Node Of An Integrated Circuit	US	26 April 2005	6,885,213
41	Circuit And Method For Testing High Speed Data Circuits	US	17 May 2005	6,895,535
42	Method,System And Program Product For Testing And/Or Diagnosing Circuits Using Embedded Test Controller Access Data	US	01 Nov 2005	6,961,871
43	Verification Of Embedded Test Structures In Circuit Designs	US	05 Sept 2006	7,103,860
44	Method And Test Circuit For Testing Memory Internal Write Enable	US	21 Nov 2006	7,139,946
45	Clock Controller For At-Speed Testing Of Scan Circuits	US	26 Dec 2006	7,155,651
46	Circuit And Method For Measuring Jitter Of High Speed Signals	US	02 Jan 2007	7,158,899
47	Circuit And Method For Adding Parametric Test Capability To Digital Boundary Scan	US	02 Jan 2007	7,159,159

48	Memory Repair Analysis Method And Circuit	US	06 Mar 2007	7,188,274
49	Method Of And Program Product For Performing Gate-Level Diagnosis Of Failing Vectors	US	13 Mar 2007	7,191,374
50	Method And Circuit For At-Speed Testing Of Scan Circuits	US	20 Mar 2007	7,194,669
51	Boundary Scan With Strobed Pad Driver Enable	US	15 May 2007	7,219,282
52	Memory Repair Circuit And Method	US	14 Aug 2007	7,257,733
53	Method And Circuit For Collecting Memory Failure Information	US	06 May 2008	7,370,251
54	Clocking Methodology For At-Speed Testing Of Scan Circuits With Synchronous Clocks	US	09 Sept 2008	7,424,656
55	Circuit And Method For Measuring Delay Of High Speed Signals	US	18 Nov 2008	7,453,255

Patent Applications				
Title		Country Code	Date Filed	Application Number
1	Method For At-Speed Testing Of Memory Interface Using Scan	US	24 May 2006	11/439,497
2	Method And Apparatus For Storing And Distributing Memory Repair Information	US	11 Sept 2007	11/853,383
3	Testing Each Side Of A Differential Pair	US	September 2008	61/101,219

and

WHEREAS, Mentor Graphics Corporation (hereinafter Assignee), a corporation organized under the laws of the state of Oregon, having a place of business at 8005 SW Boeckman Road, Wilsonville, OR 97070-7777, desires to acquire the entire right, title and interest in and to said Patent Properties and worldwide rights in the inventions described therein.

For good and valuable consideration, receipt of which is acknowledged, Assignor does hereby assign to Assignee the entire right, title and interest in and to each and all of the Patent Properties identified above, including all worldwide rights thereto, rights of priority therein and to file for protection of inventions set forth therein under the Patent Cooperation Treaty and under any other treaty or laws of any country, and in and to any and all letters patent which may be granted therefor, and any divisions, continuing applications, reexaminations, reissues, or

extensions thereof, the same to be held and enjoyed by Assignee, its successors, or assignees, to the full end of the term or terms for which any and all letters patent may be granted, together with all claims against third parties for damages by reason of past infringement of any one or more of said Patent Properties with the right to sue for and collect the same for Assignee's own use and for the use of Assignee's successors, assigns and other legal representatives.

Assignor covenants and agrees in favor of Assignee and its successors that at any time upon the request of Assignee or its successors, Assignor will, at Assignee's expense, communicate to Assignee or its successors all information known to Assignor relating to the Patent Properties, execute and deliver all papers, make all rightful oaths, testify in any legal proceedings and perform all other lawful acts necessary including: (i) to execute papers reasonably required by Assignee to perfect title to the Patent Properties, including divisions and continuations thereof and to any and all letters patent which may be granted therefor or thereon, in any country, including reissues or extensions, in Assignee or its successors; (ii) to assist Assignee or its successors in obtaining, maintaining, confirming or enforcing by reissue or reexamination a grant of a valid United States Patent to Assignee on said Patent Properties; and (iii) to assist Assignee in connection with any interference which may be declared concerning said Patent Properties and any letters patent which may be granted therefor or thereon, or any confirmation, division, continuation, reexamination or reissue thereof; (iv) to execute all papers and documents and perform any act which may be necessary in connection with claims or provisions of the International Convention for Protection of Industrial Property or similar treaties or agreements.

IN WITNESS WHEREOF, the Assignor executes this Assignment effective as of the date below:

ASSIGNOR

Signature

Dean Freed

Print Signatory Name

President

Title

September 10, 2009

Date

Subscribed and Sworn to Before Me this
10th day of September, 2009

OFFICIAL SEAL
DANIELLE M DUGGAN
NOTARY PUBLIC - OREGON
COMMISSION NO. 423911
MY COMMISSION EXPIRES JAN 26, 2012

Notary Public
My Commission Expires January 26, 2012