PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE BY SECURED PARTY

CONVEYING PARTY DATA

Name	Execution Date
Longview Fund, L.P.	02/27/2009
Alpha Capital Anstalt	02/27/2009

RECEIVING PARTY DATA

Name:	Irvine Sensors Corporation
Street Address:	3001 Redhill Ave. Building 4, Suite 108
City:	Costa Mesa
State/Country:	CALIFORNIA
Postal Code:	92626

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	11150712

OP $40.00 11150712

CORRESPONDENCE DATA

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NAME OF SUBMITTER:	Paul S. Hunter

Total Attachments: 46
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RELEASE OF SECURITY INTEREST

This release of security interest is made and executed by Longview Fund, L.P., a Delaware corporation, and Alpha Capital Anstalt, a Liechtenstein company, (together, the "**Secured Parties**"), in favor of Irvine Sensors Corporation, a Delaware corporation ("**Debtor**").

A. The Secured Parties loaned money to Debtor, and Debtor granted the Secured Parties a security interest in all of Debtor's intellectual property assets to secure indebtedness and obligations of Debtor to the Secured Parties.

B. The Secured Parties recorded their security interest as follows:

Debtor	Secured Party	Execution Date	Reel/Frame	Recordation Date
Irvine Sensors Corp.	Longview Fund, L.P. Alpha Capital Anstalt	12/29/2006	018746/0842	1/05/2007

NOW, THEREFORE, for valuable consideration received, by its execution of this Release of Security Interest, the Secured Parties hereby irrevocably and unconditionally release all right, title and interest in all of the following:

(a) the patents and patent applications listed in Exhibit A (the "**Patents**");

(b) all patents and patent applications (i) to which any of the Patents directly or indirectly claims priority, (ii) for which any of the Patents directly or indirectly forms a basis for priority, and/or (iii) that directly or indirectly incorporate by reference, or are directly or indirectly incorporated by reference into, the Patents;

(c) all reissues, reexaminations, extensions, continuations, continuations in part, continuing prosecution applications, requests for continuing examinations, divisions, registrations of any item in any of the foregoing categories (a) and (b);

(d) all non-United States patents, patent applications, and counterparts relating to the Patents or any item in any of the foregoing categories (a) through (c), including, without limitation, certificates of invention, utility models, industrial design protection, design patent protection, other governmental grants or issuances, and any rights to apply in any or all countries of the world for patents, certificates of invention, utility models, industrial design protections, design patent protections, or governmental grants or issuances of any type related to any of the Patents and the inventions, invention disclosures, and discoveries therein;

(e) inventions, invention disclosures, and discoveries described in any of the Patents of any item in the foregoing categories (a) though (d);

(f) all rights to apply in any or all countries of the world for patents, certificates of invention, utility models, industrial design protections, design patent protections, or other governmental grants or issuances of any type related to any item in any of the foregoing categories (a) through (e), including, without limitation, under the Paris Convention for the

Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement, or understanding;

(g) causes of action (whether known or unknown or whether currently pending, filed, or otherwise) and other enforcement rights under, or on account of, any of the Patents and/or the rights described in the above subparagraphs (a) through (f), including, without limitation, all causes of action and other enforcement rights for

(i) damages,
(ii) injunctive relief, and
(iii) any other remedies of any kind

for past, current and future infringement; and

(h) all rights to collect royalties and other payments under or on account of any of the Patents and/or any item in any of the foregoing categories (a) through (g).

If necessary or desired, the Secured Parties hereby authorize Debtor's authorized representative to file UCC Financing Statement Amendment(s) with the applicable filing office(s) in order to memorialize the release of any security interest by the Secured Parties.

This Release is governed by the law of the State of Delaware, excluding its choice of law principles to the contrary. This Release shall be binding upon the Secured Parties and their successors and assigns and inures, to the benefit of, with respect to the Patents (including any purchaser). The Secured Parties acknowledge that they are aware that they may hereafter discover facts different from or in addition to what they now know, believe or suspect to be true with respect to the matters herein released, that such facts may give rise to claims, causes of action, damages, consequences or results that are unforeseen or unsuspected, and that the Secured Parties are nonetheless giving up their rights, and the releases in this Release Agreement will be and remain in effect in all respects as complete, general releases, notwithstanding any such different or additional facts.

IN WITNESS WHEREOF, the undersigned has executed this Release of Security Interest on this 27th day of February 2009.

Longview Fund, L.P.

By: _____

Name: J. Michael Rudolph

Its: CFO - Investment Advisor

Alpha Capital Anstalt

By: _____

Name: _____

Its: _____

Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement, or understanding;

(g) causes of action (whether known or unknown or whether currently pending, filed, or otherwise) and other enforcement rights under, or on account of, any of the Patents and/or the rights described in the above subparagraphs (a) through (f), including, without limitation, all causes of action and other enforcement rights for

(i) damages,
(ii) injunctive relief, and
(iii) any other remedies of any kind

for past, current and future infringement; and

(h) all rights to collect royalties and other payments under or on account of any of the Patents and/or any item in any of the foregoing categories (a) through (g).

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IN WITNESS WHEREOF, the undersigned has executed this Release of Security Interest on this 27th day of February 2009.

Longview Fund, L.P.

By: _____

Name: _____

Its: _____

Alpha Capital Anstalt

By: _____

Name: Konrad Ackerman

Its: Director

Exhibit A

PATENTS TO BE ASSIGNED

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
5,235,672 (07/651,477)	US	8/10/1993 (2/6/1991)	Hardware for electronic neural network Carson, John C.
6,389,404 (09/223,476)	US	5/14/2002 (12/30/1998)	Neural processing module with input architectures that make maximal use of a weighted synapse array Carson, John C.; Saunders, Christ H.
6,650,704 (09/427,384)	US	11/18/2003 (10/25/1999)	Method of producing a high quality, high resolution image from a sequence of low quality, low resolution images that are undersampled and subject to jitter Carlson, Randolph S.; Arnold, Jack L.; Feldmus, Valentine G.
6,829,237 (09/973,857)	US	12/7/2004 (10/9/2001)	High speed multi-stage switching network formed from stacked switching layersCarson, John C.; Ozguz, Volkan H.
7,082,591 (10/346,363)	US	7/25/2006 (1/17/2003)	Method for effectively embedding various integrated circuits within field programmable gate arrays Carlson, Randolph S.
6,856,167 (10/347,038)	US	2/15/2005 (1/17/2003)	Field programmable gate array with a variably wide word width memory Ozguz, Volkan H.; Carlson, Randolph S.; Gann, Keith D.; Leon, John P.
7,265,579 (11/037,490)	US	9/4/2007 (1/18/2005)	Field programmable gate array incorporating dedicated memory stacks Carlson, Randolph Stuart; Ozguz, Volkan; Gann, Keith D.; Leon, John P.
5,508,836 (08/305,066)	US	4/16/1996 (9/13/1994)	Infrared wireless communication between electronic system components DeCaro, Robert; Saunders, Christ H.; Maeding, Dale

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
5,635,705 (08/526,415)	US	6/3/1997 (9/11/1995)	Sensing and selecting observed events for signal processing Saunders, Christ H.
6,195,268 (09/031,435)	US	2/27/2001 (2/26/1998)	Stacking layers containing enclosed IC chips Eide, Floyd K.
5,045,685 (07/534,969)	US	9/3/1991 (6/6/1990)	Analog to digital conversion on multiple channel IC chips Wall, Llewellyn E.
5,104,820 (07/720,025)	US	4/14/1992 (6/24/1991)	Method of fabricating electronic circuitry unit containing stacked IC layers having lead rerouting Go, Tiong C.(deceased,); Minahan, Joseph A.; Shanken, Stuart N.
5,279,991 (07/996,794)	US	1/18/1994 (12/24/1992)	Method for fabricating stacks of IC chips by segmenting a larger stack Minahan, Joseph A.; Pepe, Angel A.
5,432,318 (08/178,923)	US	7/11/1995 (1/7/1994)	Apparatus for segmenting stacked IC chips Minahan, Joseph A.
5,304,790 (07/956,914)	US	4/19/1994 (10/5/1992)	Apparatus and system for controllably varying image resolution to reduce data output Arnold, Jack
5,347,428 (07/985,837)	US	9/13/1994 (12/3/1992)	Module comprising IC memory stack dedicated to and structurally combined with an IC microprocessor chip Carson, John C.; Indin, Ronald J.; Shanken, Stuart N.
5,406,701 (08/120,675)	US	4/18/1995 (9/13/1993)	Fabrication of dense parallel solder bump connections Pepe, Angel A.; Reinker, David M.; Minahan, Joseph A.
5,424,920 (08/232,739)	US	6/13/1995 (4/25/1994)	Non-conductive end layer for integrated stack of IC chips Miyake, Michael K.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
5,432,729 (08/255,465)	US	7/11/1995 (6/8/1994)	Electronic module comprising a stack of IC chips each interacting with an IC chip secured to the stack Carson, John C.; Some, Raphael R.
5,581,498 (08/326,645)	US	12/3/1996 (10/20/1994)	Stack of IC chips in lieu of single IC chip Ludwig, David E.; Saunders, Christ H.; Some, Raphael R.; Stuart, John J.
5,688,721 (08/62,2671)	US	11/18/1997 (3/26/1996)	3D stack of IC chips having leads reached by vias through passivation covering access plane Johnson, Tony K.
5,953,588 (08/777,747)	US	9/14/1999 (12/21/1996)	Stackable layers containing encapsulated IC chips Camien, Andrew N; Yamaguchi, James S.
6,072,234 (09/316,740)	US	6/6/2000 (5/21/1999)	Stack of equal layer neo-chips containing encapsulated IC chips of different sizes Camien, Andrew N.; Yamaguchi, James S.
5,955,668 (09/166,458)	US	9/21/1999 (10/5/1998)	Multi-element micro gyro Hsu, Ying W.; Reeds, III, John W.; Saunders, Christ H.
6,089,089 (09/301,847)	US	7/18/2000 (4/29/1999)	Multi-element micro gyro Hsu, Ying W.
6,578,420 (09/604,782)	US	6/17/2003 (6/26/2000)	Multi-axis micro gyro structure Hsu, Ying Wen
6,014,316 (09/095,416)	US	1/11/2000 (6/10/1998)	IC stack utilizing BGA contacts Eide, Floyd K.
6,028,352 (09/095,415)	US	2/22/2000(6/10/1998)	IC stack utilizing secondary lead frames Eide, Floyd K.
6,117,704 (09/282,704)	US	9/12/2000 (3/31/1999)	Stackable layers containing encapsulated chips Yamaguchi, James S.; Ozguz, Volkan H.; Camien, Andrew N.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
6,476,392 (09/853,819)	US	11/5/2002 (5/11/2001)	Method and apparatus for temperature compensation of an uncooled focal plane array Kaufman, Charles S.; Carson, Randolph S.; Hornback, William B.
6,891,160 (10/281,393)	US	5/10/2005 (10/25/2002)	Method and apparatus for temperature compensation of an uncooled focal plane array Kaufman, Charles S.; Carson, Randolph S.; Hornback, William B.
7,235,785 (11/048,634)	US	6/26/2007 (1/31/2005)	Imaging device with multiple fields of view incorporating memory-based temperature compensation of an uncooled focal plane array Hornback, Bert; Harwood, Doug; Boyd, W. Eric; Carlson, Randy
6,596,997 (09/921,525)	US	7/22/2003 (8/3/2001)	Retro-reflector warm stop for uncooled thermal imaging cameras and method of using the same Kaufman, Charles S.
6,706,971 (10/142,557)	US	3/16/2004 (5/10/2002)	Stackable microcircuit layer formed from a plastic encapsulated microcircuit Albert, Douglas M.; Gann, Keith D.
7,174,627 (10/338,974)	US	2/13/2007 (1/9/2003)	Method of fabricating known good dies from packaged integrated circuits Gann, Keith D.
6,560,109 (09/949,024)	US	5/6/2003 (9/7/2001)	Stack of multilayer modules with heat-focusing metal layer Yamaguchi, James Satsuo; Pepe, Angel Antonio; Ozguz, Volkan H.; Camien, Andrew Nelson
6,717,061 (09/949,512)	US	4/6/2004 (9/7/2001)	Stacking of multilayer modules Yamaguchi, James Satsuo; Pepe, Angel Antonio; Ozguz, Volkan H.; Camien, Andrew Nelson

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
6,734,370 (09/948,950)	US	5/11/2004 (9/7/2001)	Multilayer modules with flexible substrates Yamaguchi, James Satsuo; Pepe, Angel Antonio; Ozguz, Volkan H.; Camien, Andrew Nelson
7,127,807 (10/431,914)	US	10/31/2006 (5/7/2003)	Process of manufacturing multilayer modules Yamaguchi, James Satsuo; Pepe, Angel Antonio; Ozguz, Volkan H.; Camien, Andrew Nelson
6,797,537 (09/938,686)	US	9/28/2004 (10/30/2001)	Method of making stackable layers containing encapsulated integrated circuit chips with one or more overlaying interconnect layers Pepe, Angel Antonio; Yamaguchi, James Satsuo
6,784,547 (10/302,680)	US	8/31/2004 (11/21/2002)	Stackable layers containing encapsulated integrated circuit chips with one or more overlying interconnect layers Pepe, Angel Antonio; Yamaguchi, James Satsuo
7,239,012 (10/951,990)	US	7/3/2007 (9/28/2004)	Three-dimensional module comprised of layers containing IC chips with overlying interconnect layers Pepe, Angel; Yamaguchi, James
6,806,559 (10/128,728)	US	10/19/2004(4/22/2002)	Method and apparatus for connecting vertically stacked integrated circuit chips Gann, Keith D.; Albert, Douglas M.
6,912,862 (10/615,641)	US	7/5/2005 (7/8/2003)	Cryopump piston position tracking Sapir, Itzhak
6,967,411 (10/360,244)	US	11/22/2005 (2/7/2003)	Stackable layers containing ball grid array packages Eide, Floyd K.
7,242,082 (11/229,351)	US	6/10/2007 (9/15/2005)	Stackable layer containing ball grid array package Eide, Floyd

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
6,993,835 (10/726,888)	US	2/7/2006 (12/4/2003)	Method for electrical interconnection of angularly disposed conductive patterns Albert, Douglas Marice
6,998,328 (10/701,783)	US	2/14/2006 (11/5/2003)	Method for creating neo-wafers from singulated integrated circuit die and a device made according to the method Stern, Jonathan Michael
7,417,323 (10/703,177)	US	(11/6/2003)	Neo-wafer device and method Sambo S. He
7,198,965 (11/354,370)	US	4/3/2007 (2/14/2006)	Method for making a neo-layer comprising embedded discrete components He, Sambo
7,180,579 (10/806,037)	US	2/20/2007 (3/22/2004)	Three-dimensional imaging processing module incorporating stacked layers containing microelectronic circuits Ludwig, David E.; Kennedy, John V.; Kleinhans, William; Liu, Tina; Krutzik, Christian
7,436,494 (11/706,724)	US	10/14/2008 (2/15/2007)	Three-dimensional LADAR module with alignment reference insert circuitry Ludwig, David E.; Kennedy, John V.; Kleinhans, William; Liu, Tina; Krutzik, Christian
7,335,576 (11/197,828)	US	2/26/2008 (8/5/2005)	Method for precision integrated circuit die singulation using differential etch rates David, Ludwig; Yamaguchi, James; Clark, Stuart; Boyd, W. Eric
7,380,459 (11/654,292)	US	6/3/2008 (1/16/2007)	Absolute pressure sensor Sapir, Itzhak
10/968,572	US	10/19/2004	Vertically stacked pre-packaged integrated circuit chips Keith Gann; Douglas N. Albert
7,440,449 (10/960,712)	US	10/6/2004	High speed switching module comprised of stacked layers incorporating T-connect structures John C. Carson; Volkan H. Orguz

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
11/977,447	US	10/24/2007	Wire bond method for angularly disposed conductive pads and a device made from the method Randy Wayne Bindrup
11/897,938	US	08/31/2007	Field programmable gate array utilizing dedicated memory stacks in a vertical layer format Ozguz, Volkan; Carlson, Randolph Stuart; Gann, Keith D.; Leon, John P.; Boyd, W Eric
11/825,643	US	7/7/2007	Ball grid array package format layers and structure Keith Gann; W Eric Boyd
11/807,671	US	5/30/2007	Large Format Thermoelectic Infrared Detector and a Method of Fabrication Ying Hsu
11/731,154	US	3/31/2007	Ball Grid Array Stack Frank Mantz
11/524,090	US	9/20/2006	Stackable tier structure comprising high density feedthrough Volkan Ozguz; Jonathan Stern
11/511,117	US	8/26/2006	MEMS cooling device Itzhak Sapir
11/499,403	US	8/4/2006	High density interconnect assembly comprising stacked electronic module John V. Kennedy
11/441,908	US	5/26/2006	Stackable tier structure comprising prefabricated high density feedthrough Volkan Ozguz; Jonathan Stern
11/429,468	US	5/5/2006	Global positioning using planetary constants Sapir Itzhak
11/415,891	US	5/1/2006	Low power electronic circuit incorporating real time clock Gary Gottlieb
11/350,974	US	2/8/2006	Stacked ball grid array package module utilizing one or more interposer layers William E. Boyd; Daniel Michaels

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
11/301,645	US	12/12/2005	Cornerbond assembly comprising three-dimensional electronic modules Albert Douglas
11/259,683	US	10/25/2005	Stacked microelectronic layer and module with three-axis channel T-connects Keith D. Gann; W. Eric Boyd
11/248,659	US	10/11/2005	Anti-tamper module Volkan H. Ozguz; John Leon
10/178,390	US	6/24/2002	Video event capture, storage and processing method and apparatus Randolph S. Carlson
60/993,689	US		Chip scale vacuum pump Itzhak Sapir
11/150,712	US	6/10/2005	Stackable semiconductor chip layer comprising prefabricated trench interconnect vias W. Eric Boyd; Angel Pepe; James Yamaguchi; Volkan Ozguz; Andrew Camien; Douglas Albert
11/062,507	US	2/22/2005	BGA-scale stacks comprised of layers containing integrated circuit die and a method for making the same Gann Keith; William E. Boyd
12/008,253	US	1/8/2008	Microcombustion power system Ying Hsu
61/007,497	US	12/12/2007	Forced vibration piezo generator Itzhak Sapir
SE0570479 (SE92905662.0)	SE	10/10/2001 (1/29/1992)	Hardware for electronic neural network Carson, John C.
NL0570479 (NL92905662.0)	NL	10/10/2001 (1/29/1992)	Hardware for electronic neural network Carson, John C.
JP2005-507894	JP	1/16/2006	Stackable layers containing ball grid array packages Inventorship not available

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
JP2006-286556	JP	10/20/2006	Stackable tier structure comprising high density feedthrough Volkan Ozguz; Jonathan Stern
JP2000-591490	JP	12/30/1999	Neural processing module with input architectures that make maximal use of a weighted synapse array Carson, John C.; Saunders, Christ H.
JP3308265 (JP12-554175)	JP	6/10/1999	IC stack utilizing flexible circuits with BGA contacts Eide, Floyd K.
JP3511008 (JP12-553982)	JP	6/10/1999	IC stack utilizing secondary leadframes Eide, Floyd K.
JP3544974 (JP06-0502691)	JP	5/5/1993	Non-conductive end layer for integrated stack of IC chips Miyake, Michael K.
GB0570479 (GB92905662.0)	GB	10/10/2001 (1/29/1992)	Hardware for electronic neural network Carson, John C.
GB1097467 (GB9992850.2)	GB	11/2/2006 (6/10/1993)	IC stack utilizing secondary leadframes Eide, Floyd K.
GB1596433 (GB04394026.1)	GB	1/2/2008 (5/12/2004)	A method for creating neo-wafers from singulated integrated circuit die and a device made according to the methodStern, Jonathan Michael
GB0596075 (GB93911250.4)	GB	8/22/2001 (5/5/1993)	Non-conductive end layer for integrated stack of IC chips Miyake, Michael K.
GB0683968 (GB94903352.6)	GB	10/24/2002 (12/1/1993)	Module comprising IC memory stack dedicated to and structurally combined with an IC microprocessor chip Carson, John C.; Indin, Ronald J.; Shanken, Stuart N.
GB0695494 (GB94915397.7)	GB	2/24/2001 (4/19/1994)	Electronic module comprising a stack of IC chips Carson, John C.; Some, Raphael R.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
GB0713609 (GB94925876.8)	GB	5/7/2003(8/12/1994)	Stack of IC chips as substitute for single IC chipLudwig, David E.; Saunders, Christ H.; Some, Raphael R.; Stuart, John J.
GB067087 (GB94909418.9)	GB	(12/16/1993)	Fabricating stacks of IC chips by segmenting a larger stack MINIHAN JOSEPH A; PEPE ANGEL A
FR1097467 (FR99928570.2)	FR	11/2/2006 (6/10/1993)	IC stack utilizing secondary leadframes Eide, Floyd K.
FR1596433 (FR04394026.1)	FR	1/2/2008 (5/12/2004)	A method for creating neo-wafers from singulated integrated circuit die and a device made according to the method Stern, Jonathan Michael
FR0596075 (FR93911250.4)	FR	8/22/2001 (5/5/1993)	Non-conductive end layer for integrated stack of IC chips Miyake, Michael K.
FR0683968 (FR94903352.6)	FR	10/24/2002 (12/1/1993)	Module comprising IC memory stack dedicated to and structurally combined with an IC microprocessor chip Carson, John C.; Indin, Ronald J.; Shanken, Stuart N.
FR0695494 (FR94915397.7)	FR	2/24/2001 (4/19/1994)	Electronic module comprising a stack of IC chips Carson, John C.; Some, Raphael R.
FR0713609 (FR94925876.8)	FR	5/7/2003 (8/12/1994)	Stack of IC chips as substitute for single IC chip Ludwig, David E.; Saunders, Christ H.; Some, Raphael R.; Stuart, John J.
EP02705988.0	EP	1/25/2002	A stackable microcircuit layer formed from a plastic encapsulated microcircuit and method of making the same Albert, Douglas M.; Gann, Keith D.
EP06255467.0	EP	10/24/2006	Stackable tier structure comprising high density feedthrough Volkan Ozguz; Jonathan Stern

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
EP99967712.3	EP	12/30/1999	Neural processing module with input architectures that make maximal use of a weighted synapse array Carson, John C.; Saunders, Christ H.
EP99928570.2	EP	6/10/1993	IC stack utilizing flexible circuits with BGA contacts Eide, Floyd K.
EP02805694.3	EP	7/16/2002	Wearable biomonitor with flexible thinned integrated circuit Ogzuz, Volkhan H; Khashayar, Abbas
EP02789292.6	EP	10/25/2002	Stackable layers containing encapsulated integrated circuit chips with one or more overlying interconnect layers and a method of making the same Pepe, Angel Antonio; Yamaguchi, James Satsuo
EP02798173.7	EP	9/9/2002	Stacking of multilayer modules Yamaguchi, James Satsuo; Pepe, Angel Antonio; Ozguz, Volkan H.; Camien, Andrew Nelson
EP95935157.8	EP	9/27/1995	Infrared wireless communication between electronic system components DeCaro, Robert; Saunders, Christ H.; Maeding, Dale
EP03721978.9	EP	4/22/2003	Method and apparatus for connecting vertically stacked integrated circuit chips Gann, Keith D.; Albert, Douglas M.
DE69232116 (DE69232116)	DE	10/10/2001 (1/29/1992)	Hardware for electronic neural network Carson, John C.
DE69330630 (DE69330630)	DE	8/22/2001 (5/5/1993)	Non-conductive end layer for integrated stack of IC chips Miyake, Michael K.
DE69426695 (DE6942669.5)	DE	2/24/2001 (4/19/1994)	Electronic module comprising a stack of IC chips Carson, John C.; Some, Raphael R.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
DE602004011025 (DE602004011025)	DE	1/2/2008 (5/12/2004)	A method for creating neo-wafers from singulated integrated circuit die and a device made according to the method Stern, Jonathan Michael
PCT/US06/039915	WO	8/26/2006	MEMS cooling device Itzhak Sapir
4,814,629 (07/107352)	US	3/21/1989 (10/13/1987)	Pixel displacement by series-parallel analog switching Arnold, Jack L.
11/825,643	US	7/7/2007	Ball grid array package format layers and structure Keith Gann
EP06738029.5	EP	3/10/2006	Method for making a neo-layer comprising embedded discrete components Sambo S. He
JP2000-519921	JP	11/10/1998	Method for thinning semiconductor wafers with circuits and wafers made by the same Inventorship not available
JP2004-72804	JP	3/15/2004	Stackable layer, mini stack, and laminated electronic module Volkan Ozguz
EP06735419.1	EP	2/14/2006	Stacked ball grid array package module utilizing one or more interposer layers William E. Boyd
5,635,010	US	4/14/1995	Dry adhesive joining of layers of electronic devices Angel A. Pepe
6,731,121	US	10/16/2000	Highly configurable capacitive transducer interface circuit Christ Ying Hsu

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
6,513,380	US	6/19/2001	Mems sensor with single central anchor and motion-limiting connection geometry John William Reeds III
6,715,352	US	6/26/2001	Method of designing a flexure system for tuning the modal response of a decoupled micromachined gyroscope and a gyroscoped designed according to the method Michael J. Tracy
6,370,937	US	3/19/2001	Method of canceling quadrature error in an angular rate sensor Ying Wen Hsu
JP2664754	JP	1/4/1998	High density electronic package comprising stacked sub-modules Tiong C. Go
JP2001-533437	JP	10/16/2000	Highly configurable capacitive transducer interface circuit Christ Ying Hsu
EP02744453.8	EP	6/18/2002	Mems sensor with single central anchor and motion-limiting connection geometry John William Reeds III
EP02746710.9	EP	6/18/2002	Method of designing a flexure system for tuning the modal response of a decoupled micromachined gyroscope and a gyroscoped designed according to the method Michael J. Tracy
JP2002-562134	JP	1/25/2002	A stackable microcircuit layer formed from a plastic encapsulated microcircuit and method of making the same

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
12/287,691	US	10/10/2008	Three dimensional LADAR module with alignment reference insert circuitry comprising high density interconnect structure John Kennedy; David Ludwig; Christian Krutzik
EP03818224.2	EP	8/8/2003	Stackable layers containing ball grid array packages Eide, Floyd K.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
5,235,672 (07/651,477)	US	8/10/1993 (2/6/1991)	Hardware for electronic neural network Carson, John C.
6,389,404 (09/223,476)	US	5/14/2002 (12/30/1998)	Neural processing module with input architectures that make maximal use of a weighted synapse array Carson, John C.; Saunders, Christ H.
6,650,704 (09/427,384)	US	11/18/2003 (10/25/1999)	Method of producing a high quality, high resolution image from a sequence of low quality, low resolution images that are undersampled and subject to jitter Carlson, Randolph S.; Arnold, Jack L.; Feldmus, Valentine G.
6,829,237 (09/973,857)	US	12/7/2004 (10/9/2001)	High speed multi-stage switching network formed from stacked switching layersCarson, John C.; Ozguz, Volkan H.
7,082,591 (10/346,363)	US	7/25/2006 (1/17/2003)	Method for effectively embedding various integrated circuits within field programmable gate arrays Carlson, Randolph S.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
6,856,167 (10/347,038)	US	2/15/2005 (1/17/2003)	Field programmable gate array with a variably wide word width memory Ozguz, Volkan H.; Carlson, Randolph S.; Gann, Keith D.; Leon, John P.
7,265,579 (11/037,490)	US	9/4/2007 (1/18/2005)	Field programmable gate array incorporating dedicated memory stacks Carlson, Randolph Stuart; Ozguz, Volkan; Gann, Keith D.; Leon, John P.
5,508,836 (08/305,066)	US	4/16/1996 (9/13/1994)	Infrared wireless communication between electronic system components DeCaro, Robert; Saunders, Christ H.; Maeding, Dale
5,635,705 (08/526,415)	US	6/3/1997 (9/11/1995)	Sensing and selecting observed events for signal processing Saunders, Christ H.
6,195,268 (09/031,435)	US	2/27/2001 (2/26/1998)	Stacking layers containing enclosed IC chips Eide, Floyd K.
5,045,685 (07/534,969)	US	9/3/1991 (6/6/1990)	Analog to digital conversion on multiple channel IC chips Wall, Llewellyn E.
5,104,820 (07/720,025)	US	4/14/1992 (6/24/1991)	Method of fabricating electronic circuitry unit containing stacked IC layers having lead rerouting Go, Tiong C.(deceased,); Minahan, Joseph A.; Shanken, Stuart N.
5,279,991 (07/996,794)	US	1/18/1994 (12/24/1992)	Method for fabricating stacks of IC chips by segmenting a larger stack Minahan, Joseph A.; Pepe, Angel A.
5,432,318 (08/178,923)	US	7/11/1995 (1/7/1994)	Apparatus for segmenting stacked IC chips Minahan, Joseph A.
5,304,790 (07/956,914)	US	4/19/1994 (10/5/1992)	Apparatus and system for controllably varying image resolution to reduce data output Arnold, Jack

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
5,347,428 (07/985,837)	US	9/13/1994 (12/3/1992)	Module comprising IC memory stack dedicated to and structurally combined with an IC microprocessor chip Carson, John C.; Indin, Ronald J.; Shanken, Stuart N.
5,406,701 (08/120,675)	US	4/18/1995 (9/13/1993)	Fabrication of dense parallel solder bump connections Pepe, Angel A.; Reinker, David M.; Minahan, Joseph A.
5,424,920 (08/232,739)	US	6/13/1995 (4/25/1994)	Non-conductive end layer for integrated stack of IC chips Miyake, Michael K.
5,432,729 (08/255,465)	US	7/11/1995 (6/8/1994)	Electronic module comprising a stack of IC chips each interacting with an IC chip secured to the stack Carson, John C.; Some, Raphael R.
5,581,498 (08/326,645)	US	12/3/1996 (10/20/1994)	Stack of IC chips in lieu of single IC chip Ludwig, David E.; Saunders, Christ H.; Some, Raphael R.; Stuart, John J.
5,688,721 (08/62,2671)	US	11/18/1997 (3/26/1996)	3D stack of IC chips having leads reached by vias through passivation covering access plane Johnson, Tony K.
5,953,588 (08/777,747)	US	9/14/1999 (12/21/1996)	Stackable layers containing encapsulated IC chips Camien, Andrew N; Yamaguchi, James S.
6,072,234 (09/316,740)	US	6/6/2000 (5/21/1999)	Stack of equal layer neo-chips containing encapsulated IC chips of different sizes Camien, Andrew N.; Yamaguchi, James S.
5,955,668 (09/166,458)	US	9/21/1999 (10/5/1998)	Multi-element micro gyro Hsu, Ying W.; Reeds, III, John W.; Saunders, Christ H.
6,089,089 (09/301,847)	US	7/18/2000 (4/29/1999)	Multi-element micro gyro Hsu, Ying W.
6,578,420 (09/604,782)	US	6/17/2003 (6/26/2000)	Multi-axis micro gyro structure Hsu, Ying Wen

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
6,014,316 (09/095,416)	US	1/11/2000 (6/10/1998)	IC stack utilizing BGA contacts Eide, Floyd K.
6,028,352 (09/095,415)	US	2/22/2000(6/10/1998)	IC stack utilizing secondary lead frames Eide, Floyd K.
6,117,704 (09/282,704)	US	9/12/2000 (3/31/1999)	Stackable layers containing encapsulated chips Yamaguchi, James S.; Ozguz, Volkan H.; Camien, Andrew N.
6,476,392 (09/853,819)	US	11/5/2002 (5/11/2001)	Method and apparatus for temperature compensation of an uncooled focal plane array Kaufman, Charles S.; Carson, Randolph S.; Hornback, William B.
6,891,160 (10/281,393)	US	5/10/2005 (10/25/2002)	Method and apparatus for temperature compensation of an uncooled focal plane array Kaufman, Charles S.; Carson, Randolph S.; Hornback, William B.
7,235,785 (11/048,634)	US	6/26/2007 (1/31/2005)	Imaging device with multiple fields of view incorporating memory-based temperature compensation of an uncooled focal plane array Hornback, Bert; Harwood, Doug; Boyd, W. Eric; Carlson, Randy
6,596,997 (09/921,525)	US	7/22/2003 (8/3/2001)	Retro-reflector warm stop for uncooled thermal imaging cameras and method of using the same Kaufman, Charles S.
6,706,971 (10/142,557)	US	3/16/2004 (5/10/2002)	Stackable microcircuit layer formed from a plastic encapsulated microcircuit Albert, Douglas M.; Gann, Keith D.
7,174,627 (10/338,974)	US	2/13/2007 (1/9/2003)	Method of fabricating known good dies from packaged integrated circuits Gann, Keith D.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
6,560,109 (09/949,024)	US	5/6/2003 (9/7/2001)	Stack of multilayer modules with heat-focusing metal layer Yamaguchi, James Satsuo; Pepe, Angel Antonio; Ozguz, Volkan H.; Camien, Andrew Nelson
6,717,061 (09/949,512)	US	4/6/2004 (9/7/2001)	Stacking of multilayer modules Yamaguchi, James Satsuo; Pepe, Angel Antonio; Ozguz, Volkan H.; Camien, Andrew Nelson
6,734,370 (09/948,950)	US	5/11/2004 (9/7/2001)	Multilayer modules with flexible substrates Yamaguchi, James Satsuo; Pepe, Angel Antonio; Ozguz, Volkan H.; Camien, Andrew Nelson
7,127,807 (10/431,914)	US	10/31/2006 (5/7/2003)	Process of manufacturing multilayer modules Yamaguchi, James Satsuo; Pepe, Angel Antonio; Ozguz, Volkan H.; Camien, Andrew Nelson
6,797,537 (09/938,686)	US	9/28/2004 (10/30/2001)	Method of making stackable layers containing encapsulated integrated circuit chips with one or more overlaying interconnect layers Pepe, Angel Antonio; Yamaguchi, James Satsuo
6,784,547 (10/302,680)	US	8/31/2004 (11/21/2002)	Stackable layers containing encapsulated integrated circuit chips with one or more overlying interconnect layers Pepe, Angel Antonio; Yamaguchi, James Satsuo
7,239,012 (10/951,990)	US	7/3/2007 (9/28/2004)	Three-dimensional module comprised of layers containing IC chips with overlying interconnect layers Pepe, Angel; Yamaguchi, James
6,806,559 (10/128,728)	US	10/19/2004(4/22/2002)	Method and apparatus for connecting vertically stacked integrated circuit chips Gann, Keith D.; Albert, Douglas M.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
6,912,862 (10/615,641)	US	7/5/2005 (7/8/2003)	Cryopump piston position tracking Sapir, Itzhak
6,967,411 (10/360,244)	US	11/22/2005 (2/7/2003)	Stackable layers containing ball grid array packages Eide, Floyd K.
7,242,082 (11/229,351)	US	6/10/2007 (9/15/2005)	Stackable layer containing ball grid array package Eide, Floyd
6,993,835 (10/726,888)	US	2/7/2006 (12/4/2003)	Method for electrical interconnection of angularly disposed conductive patterns Albert, Douglas Marice
6,998,328 (10/701,783)	US	2/14/2006 (11/5/2003)	Method for creating neo-wafers from singulated integrated circuit die and a device made according to the method Stern, Jonathan Michael
7,417,323 (10/703,177)	US	(11/6/2003)	Neo-wafer device and method Sambo S. He
7,198,965 (11/354,370)	US	4/3/2007 (2/14/2006)	Method for making a neo-layer comprising embedded discrete components He, Sambo
7,180,579 (10/806,037)	US	2/20/2007 (3/22/2004)	Three-dimensional imaging processing module incorporating stacked layers containing microelectronic circuits Ludwig, David E.; Kennedy, John V.; Kleinhans, William; Liu, Tina; Krutzik, Christian
7,436,494 (11/706,724)	US	10/14/2008 (2/15/2007)	Three-dimensional LADAR module with alignment reference insert circuitry Ludwig, David E.; Kennedy, John V.; Kleinhans, William; Liu, Tina; Krutzik, Christian
7,335,576 (11/197,828)	US	2/26/2008 (8/5/2005)	Method for precision integrated circuit die singulation using differential etch rates David, Ludwig; Yamaguchi, James; Clark, Stuart; Boyd, W. Eric
7,380,459 (11/654,292)	US	6/3/2008 (1/16/2007)	Absolute pressure sensor Sapir, Itzhak

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
10/968,572	US	10/19/2004	Vertically stacked pre-packaged integrated circuit chips Keith Gann; Douglas N. Albert
7,440,449 (10/960,712)	US	10/6/2004	High speed switching module comprised of stacked layers incorporating T-connect structures John C. Carson; Volkan H. Orguz
11/977,447	US	10/24/2007	Wire bond method for angularly disposed conductive pads and a device made from the method Randy Wayne Bindrup
11/897,938	US	08/31/2007	Field programmable gate array utilizing dedicated memory stacks in a vertical layer format Ozguz, Volkan; Carlson, Randolph Stuart; Gann, Keith D.; Leon, John P.; Boyd, W Eric
11/825,643	US	7/7/2007	Ball grid array package format layers and structure Keith Gann; W Eric Boyd
11/807,671	US	5/30/2007	Large Format Thermoelectic Infrared Detector and a Method of Fabrication Ying Hsu
11/731,154	US	3/31/2007	Ball Grid Array Stack Frank Mantz
11/524,090	US	9/20/2006	Stackable tier structure comprising high density feedthrough Volkan Ozguz; Jonathan Stern
11/511,117	US	8/26/2006	MEMS cooling device Itzhak Sapir
11/499,403	US	8/4/2006	High density interconnect assembly comprising stacked electronic module John V. Kennedy
11/441,908	US	5/26/2006	Stackable tier structure comprising prefabricated high density feedthrough Volkan Ozguz; Jonathan Stern
11/429,468	US	5/5/2006	Global positioning using planetary constants Sapir Itzhak

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
11/415,891	US	5/1/2006	Low power electronic circuit incorporating real time clock Gary Gottlieb
11/350,974	US	2/8/2006	Stacked ball grid array package module utilizing one or more interposer layers William E. Boyd; Daniel Michaels
11/301,645	US	12/12/2005	Cornerbond assembly comprising three-dimensional electronic modules Albert Douglas
11/259,683	US	10/25/2005	Stacked microelectronic layer and module with three-axis channel T-connects Keith D. Gann; W. Eric Boyd
11/248,659	US	10/11/2005	Anti-tamper module Volkan H. Ozguz; John Leon
10/178,390	US	6/24/2002	Video event capture, storage and processing method and apparatus Randolph S. Carlson
60/993,689	US		Chip scale vacuum pump Itzhak Sapir
11/150,712	US	6/10/2005	Stackable semiconductor chip layer comprising prefabricated trench interconnect vias W. Eric Boyd; Angel Pepe; James Yamaguchi; Volkan Ozguz; Andrew Camien; Douglas Albert
11/062,507	US	2/22/2005	BGA-scale stacks comprised of layers containing integrated circuit die and a method for making the same Gann Keith; William E. Boyd
12/008,253	US	1/8/2008	Microcombustion power system Ying Hsu
61/007,497	US	12/12/2007	Forced vibration piezo generator Itzhak Sapir
SE0570479 (SE92905662.0)	SE	10/10/2001 (1/29/1992)	Hardware for electronic neural network Carson, John C.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
NL0570479 (NL92905662.0)	NL	10/10/2001 (1/29/1992)	Hardware for electronic neural network Carson, John C.
JP2005-507894	JP	1/16/2006	Stackable layers containing ball grid array packages Inventorship not available
JP2006-286556	JP	10/20/2006	Stackable tier structure comprising high density feedthrough Volkan Ozguz; Jonathan Stern
JP2000-591490	JP	12/30/1999	Neural processing module with input architectures that make maximal use of a weighted synapse array Carson, John C.; Saunders, Christ H.
JP3308265 (JP12-554175)	JP	6/10/1999	IC stack utilizing flexible circuits with BGA contacts Eide, Floyd K.
JP3511008 (JP12-553982)	JP	6/10/1999	IC stack utilizing secondary leadframes Eide, Floyd K.
JP3544974 (JP06-0502691)	JP	5/5/1993	Non-conductive end layer for integrated stack of IC chips Miyake, Michael K.
GB0570479 (GB92905662.0)	GB	10/10/2001 (1/29/1992)	Hardware for electronic neural network Carson, John C.
GB1097467 (GB9992850.2)	GB	11/2/2006 (6/10/1993)	IC stack utilizing secondary leadframes Eide, Floyd K.
GB1596433 (GB04394026.1)	GB	1/2/2008 (5/12/2004)	A method for creating neo-wafers from singulated integrated circuit die and a device made according to the methodStern, Jonathan Michael
GB0596075 (GB93911250.4)	GB	8/22/2001 (5/5/1993)	Non-conductive end layer for integrated stack of IC chips Miyake, Michael K.
GB0683968 (GB94903352.6)	GB	10/24/2002 (12/1/1993)	Module comprising IC memory stack dedicated to and structurally combined with an IC microprocessor chip Carson, John C.; Indin, Ronald J.; Shanken, Stuart N.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
GB0695494 (GB94915397.7)	GB	2/24/2001 (4/19/1994)	Electronic module comprising a stack of IC chips Carson, John C.; Some, Raphael R.
GB0713609 (GB94925876.8)	GB	5/7/2003(8/12/1994)	Stack of IC chips as substitute for single IC chipLudwig, David E.; Saunders, Christ H.; Some, Raphael R.; Stuart, John J.
GB067087 (GB94909418.9)	GB	(12/16/1993)	Fabricating stacks of IC chips by segmenting a larger stack MINIHAN JOSEPH A; PEPE ANGEL A
FR1097467 (FR99928570.2)	FR	11/2/2006 (6/10/1993)	IC stack utilizing secondary leadframes Eide, Floyd K.
FR1596433 (FR04394026.1)	FR	1/2/2008 (5/12/2004)	A method for creating neo-wafers from singulated integrated circuit die and a device made according to the method Stern, Jonathan Michael
FR0596075 (FR93911250.4)	FR	8/22/2001 (5/5/1993)	Non-conductive end layer for integrated stack of IC chips Miyake, Michael K.
FR0683968 (FR94903352.6)	FR	10/24/2002 (12/1/1993)	Module comprising IC memory stack dedicated to and structurally combined with an IC microprocessor chip Carson, John C.; Indin, Ronald J.; Shanken, Stuart N.
FR0695494 (FR94915397.7)	FR	2/24/2001 (4/19/1994)	Electronic module comprising a stack of IC chips Carson, John C.; Some, Raphael R.
FR0713609 (FR94925876.8)	FR	5/7/2003 (8/12/1994)	Stack of IC chips as substitute for single IC chip Ludwig, David E.; Saunders, Christ H.; Some, Raphael R.; Stuart, John J.
EP02705988.0	EP	1/25/2002	A stackable microcircuit layer formed from a plastic encapsulated microcircuit and method of making the same Albert, Douglas M.; Gann, Keith D.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
EP06255467.0	EP	10/24/2006	Stackable tier structure comprising high density feedthrough Volkan Ozguz; Jonathan Stern
EP99967712.3	EP	12/30/1999	Neural processing module with input architectures that make maximal use of a weighted synapse array Carson, John C.; Saunders, Christ H.
EP99928570.2	EP	6/10/1993	IC stack utilizing flexible circuits with BGA contacts Eide, Floyd K.
EP02805694.3	EP	7/16/2002	Wearable biomonitor with flexible thinned integrated circuit Ogzuz, Volkhan H; Khashayar, Abbas
EP02789292.6	EP	10/25/2002	Stackable layers containing encapsulated integrated circuit chips with one or more overlying interconnect layers and a method of making the same Pepe, Angel Antonio; Yamaguchi, James Satsuo
EP02798173.7	EP	9/9/2002	Stacking of multilayer modules Yamaguchi, James Satsuo; Pepe, Angel Antonio; Ozguz, Volkan H.; Camien, Andrew Nelson
EP95935157.8	EP	9/27/1995	Infrared wireless communication between electronic system components DeCaro, Robert; Saunders, Christ H.; Maeding, Dale
EP03721978.9	EP	4/22/2003	Method and apparatus for connecting vertically stacked integrated circuit chips Gann, Keith D.; Albert, Douglas M.
DE69232116 (DE69232116)	DE	10/10/2001 (1/29/1992)	Hardware for electronic neural network Carson, John C.
DE69330630 (DE69330630)	DE	8/22/2001 (5/5/1993)	Non-conductive end layer for integrated stack of IC chips Miyake, Michael K.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
DE69426695 (DE6942669.5)	DE	2/24/2001 (4/19/1994)	Electronic module comprising a stack of IC chips Carson, John C.; Some, Raphael R.
DE602004011025 (DE602004011025)	DE	1/2/2008 (5/12/2004)	A method for creating neo-wafers from singulated integrated circuit die and a device made according to the method Stern, Jonathan Michael
PCT/US06/039915	WO	8/26/2006	MEMS cooling device Itzhak Sapir
4,814,629 (07/107352)	US	3/21/1989 (10/13/1987)	Pixel displacement by series-parallel analog switching Arnold, Jack L.
11/825,643	US	7/7/2007	Ball grid array package format layers and structure Keith Gann
EP06738029.5	EP	3/10/2006	Method for making a neo-layer comprising embedded discrete components Sambo S. He
JP2000-519921	JP	11/10/1998	Method for thinning semiconductor wafers with circuits and wafers made by the same Inventorship not available
JP2004-72804	JP	3/15/2004	Stackable layer, mini stack, and laminated electronic module Volkan Ozguz
EP06735419.1	EP	2/14/2006	Stacked ball grid array package module utilizing one or more interposer layers William E. Boyd
5,635,010	US	4/14/1995	Dry adhesive joining of layers of electronic devices Angel A. Pepe
6,731,121	US	10/16/2000	Highly configurable capacitive transducer interface circuit Christ Ying Hsu
6,513,380	US	6/19/2001	Mems sensor with single central anchor and motion-limiting connection geometry John William Reeds III
6,715,352	US	6/26/2001	Method of designing a flexure system for tuning the modal response of a decoupled micromachined gyroscope and a gyroscoped designed according to the method Michael J. Tracy

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
6,370,937	US	3/19/2001	Method of canceling quadrature error in an angular rate sensor Ying Wen Hsu
JP2664754	JP	1/4/1998	High density electronic package comprising stacked sub-modules Tiong C. Go
JP2001-533437	JP	10/16/2000	Highly configurable capacitive transducer interface circuit Christ Ying Hsu
EP02744453.8	EP	6/18/2002	Mems sensor with single central anchor and motion-limiting connection geometry John William Reeds III
EP02746710.9	EP	6/18/2002	Method of designing a flexure system for tuning the modal response of a decoupled micromachined gyroscope and a gyroscoped designed according to the method Michael J. Tracy
JP2002-562134	JP	1/25/2002	A stackable microcircuit layer formed from a plastic encapsulated microcircuit and method of making the same
12/287,691	US	10/10/2008	Three dimensional LADAR module with alignment reference insert circuitry comprising high density interconnect structure John Kennedy; David Ludwig; Christian Krutzik
EP03818224.2	EP	8/8/2003	Stackable layers containing ball grid array packages Eide, Floyd K.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
PCT/US00/029448	WO	10/25/2000	SYSTEM AND METHODS FOR PRODUCING HIGH RESOLUTION IMAGES FROM A VIDEO SEQUENCE OF LOWER RESOLUTION IMAGES CARLSON RANDOLPH S; ARNOLD JACK L; FELDMUS VALENTIN G
PCT/US92/005348	WO	6/24/1992	Fabricating electronic circuitry unit containing stacked IC layers having lead rerouting Go, Tiong C.(deceased,); Minahan, Joseph A.; Shanken, Stuart N.
PCT/US03/004462	WO	5/5/1993	Non-conductive end layer for integrated stack of IC chips Miyake, Michael K.
PCT/US99/013171	WO	6/10/1999	IC stack utilizing flexible circuits with BGA contacts Eide, Floyd K.
PCT/US06/008920	WO	3/10/2006	Method for making a neo-layer comprising embedded discrete components He, Sambo
PCT/US01/031583	WO	10/9/2001	High speed switching module comprised of stacked layers incorporating T-connect structures John C. Carson; Volkan H. Orguz
PCT/US02/002276	WO	1/25/2002	A stackable microcircuit layer formed from a plastic encapsulated microcircuit and method of making the same Albert, Douglas M.; Gann, Keith D.
PCT/US02/006848	WO	3/4/2002	Retro-reflector warm stop for uncooled thermal imaging cameras and method of using the same Kaufman, Charles S.
PCT/US02/022617	WO	7/16/2002	Wearable biomonitor with flexible thinned integrated circuit Ogzuz, Volkhan H; Khashayar, Abbas
PCT/US02/028628	WO	9/9/2002	Stacking of multilayer modules Yamaguchi, James Satsuo; Pepe, Angel Antonio; Ozguz, Volkan H.; Camien, Andrew Nelson

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
PCT/US02/034339	WO	10/25/2002	Stackable layers containing encapsulated integrated circuit chips with one or more overlying interconnect layers and a method of making the same Pepe, Angel Antonio; Yamaguchi, James Satsuo
PCT/US02/19779	WO	6/24/2002	Video event capture, storage and processing method and apparatus Randolph S. Carlson
PCT/US03/009190	WO	9/27/1993	Fabrication of dense parallel solder bump connections Pepe, Angel A.; Reinker, David M.; Minahan, Joseph A.
PCT/US03/013569	WO	4/22/2003	Method and apparatus for connecting vertically stacked integrated circuit chips Gann, Keith D.; Albert, Douglas M.
PCT/US03/024706	WO	08/08/2003	Stackable layers containing ball grid array packages Eide, Floyd K.
PCT/US83/01142	WO	7/25/1983	Multiplexer circuitry for high density analog signals
PCT/US88/003084	WO	9/8/1988	Bonding of aligned conductive bumps on adjacent surfaces Go, Tiong C.
PCT/US92/000780	WO	1/29/1992	Hardware for electronic neural network Carson, John C.
PCT/US92/003705	WO	6/28/1990	Fabricating electronic circuitry unit containing stacked IC layers having lead rerouting Go, Tiong C.(deceased,); Minahan, Joseph A.; Shanken, Stuart N.
PCT/US93/009470	WO	10/5/1993	Apparatus and system for controllably varying image resolution to reduce data output Arnold, Jack
PCT/US93/011601	WO	12/1/1993	Module comprising IC memory stack dedicated to and structurally combined with an IC microprocessor chip Carson, John C.; Indin, Ronald J.; Shanken, Stuart N.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
PCT/US93/012268	WO	12/16/1993	Fabricating stacks of IC chips by segmenting a larger stack MINIHAN JOSEPH A; PEPE ANGEL A
PCT/US94/004322	WO	4/19/1994	Electronic module comprising a stack of IC chips Carson, John C.; Some, Raphael R.
PCT/US94/009186	WO	8/12/1994	Stack of IC chips as substitute for single IC chip Ludwig, David E.; Saunders, Christ H.; Some, Raphael R.; Stuart, John J.
PCT/US95/002851	WO	3/7/1995	3D stack of IC chips having leads reached by vias through passivation covering access plane Johnson, Tony K.
PCT/US95/012378	WO	9/27/1995	Infrared wireless communication between electronic system components DeCaro, Robert; Saunders, Christ H.; Maeding, Dale
PCT/US96/000746	WO	1/22/1996	Stackable modules and multimodular assemblies Carson, John C.; DeCaro, Robert E.; Hsu, Ying; Miyake, Michael K.
PCT/US96/014610	WO	9/11/1996	SENSING AND SELECTING OBSERVED EVENTS FOR SIGNAL PROCESSING SAUNDERS CHRIST H
PCT/US98/021798	WO	10/14/1998	Multi-element micro gyro Hsu, Ying Wen
PCT/US98/023929	WO	11/10/1998	Method for thinning semiconductor wafers with circuits and wafers made by the same Albert, Douglas; Ogzuz Volkhan H
PCT/US99/001734	WO	3/23/1990	Analog to digital conversion incorporated in Z-technology module Wall, Llewellyn E.
PCT/US99/004211	WO	2/25/1999	STACKING LAYERS CONTAINING ENCLOSED IC CHIPS EIDE FLOYD
PCT/US99/031124	WO	12/30/1999	Neural processing module with input architectures that make maximal use of a weighted synapse array Carson, John C.; Saunders, Christ H.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
07/329,003	US	3/27/1989	Analog to digital conversion on multiple channel IC chips Wall, Llewellyn E.
07/377,241	US	7/7/1989	Inventorship not available
07/884,719	US	5/15/1992	Method for fabricating stacks of IC chips by segmenting a larger stack Minahan, Joseph A.; Pepe, Angel A.
07/884660	US	5/15/1992	Non-conductive end layer for integrated stack of IC chips Miyake, Michael K.
07/955461	US	10/2/1992	Fabrication of dense parallel solder bump connections Joseph Minahan
08/052,475	US	4/23/1993	Electronic module comprising a stack of IC chips each interacting with an IC chip secured to the stack faceCarson, John C.; Some, Raphael R.
08/106,909	US	8/13/1993	Inventorship not available
08/213,149	US	3/15/1994	3D stack of IC chips having leads reached by vias through passivation covering access plane Johnson, Tony K.
08/870,812	US	6/6/1997	Multi-element micro gyro Hsu, Ying W.; Reeds, III, John W.; Saunders, Christ H.
08/943,305	US	10/14/1997	Multi-element micro gyro Hsu, Ying W.; Reeds, III, John W.; Saunders, Christ H.
09/190,378	US	11/10/1998	Method for thinning semiconductor wafers with circuits and wafers made by the same Albert, Douglas
09/770,864	US	1/26/2001	Method of making a stackable microcircuit layer from a plastic encapsulated microcircuit Douglas M. Albert; Keith D. Gann
10/197,006	US	7/16/2002	Wearable biomonitor with flexible thinned integrated circuit Ogzuz, Volkhan H; Khashayar, Abbas
10/663,371	US		Stacked microelectronic module with vertical interconnect viasOgzuz, Volkhan H;

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
10/805,849	US	3/22/2004	Three-dimensional imaging device incorporating stacked layers containing microelectronic circuits David E. Ludwig; John V. Kennedy; Christian Krutzik
11/003,429	US	12/6/2004	Wearable biomonitor with flexible thinned integrated circuit Ogzuz, Volkhan H; Khashayar, Abbas
60/036,759	US	1/28/1997	Multi-element micro gyro Hsu, Ying W.; Reeds, III, John W.; Saunders, Christ H.
60/049,025	US	6/9/1997	Stacking layers containing enclosed IC chips Eide, Floyd K.
60/049,026	US	6/9/1997	Stacking layers containing enclosed IC chipsEide, Floyd K.
60/049,582	US	6/13/1997	IC stack utilizing BGA contacts Eide, Floyd K.
60/065,088	US		
60/238,797	US	10/6/2000	High speed data switch with traverse-mated stacks containing superconducting electronics John Carson
60/274,120	US		
60/305,353	US		Biomonitor device Ogzuz, Volkhan H
60/346,494	US	1/9/2002	Low cost miniature computer and methods for making sameGann, Keith
60/348,852	US	1/17/2002	Field programmable gate array structure incorporating high density support circuitry and method for making same Ozguz, Volkan H.;
60/354,442	US	2/7/2002	BGA layer and assembly and method for making same Eide, Floyd K.
60/355,955	US	2/12/2002	Stacked BGA assemblyEide, Floyd K.
60/394,167	US	7/8/2002	Cryopump piston position tracking using an encoder Sapir, Itzhak
60/410,895	US		Wearable biomonitor with flexible thinned integrated circuit Ogzuz, Volkhan H; Khashayar, Abbas

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
60/424,022	US		NEO-wafers and NEO-chips, device and method Sambo S. He
60/424,025	US	11/6/2002	Creating wafers from singulated die Stern, Jonathan Michael
60/462,677	US	3/28/2003	High-speed transmitter and receiver incorporating three-dimensional readout electronic module David E. Ludwig;
60/546,598	US	2/20/2004	BGA-scale stacks comprised of thin small outline packages and method for making the same Gann Keith; William E. Boyd
60/617,356	US	10/8/2004	Anti-tamper module Volkan H. Ozguz; John Leon
60/652,777	US	2/14/2005	Stacked ball grid array package module utilizing one or more interposer layers William E. Boyd; Daniel Michaels
60/678,618	US	5/5/2005	GPS incorporating low power real time clock circuitry Itzhak Sapir
60/684,372	US	5/26/2005	Stackable layers of encapsulated integrated circuit chips interconnected with prefabricated via structures Volkan Ozguz; Jonathan Stern
60/710,717	US	8/24/2005	Surface trenched stackable layers Keith Gann; Douglas N. Albert
60/711,375	US	8/26/2005	High density interconnect scheme for stacked electronic modules John V. Kennedy
60/711,376	US	8/26/2005	MEMS cooling device Itzhak Sapir
60/758,922	US	1/17/2006	Absolute pressure sensor Sapir, Itzhak
60/628,742	US	11/18/2004	Interface optimization of high density interconnects Stewart Clark
60/617,426	US	10/8/2004	Interface optimization of high density interconnects Stewart Clark

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
RE33331 (07/336,017)	US	9/11/1990 (4/10/1989)	Multiplexer circuitry for high density analog signals Inventorship not available
4,490,626 (06/403,004)	US	12/25/1984 (7/29/1982)	Multiplexer circuitry for high density analog signals Carlson, Randolph S.
4,912,545 (07/097,797)	US	3/27/1990 (9/16/1987)	Bonding of aligned conductive bumps on adjacent surfaces Go, Tiong C.
4,983,533 (07/114,415)	US	1/8/1991 (10/28/1987)	High-density electronic modules - process and product Go, Tiong C.
4,290,844 (06/015070)	US	9/22/1981 (2/26/1979)	Focal plane photo-detector mosaic array fabrication Rotolante, Ralph A.; Koehler, Toivo
4,304,624 (05/855242)	US	12/8/1981 (11/28/1977)	Method of fabricating a multi-layer structure for detector array module Carson, John C.; Dahlgren, Paul F.
4,352,715 (06/206993)	US	10/5/1982 (11/17/1980)	Detector array module fabrication Carson, John C.; Dahlgren, Paul F.
4,354,107 (06/206994)	US	10/12/1982 (11/14/1980)	Detector array module-structure and fabrication Carson, John C.; Dahlgren, Paul F.
4,403,238 (06/213933)	US	9/6/1983 (12/8/1980)	Detector array focal plane configuration Clark, Stewart A.
4,449,044 (06/262296)	US	5/15/1984 (5/11/1981)	Focal plane photo-detector mosaic array apparatus Rotolante, Ralph A.; Koehler, Toivo
4,525,921 (06/517221)	US	7/2/1985 (7/25/1983)	High-density electronic processing package-structure and fabrication Carson, John C.; Clark, Stewart A.
4,551,629 (06/572802)	US	11/5/1985 (1/23/1984)	Detector array module-structure and fabrication Carson, John C.; Clark, Stewart A.
4,555,623 (06/558099)	US	11/26/1985 (12/5/1983)	Pre-amplifier in focal plane detector array Bridgewater, Walter F.; De Caro, Robert E.; Larson, Roger; Wall, Llewellyn E.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
4,596,948 (06/661727)	US	6/24/1986 (10/17/1984)	Constant current source for integrated circuits Wall, Llewellyn E.
4,617,160 (06/674096)	US	10/14/1986 (11/23/1984)	Method for fabricating modules comprising uniformly stacked, aligned circuit-carrying layers Belanger, Robert J.; Bisignano, Alan G.
4,646,128 (06/720902)	US	2/24/1987 (4/8/1985)	High-density electronic processing package--structure and fabrication Carson, John C.; Clark, Stewart A.
4,672,737 (06/761889)	US	6/16/1987 (8/2/1985)	Detector array module fabrication process Carson, John C.; Clark, Stewart A.
4,675,532 (06/795988)	US	6/23/1987 (11/6/1985)	Combined staring and scanning photodetector sensing system having both temporal and spatial filter in Carson, John C.
4,704,319 (06/842159)	US	11/3/1987 (3/21/1986)	Apparatus and method for fabricating modules comprising stacked circuit-carrying layers Belanger, Robert J.; Bisignano, Alan G.
4,706,166 (06/856835)	US	11/10/1987 (4/25/1986)	High-density electronic modules--process and product Go, Tiong C.
4,764,846 (07/000562)	US	8/16/1988 (1/5/1987)	High density electronic package comprising stacked sub-modules Go, Tiong C.
4,779,005 (07/048551)	US	10/18/1988 (5/11/1987)	Multiple detector viewing of pixels using parallel time delay and integration circuitry Arnold, Jack L.
4,791,286 (07/042686)	US	12/13/1988 (4/27/1987)	Pre-amplifier in focal plane detector array Wall, Llewellyn E.
4,806,761 (07/023644)	US	2/21/1989 (3/9/1987)	Thermal imager incorporating electronics module having focal plane sensor mosaic Carson, John C.; Clark, Stewart A.
4,912,545 (07/097797)	US	3/27/1990 (9/16/1987)	Bonding of aligned conductive bumps on adjacent surfaces Go, Tiong C.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
5,701,233 (08/376,799)	US	12/23/1997 (1/23/1995)	Stackable modules and multimodular assemblies Carson, John C.; DeCaro, Robert E.; Hsu, Ying; Miyake, Michael K.
5,745,631 (08/592,691)	US	4/28/1998 (1/26/1996)	Self-aligning optical beam system Reinker, David M.
NL0511218 (NL90917886.5)	NL	3/12/1997 (6/28/1990)	Fabricating electronic circuitry unit containing stacked IC layers having lead rerouting Go, Tiong C.(deceased,); Minahan, Joseph A.; Shanken, Stuart N.
JP06-0515293	JP	12/16/1993	Inventorship not available
JP97-0513369	JP	9/27/1995	Infrared wireless communication between electronic system components DeCaro, Robert; Saunders, Christ H.; Maeding, Dale
JP02-0506137	JP	3/23/1990	Inventorship not available
JP04-0505734	JP	1/29/1992	Hardware for electronic neural network Carson, John C.
JP58-502699	JP	7/25/1983	Inventorship not available
PCT/US98/021798	WO	10/14/1998	Multi-element micro gyroHsu, Ying Wen
FR0511218 (FR90917886.5)	FR	3/12/1997 (6/28/1990)	Fabricating electronic circuitry unit containing stacked IC layers having lead rerouting Go, Tiong C.(deceased,); Minahan, Joseph A.; Shanken, Stuart N.
EP0116072 (EP83902618.4)	EP	10/11/1989 (7/25/1983)	Multiplexer circuitry for high density analog signals
EP01979633.3	EP	10/9/2001	High speed multi-stage stacked layer switch John C. Carson; Volkan H. Orguz
EP02797722.2	EP	3/4/2002	Retro-reflector warm stop for uncooled thermal imaging cameras and method of using the same Kaufman, Charles S.
EP0511218 (EP90917886.5)	EP	3/12/1997 (6/28/1990)	Fabricating electronic circuitry unit containing stacked IC layers having lead rerouting Go, Tiong C.(deceased,); Minahan, Joseph A.; Shanken, Stuart N.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
EP0570479 (EP92905662.0)	EP	10/10/2001 (1/29/1992)	Hardware for electronic neural network Carson, John C.
EP067087(EP94909418.9)	EP	(12/16/1993)	Fabricating stacks of IC chips by segmenting a larger stackMINIHAN JOSEPH A; PEPE ANGEL A
EP0683968 (EP94903352.6)	EP	10/24/2002 (12/1/1993)	Module comprising IC memory stack dedicated to and structurally combined with an IC microprocessor chip Carson, John C.; Indin, Ronald J.; Shanken, Stuart N.
EP0695494 (EP94915397.7)	EP	2/24/2001 (4/19/1994)	Electronic module comprising a stack of IC chips Carson, John C.; Some, Raphael R.
EP0713609 (EP94925876.8)	EP	5/7/2003 (8/12/1994)	Stack of IC chips as substitute for single IC chip Ludwig, David E.; Saunders, Christ H.; Some, Raphael R.; Stuart, John J.
EP90906503.9	EP	3/23/1990	Analog to digital conversion in Z-technology module Wall, Llewellyn E.
EP92916059.6	EP	6/24/1992	Fabricating electronic circuitry unit containing stacked IC layers having lead rerouting Go, Tiong C.(deceased,); Minahan, Joseph A.; Shanken, Stuart N.
EP93922760.9	EP	9/27/1993	Fabrication of dense parallel solder bump connections Pepe, Angel A.; Reinker, David M.; Minahan, Joseph A.
EP96902733.3	EP	1/22/1996	Stackable modules and multimodular assemblies Carson, John C.; DeCaro, Robert E.; Hsu, Ying; Miyake, Michael K.
EP98957755.6	EP	11/10/1998	Method for thinning semiconductor wafers with circuits and wafers made by the same Albert, Douglas; Ogzuz Volkhan H
EP98964683.1	EP	10/14/1998	Multi-element micro gyro Hsu, Ying Wen

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
DE0683968 (DE94903352.6)	DE	10/24/2002 (12/1/1993)	Module comprising IC memory stack dedicated to and structurally combined with an IC microprocessor chip Carson, John C.; Indin, Ronald J.; Shanken, Stuart N.
DE69030195 (DE69030195.2)	DE	3/12/1997 (6/28/1990)	Fabricating electronic circuitry unit containing stacked IC layers having lead rerouting Go, Tiong C.(deceased,); Minahan, Joseph A.; Shanken, Stuart N.
FR0116072 (FR83902618.4)	FR	7/25/1983	Multiplexer circuitry for high density analog signals Inventorship not available
DE0116072 (DE83902618.4)	DE	7/25/1983	Multiplexer circuitry for high density analog signals Inventorship not available
GB0116072 (GB83902618.4)	GB	7/25/1983	Multiplexer circuitry for high density analog signals Inventorship not available
NL0116072 (NL83902618.4)	NL	7/25/1983	Multiplexer circuitry for high density analog signals Inventorship not available
SE0116072 (SE83902618.4)	SE	7/25/1983	Multiplexer circuitry for high density analog signals Inventorship not available
EP0596075 (EP93911250.4)	EP	8/22/2001 (5/5/1993)	Non-conductive end layer for integrated stack of IC chipsMiyake, Michael K.
EP1097467 (EP99928570.2)	EP	11/2/2006 (6/10/1993)	IC stack utilizing secondary leadframes Eide, Floyd K.
10/339,023	US	1/9/2003	Method for making stacked integrated circuits (ICs) using prepackaged partsKeith D. Gann
11/644,438	US	12/22/2006	Method for making stacked integrated circuits (ICs) using prepackaged parts Keith D. Gann

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
09/949,203	US	9/7/2001	Method of manufacturing multilayer modules James Satsuo Yamaguchi; Angel Antonio Pepe; Volkan H. Ozguz; Andrew Nelson Camien
EP1596433 (EP04394026.1)	EP	1/2/2008 (5/12/2004)	A method for creating neo-wafers from singulated integrated circuit die and a device made according to the method Stern, Jonathan Michael
TR1596433 (TR04394026.1)	TR	1/2/2008 (5/12/2004)	A method for creating neo-wafers from singulated integrated circuit die and a device made according to the method Stern, Jonathan Michael
IT1596433 (IT04394026.1)	IT	1/2/2008 (5/12/2004)	A method for creating neo-wafers from singulated integrated circuit die and a device made according to the method Stern, Jonathan Michael
IE1596433 (IE04394026.1)	IE	1/2/2008 (5/12/2004)	A method for creating neo-wafers from singulated integrated circuit die and a device made according to the method Stern, Jonathan Michael
EP05111589.7	EP	12/1/2005	BGA-scale stacks comprised of layers containing integrated circuit die and a method for making the same Gann Keith; William E. Boyd
11/302,480	US	12/12/2005	Neo-wafer device comprised of multiple singulated integrated circuit die Stern Jonathan
JP2098125 (JP63-501172)	JP	10/20/1987	High-density electronic modules, process and product Go, Tiong C.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
DE6933329	DE	12/16/1993	Method for fabricating stacks of IC chips by segmenting a larger stack Joseph A. Minahan
IT0676087	IT	12/16/1993	Method for fabricating stacks of IC chips by segmenting a larger stack Joseph A. Minahan
NL0676087	NL	12/16/1993	Method for fabricating stacks of IC chips by segmenting a larger stack Joseph A. Minahan
PCT/US99/023460	WO	10/6/1999	Multi-element micro gyro Ying W. Hsu
EP99951869.9	EP	10/6/1999	Multi-element micro gyro Ying W. Hsu
60/049,580	US	6/13/1997	IC stack utilizing secondary leadframes Floyd K. Eide
PCT/US99/013173	WO	06/10/1999	IC stack utilizing secondary leadframes Floyd K. Eide
DE69933873	DE	6/10/1999	IC stack utilizing secondary leadframes Floyd K. Eide
PCT/US02/006803	WO	3/4/2002	Method and apparatus for temperature compensation of an uncooled focal plane array Randolph S. Carson
EP02721271.1	EP	3/4/2002	Method and apparatus for temperature compensation of an uncooled focal plane array Randolph S. Carson

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
CY1596433	CY	5/12/2004	Method for creating neo-wafers from singulated integrated circuit die and a device made according to the method Jonathan Stern
EE1596433	EE	5/12/2004	Method for creating neo-wafers from singulated integrated circuit die and a device made according to the method Jonathan Stern
GR1596433	GR	5/12/2004	Method for creating neo-wafers from singulated integrated circuit die and a device made according to the method Jonathan Stern
HU1596433	HU	5/12/2004	Method for creating neo-wafers from singulated integrated circuit die and a device made according to the method Jonathan Stern
LU1596433	LU	5/12/2004	Method for creating neo-wafers from singulated integrated circuit die and a device made according to the method Jonathan Stern
11/302,480	US	12/12/2005	Neo-wafer device comprised of multiple singulated integrated circuit die Jonathan Stern
60/785,135	US	3/24/2006	Method for image jitter reduction in a multiplayer LADAR device John Kennedy
60/300,449	US	6/25/2001	Video event capture, storage and processing method and apparatus Randolph S. Carlson
PCT/US06/005754	WO	2/14/2006	Stacked ball grid array package module utilizing one or more interposer layers William E. Boyd

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
PCT/US96/005065	WO	4/11/1996	Dry adhesive joining of layers of electronic devices Angel A. Pepe
PCT/US88/000060	WO	1/4/1998	High density electronic package comprising stacked sub-modules Tiong C. Go
PCT/US00/041207	WO	10/16/2006	Highly configurable capacitive transducer interface circuit Christ Ying Hsu
PCT/US02/019452	WO	6/18/2002	Mems sensor with single central anchor and motion-limiting connection geometry John William Reeds III
PCT/US02/020290	WO	6/26/2002	Method of designing a flexure system for turning the modal response of a decoupled micromachined gyroscope and a gyroscope designed according to the method Michael J. Tracy
PCT/US01/08720	WO	3/19/2001	Method of canceling quadrature error in an angular rate sensor Ying Wen Hsu
06/187,787	US	9/16/1980	Detector array module-structure and fabrication John C. Carson
06/282,459	US	7/13/1981	Detector array module-structure and fabrication John C. Carson
60/159,832	US	10/15/1999	Universal capacitive interface circuit Christ Ying Hsu

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
06/721,040	US	4/8/1985	Thermal imager incorporating electronics module having focal plane sensor mosaic John C. Carson
60/190,271	US	3/17/2000	Method for canceling quadrature error in angular rate sensor Ying Wen Hsu
EP0340241	EP	1/4/1998	High density electronic package comprising stacked sub-modules Tiong C. Go
DE3854814	DE	1/4/1998	High density electronic package comprising stacked sub-modules Tiong C. Go
FR0340241	FR	1/4/1998	High density electronic package comprising stacked sub-modules Tiong C. Go
GB0340241	GB	1/4/1998	High density electronic package comprising stacked sub-modules Tiong C. Go
EP00982671.0	EP	10/16/2000	Highly configurable capacitive transducer interface circuit Christ Ying Hsu
PCT/US87/002746	WO	10/20/1987	High-density electronic modules, process and product Tiong C. Go
EP0385979	EP	10/20/1987	High-density electronic modules, process and product Tiong C. Go
DE0385979	DE	10/20/1987	High-density electronic modules, process and product Tiong C. Go

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
FR0385979	FR	10/20/1987	High-density electronic modules, process and product Tiong C. Go
60/809,466	US	5/30/2006	Large format thermoelectric infrared detector and a method of fabrication Ying Hsu
GB0385979	GB	10/20/1987	High-density electronic modules, process and product Tiong C. Go