PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	SECURITY AGREEMENT

CONVEYING PARTY DATA

Name	Execution Date
Spansion LLC	05/10/2010
Spansion Inc.	05/10/2010
Spansion Technology Inc.	05/10/2010
Spansion Technology LLC	05/10/2010

RECEIVING PARTY DATA

Name:	Barclays Bank plc
Street Address:	745 Seventh Avenue
City:	New York
State/Country:	NEW YORK
Postal Code:	10019

PROPERTY NUMBERS Total: 1907

Property Type	Number
Application Number:	10817131
Application Number:	10975629
Application Number:	11000685
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Application Number:	11103960

Application Number:	11065307
Application Number:	11065306
Application Number:	10758148
Application Number:	10475997
Application Number:	11479373

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NAME OF SUBMITTER:	Adam Kummins

Total Attachments: 166
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PATENT SECURITY AGREEMENT

This Patent Security Agreement, dated as of May 10, 2010 (as amended, restated or otherwise modified from time to time, the "Patent Security Agreement"), between each of SPANSION INC., a Delaware corporation, SPANSION LLC, a Delaware limited liability company, SPANSION TECHNOLOGY LLC, a Delaware limited liability company, and certain of their subsidiaries party hereto from time to time (collectively, the "Grantors"), and BARCLAYS BANK PLC, in its capacity as administrative agent and collateral agent for the Secured Parties (together with any successors and assigns thereto in such capacity, the "Administrative Agent").

WITNESSETH:

WHEREAS, Grantors, Spansion International, Inc. and Cerium Laboratories LLC are party to a Pledge and Security Agreement dated as of May 10, 2010 (the "Pledge and Security Agreement") between each of the Grantors and the other grantors thereto and the Administrative Agent pursuant to which the Grantors are required to execute and deliver this Patent Security Agreement; and

NOW, THEREFORE, in consideration of the premises and to induce the Secured Parties to enter into the Loan Documents, the Grantors hereby agree with the Administrative Agent, as follows:

SECTION 1. Defined Terms. Unless otherwise defined herein, terms defined in the Pledge and Security Agreement and used herein have the meaning given to them in the Pledge and Security Agreement.

SECTION 2. Grant of Security Interest in Patent Collateral. Each Grantor hereby pledges and grants to Administrative Agent, for the benefit of the Secured Parties, a security interest in all of such Grantor's right, title and interest in, to and under the following, whether presently existing or hereafter created or acquired (collectively, the "Patent Collateral"):

(a) all United States and foreign patents and certificates of invention, or similar industrial property rights, and applications for any of the foregoing (collectively, "Patents"), including, but not limited to: (i) each patent and patent application referred to on Schedule I hereto (as such schedule may be amended or supplemented from time to time), (ii) all reissues, divisions, continuations, continuations-in-part, extensions, renewals, and reexaminations thereof, (iii) all rights corresponding thereto throughout the world, (iv) all inventions and improvements described therein, (v) all rights to sue for past, present and future infringements thereof, (vi) all licenses, claims, damages, and proceeds of suit arising therefrom, and (vii) all Proceeds of the foregoing, including, without limitation, licenses, royalties, income, payments, claims, damages, and proceeds of suit; and

(b) any and all agreements providing for the granting of any right in or to Patents (whether such Grantor is licensee or licensor thereunder) including those referred to on Schedule I hereto (collectively, "Patent Licenses").

SECTION 3. Security Agreement. The security interest granted pursuant to this Patent Security Agreement is granted in conjunction with the security interest granted to the Administrative Agent for the Secured Parties pursuant to the Pledge and Security Agreement and Grantors hereby acknowledge and affirm that the rights and remedies of the Administrative Agent with respect to the security interest in the Patent Collateral made and granted hereby are more fully set forth in the Pledge and Security Agreement, the terms and provisions of which are incorporated by reference herein as if fully set forth herein. In the event that any provision of this Patent Security Agreement is deemed to conflict with the Pledge and Security Agreement, the provisions of the Pledge and Security Agreement shall control.

SECTION 4. Applicable Law. THIS PATENT SECURITY AGREEMENT AND THE RIGHTS AND OBLIGATIONS OF THE PARTIES HEREUNDER SHALL BE GOVERNED BY, AND SHALL BE CONSTRUED AND ENFORCED IN ACCORDANCE WITH, THE LAWS OF THE STATE OF NEW YORK, WITHOUT REGARD TO ITS CONFLICTS OF LAW PROVISIONS (OTHER THAN SECTION 5-1401 OF THE NEW YORK GENERAL OBLIGATION LAWS). THE PROVISIONS OF THE LEASE AGREEMENT UNDER THE HEADINGS "MISCELLANEOUS" AND "WAIVER OF JURY TRIAL" ARE INCORPORATED HEREIN BY THIS REFERENCE AND SUCH INCORPORATION SHALL SURVIVE ANY TERMINATION OF THE PODS FINANCING AGREEMENTS.

SECTION 5. Counterparts. This Patent Security Agreement may be executed originally or by facsimile or other means of electronic transmission and in any number of counterparts, each of which when so executed and delivered shall be deemed an original, but all such counterparts together shall constitute but one and the same instrument.

[Remainder of page intentionally left blank]

IN WITNESS WHEREOF, each Grantor has caused this Patent Security Agreement to be executed and delivered by its duly authorized officer as of the date first set forth above.

SPANSION LLC,
as Grantor

By:_____
Name: John H. Kispert
Title: President and Chief Executive Officer

SPANSION INC.,
as Grantor

By:_____
Name: John H. Kispert
Title: President and Chief Executive Officer

SPANSION TECHNOLOGY LLC,
as Grantor

By:_____
Name: John H. Kispert
Title: Chief Executive Officer

Accepted and Agreed:

BARCLAYS BANK PLC,
as Collateral Agent

By: _____
Name: Ritam Bhalla
Title: Vice President

Schedule I

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
INSITU SURFACE TREATMENT FOR MEMORY CELL FORMATION	Spansion LLC	10/817,131 4/2/2004	20050227382
SYSTEM AND METHOD FOR IMPROVED MEMORY PERFORMANCE IN A MOBILE DEVICE	Spansion LLC	10/975,629 10/28/2004	20060095622
POLYMERBASED TRANSISTOR DEVICES, METHODS, AND SYSTEMS	Spansion LLC	11/000,685 12/1/2004	20060113524
MEMORY DEVICE HAVING TRAPEZOIDAL BITLINES AND METHOD OF FABRICATING SAME	Spansion LLC	11/033,588 1/12/2005	20060151821
MEMORY DEVICE WITH IMPROVED SWITCHING SPEED AND DATA RETENTION	Spansion LLC	11/078873 3/11/05	20060202192
MEMORY DEVICE WITH IMPROVED DATA RETENTION	Spansion LLC	11/089708 3/25/05	20060214304
METHOD OF PROVIDING AN ERASE ACTIVATION ENERGY OF A MEMEORY DEVICE	Spansion LLC	11/095849 3/31/05	20060221713
MULTICHIP MODULE HAVING A SUPPORT STRUCTURE AND METHOD OF MANUFACTURE	Spansion LLC	11/125396 5/4/05	20060249826
METHOD OF FABRICATING SEMICONDUCTOR DEVICE AND SEMICONDUCTOR DEVICE	Spansion LLC	11/133966 5/20/05	20050263871
JUNCTION LEAKAGE SUPPRESSION IN MEMORY DEVICES	Spansion LLC	11/133,966 5/20/2005	20050263871
READ MODE FOR FLASH MEMORY	Spansion LLC	11/189,923 7/27/2005	20070026675
SYSTEM AND METHOD FOR IMPROVING MESA WIDTH IN A SEMICONDUCTOR DEVICE	Spansion LLC & Advanced Micro Devices, Inc.	11/193409 8/1/05	20070026675
METHOD FOR FORMING NARROW STRUCTURES IN A SEMICONDUCTOR DEVICE	Spansion LLC & Advanced Micro Devices, Inc.	11/235,214 9/27/2005	20070072437

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
CONTACT SPACER FORMATION USING ATOMIC LAYER DEPOSITION	Spansion LLC & Globalfoundries Inc.	11/240,468 10/3/2005	20070077754
DIGITAL DATA TRANSFER BETWEEN DIFFERENT CLOCK DOMAINS	Spansion LLC	11/242215 10/3/05	20070076830
TRIPLE LAYER ANTIREFLECTIVE HARD MASK	Spansion LLC & Globalfoundries Inc.	11/256,184 10/24/2005	20070093070
NONVOLATILE MEMORY DEVICE	Spansion LLC	11/259874 10/26/05	20060101301
SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THEREOF	Spansion LLC	11/261176 10/28/05	20060091445
MEMORY CELL SYSTEM USING SILICONRICH NITRIDE	Spansion LLC & Advanced Micro Devices, Inc.	11/277008 3/20/06	20070215932
WATER FILTRATION SYSTEM	Spansion LLC & General Electric Company	11/290021 11/30/05	20070119773
SEMICONDUCTOR MEMORY AND METHOD OF FABRICATING THE SAME	Spansion LLC	11/291342 11/30/05	20060091422
FABRICATION METHOD FOR A SEMICONDUCTOR DEVICE	Spansion LLC	11/317083 12/21/05	20060276032
NONVOLATILE SONOSTYPE MEMORY DEVICE	Spansion LLC	11/319999 12/27/05	20060231883
SEMICONDUCTOR MEMORY DEVICE HAVING LOWERED BIT LINE RESISTANCE	Spansion LLC	11/338956 1/24/06	20060244037
STACKED TYPE SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING STACKED TYPE SEMICONDUCTOR DEVICE	Spansion LLC	11/339352 1/25/06	20060170090
SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME	Spansion LLC	11/341,932 1/26/2006	20060244019
SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR	Spansion LLC	11/361,630 2/24/2006	20060263989

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR	Spansion LLC	11/363792 2/28/06	20060281242
VERTICAL SEMICONDUCTOR DEVICE	Spansion LLC	11/378463 3/16/06	20070215940
SEMICONDUCTOR DEVICE WITH RECONFIGURABLE LOGIC	Spansion LLC	11/394515 3/31/06	20060237773
MEMORY CELL ARRAY WITH LOW RESISTANCE COMMON SOURCE AND HIGH CURRENT DRIVABILITY	Spansion LLC	11/412574 4/27/06	20070252219
SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD THEREFOR	Spansion LLC	11/414081 4/27/06	20070052064
SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR	Spansion LLC	11/414646 4/27/06	20070052017
METHOD AND APPARATUS FOR DRAIN PUMP POWER CONSERVATION	Spansion LLC	11/423649 6/12/06	20070284609
SEMICONDUCTOR DEVICE AND METHOD FOR FABRICATING THE SAME	Spansion LLC	11/441771 5/26/06	20060278918
SEMICONDUCTOR DEVICE HAVING LAMINATED ELECTRONIC CONDUCTOR ON BIT LINE	Spansion LLC	11/444216 5/30/06	20060278936
SEMICONDUCTOR DEVICE AND PROGRAM DATA REDUNDANCY METHOD THEREFOR	Spansion LLC	11/469,755 8/2/2006	20080121981
INTEGRATED CIRCUIT MEMORY SYSTEM EMPLOYING SILICON RICH LAYERS	Spansion LLC & Advanced Micro Devices, Inc.	11/461131 7/31/06	20080023751
MEMORY CELL SYSTEM WITH MULTIPLE NITRIDE LAYERS	Spansion LLC & Globalfoundries Inc.	11/461428 7/31/06	20080023750
MEMORY CELL SYSTEM WITH NITRIDE CHARGE ISOLATION	Spansion LLC & Advanced Micro Devices, Inc.	11/461998 8/2/06	20080032464
MEMORY SYSTEM WITH PROTECTION LAYER TO COVER THE MEMORY GATE STACK AND METHODS FOR FORMING SAME	Spansion LLC	11/469164 8/31/06	20080121981

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
MULTIPLE COMMUNICATION CHANNELS ON MMC OR SD CMD LINE	Spansion LLC & Inside Contactless	11/469755 9/1/06	20080059668
SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR	Spansion LLC	11/478537 6/28/06	20060291262
SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME	Spansion LLC	11/479379 6/30/06	20070001311
SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD	Spansion LLC	11/480207 6/29/06	20070015366
VOLTAGE BOOSTING DEVICE AND METHOD FOR SEMICONDUCTOR DEVICE	Spansion LLC	11/493467 7/25/06	20070085597
FABRICATION AND METHOD OF OPERATION OF MULTILEVEL MEMORY CELL ON SOI SUBSTRATE	Spansion LLC	11/493468 7/25/06	20070018233
SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR	Spansion LLC	11/495116 7/27/06	20070026604
STORAGE DEVICE, CONTROL METHOD OF STORAGE DEVICE, AND CONTROL METHOD OF STORAGE CONTROL DEVICE	Spansion LLC	11/510061 8/25/06	20070047373
STORAGE DEVICE AND CONTROL METHOD OF STORAGE DEVICE	Spansion LLC	11/510077 8/25/06	20070047342
FLASH MEMORY CELL STRUCTURE UTILIZING LAYERS HAVING DIFFERING SILICON CONCENTRATIONS	Spansion LLC & Globalfoundries Inc.	11/529166 9/28/06	20080079061
STORAGE DEVICE AND CONTROL METHOD THEREOF	Spansion LLC	11/529790 9/29/06	20070076492
SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR	Spansion LLC	11/529805 9/29/06	20070077726
DUAL STORAGE NODE MEMORY DEVICES AND METHODS FOR FABRICATING THE SAME	Spansion LLC	11/530,145 8/25/2006	20070047342

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MEMORY CELL SYSTEM WITH CHARGE TRAP	Spansion LLC & Advanced Micro Devices, Inc.	11/539984 10/10/06	20080083946
SEMICONDUCTOR DEVICE, FABRICATION METHOD THEREFOR, AND FILM FABRICATION METHOD	Spansion LLC	11/540034 9/28/06	20070105304
USING THIN UNDOPED TEOS WITH BPTEOS ILD OR BPTEOS ILD ALONE TO IMPROVE CHARGE LOSS AND CONTACT RESISTANCE IN MULTIBIT MEMORY DEVICES	Spansion LLC	11/546,688 10/12/2006	20070029604
BURIED WORD LINE MEMORY INTEGRATED CIRCUIT SYSTEM	Spansion LLC	11/045,694 10/17/2006	20070091684
PLANARIZATION METHOD USING HYBRID OXIDE AND POLYSILICON CMP	Spansion LLC & Globalfoundries Inc.	11/551,390 10/20/2006	20080096388
CONTACTS FOR SEMICONDUCTOR DEVICES	Spansion LLC & Advanced Micro Devices, Inc.	11/551,532 10/20/2006	20080096348
METHOD FOR MANUFACTURING A MEMORY DEVICE WITH ISOLATED MEMORY CELL CHARGE TRAPPING STRUCTURE	Spansion LLC & Globalfoundries Inc.	11/551535 10/20/06	20080096357
PCHANNEL NAND IN ISOLATED NWELL	Spansion LLC	11/567257 12/6/06	20080135918
CONFORMAL LINER FOR GAPFILLING	Spansion LLC & Globalfoundries Inc.	11/582442 10/18/06	20080096364
MEMORY DEVICE PROTECTION LAYER	Spansion LLC	11/608,032 12/7/2006	20080135913
CU ANNEALING FOR IMPROVED DATA RETENTION IN FLASH MEMORY DEVICES	Spansion LLC	11/593086 11/6/06	20080108193
PREVENTION OF OXIDATION OF CARRIER IONS TO IMPROVE MEMORY RETENTION PROPERTIES OF POLYMER MEMORY CELL	Spansion LLC	11/608388 12/8/06	20080135834

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INTEGRATED CIRCUIT SYSTEM WITH METAL AND SEMICONDUCTING GATE	Spansion LLC & Advanced Micro Devices, Inc.	11/611856 12/16/06	20080142873
STRAPPING CONTACT FOR CHARGE PROTECTION	Spansion LLC	11/612265 12/18/06	20080142889
DUALBIT MEMORY DEVICE HAVING TRENCH ISOLATION MATERIAL DISPOSED NEAR BIT LINE CONTACT AREAS	Spansion LLC	11/612413 12/18/06	20080144366
ERASING FLASH MEMORY USING ADAPTIVE DRAIN AND/OR GATE BIAS	Spansion LLC	11/612863 12/19/06	20080144396
PORTABLE DIGITAL RIGHTS MANAGEMENT (DRM)	Spansion LLC	11/612874 12/19/06	20080148414
METHOD AND APPARATUS FOR MULTICHIP PACKAGING	Spansion LLC	11/612992 12/19/06	20080142942
SEMICONDUCTOR MEMORY COMPRISING DUAL CHARGE STORAGE NODES AND METHODS FOR ITS FABRICATION	Spansion LLC	11/613513 12/20/06	20080149999
NEAR FIELD COMMUNICATION, SECURITY AND NONVOLATILE MEMORY INTEGRATED SUBSYSTEM FOR EMBEDDED PORTABLE APPLICATIONS	Spansion LLC	11/613620 12/20/06	20080155257
SECURE DATA VERIFICATION VIA BIOMETRIC INPUT	Spansion LLC	11/613627 12/20/06	20080155268
MULTIPLE STAKEHOLDER SECURE MEMORY PARTITIONING AND ACCESS CONTROL	Spansion LLC	11/613691 12/20/06	20080109662
METHODS FOR FABRICATING A SPLIT CHARGE STORAGE NODE SEMICONDUCTOR MEMORY	Spansion LLC	11/614048 12/20/06	20080153222
METHOD AND APPARATUS FOR PROTECTION AGAINST PROCESSINDUCED CHARGING	Spansion LLC & Advanced Micro Devices, Inc.	11/614053 12/20/06	20080151590
NONVOLATILE MEMORY SUBSYSTEM INTEGRATED WITH SECURITY FOR STORING NEAR FIELD TRANSACTIONS	Spansion LLC	11/614257 12/21/06	20080155258

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SOLIDSTATE MEMORYBASED GENERATION AND HANDLING OF SECURITY AUTHENTICATION TOKENS	Spansion LLC	11/614306 12/21/06	20080155271
SECURE COPROCESSING MEMORY CONTROLLER INTEGRATED INTO AN EMBEDDED MEMORY SUBSYSTEM	Spansion LLC	11/614309 12/21/06	20080109903
FLOATING GATE PROCESS METHODOLOGY	Spansion LLC	11/614767 12/21/06	20080153183
COPPER PROCESS METHODOLOGY	Spansion LLC	11/614770 12/21/06	20080153185
ZERO INTERFACE POLYSILICON TO POLYSILICON GATE FOR FLASH MEMORY	Spansion LLC & Globalfoundries Inc.	11/614801 12/21/06	20080149986
MEMORY SYSTEM WITH FIN FET TECHNOLOGY	Spansion LLC	11/614,815 12/21/2006	20080150029
MEMORY SYSTEM WITH SELECT GATE ERASE	Spansion LLC	11/614,839 12/21/2006	20080150000
METHOD OF FORMING SPACEDAPART CHARGE TRAPPING STACKS	Spansion LLC	11/615365 12/22/06	20080149988
FLASH MEMORY DEVICES AND METHODS FOR FABRICATING THE SAME	Spansion LLC	11/615489 12/22/06	20080149989
SYSTEMS AND METHODS FOR DISTINGUISHING BETWEEN ACTUAL DATA AND ERASED/BLANK MEMORY WITH REGARD TO ENCRYPTED DATA	Spansion LLC	11/615492 12/22/06	20080155275
INTEGRATED CIRCUIT WAFER SYSTEM WITH CONTROL STRATEGY	Spansion LLC	11/615,583 12/22/2006	20080153180
MEMORY DEVICE ETCH METHODS	Spansion LLC & Advanced Micro Devices, Inc.	11/616085 12/26/06	20080153298
PERSONAL DIGITAL RIGHTS MANAGEMENT AGENTSERVER	Spansion LLC	11/616385 12/27/06	20080162353

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LOCAL INTERCONNECT HAVING INCREASED MISALIGNMENT TOLERANCE	Spansion LLC	11/616,544 12/27/2006	20080157160
METHOD FOR IMPROVED PLANARIZATION IN SEMICONDUCTOR DEVICES	Spansion LLC & Advanced Micro Devices, Inc.	11/616563 12/27/06	20080160764
DUALBIT MEMORY DEVICE HAVING ISOLATION MATERIAL DISPOSED UNDERNEATH A BIT LINE SHARED BY ADJACENT DUALBIT MEMORY CELLS	Spansion LLC	11/616718 12/27/06	20080157263
SYSTEMS AND METHODS FOR ACCESS VIOLATION MANAGEMENT OF SECURED MEMORY	Spansion LLC	11/618075 12/29/06	20080162784
FULLY ASSOCIATIVE BANKING FOR MEMORY	Spansion LLC	11/625150 1/19/07	20080177930
BYTE MASK COMMAND FOR MEMORIES	Spansion LLC	11/625158 1/19/07	20080177931
METHODS OF PROGRAMMING AND ERASING RESISTIVE MEMORY DEVICES	Spansion LLC	11/633800 12/5/06	20080130381
GETTERING/STOP LAYER FOR PREVENTION OF REDUCTION OF INSULATING OXIDE IN METALINSULATORMETAL DEVICE	Spansion LLC	11/633844 12/5/06	20080130195
DAMASCENE METALINSULATORMETAL (MIM) DEVICE	Spansion LLC & Globalfoundries Inc.	11/633,929 12/5/2006	20080132068
METHOD OF PROGRAMMING MEMORY DEVICE	Spansion LLC	11/633845 12/5/06	20080130357
METHOD OF PROGRAMMING, ERASING AND REPAIRING A MEMORY DEVICE	Spansion LLC	11/633940 12/5/06	20080133818
METHOD OF ERASING A RESISTIVE MEMORY DEVICE	Spansion LLC	11/633941 12/5/06	20080130392
METHOD TO PROVIDE A HIGHER REFERENCE VOLTAGE AT A LOWER POWER SUPPLY IN FLASH MEMORY DEVICES	Spansion LLC	11/634776 12/6/06	20080136381

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BARRIER REGION UNDERLYING SOURCE/DRAIN REGIONS FOR DUALBIT MEMORY DEVICES	Spansion LLC	11/634777 12/6/06	20080135902
SEMICONDUCTOR MANUFACTURING APPARATUS AND CONTROL SYSTEM AND CONTROL METHOD THEREFOR	Spansion LLC	11/636064 12/6/06	20070142957
MEMORY CELLS HAVING SPLIT CHARGE STORAGE NODES AND METHODS FOR FABRICATING MEMORY CELLS HAVING SPLIT CHARGE STORAGE NODES	Spansion LLC	11/639666 12/15/06	20080142875
METHODS AND SYSTEMS FOR MEMORY DEVICES	Spansion LLC	11/639935 12/15/06	20080144391
STRESS MANAGEMENT IN BGA PACKAGING	Spansion LLC	11/641506 12/19/06	20080142956
RESISTIVE MEMORY ARRAY USING PIN DIODE SELECT DEVICE AND METHODS OF FABRICATION THEREOF	Spansion LLC	11/641646 12/19/06	20080144354
METHOD OF DEPOSITING COPPER USING PHYSICAL VAPOR DEPOSITION	Spansion LLC & Globalfoundries Inc.	11/641647 12/19/06	20080146028
THIN OXIDE DUMMY TILING AS CHARGE PROTECTION	Spansion LLC	11/645475 12/26/06	20080153269
DEEP BITLINE IMPLANT TO AVOID PROGRAM DISTURB	Spansion LLC	11/646157 12/26/06	20080153274
STRUCTURE AND METHOD FOR WIRE BOND INTEGRITY CHECK ON BGA SUBSTRATES USING INDIRECT ELECTRICAL INTERCONNECTIVITY PATHWAY BETWEEN WIRE BONDS AND GROUND	Spansion LLC	11/650907 1/8/07	20090001573
SELFALIGNED PATTERNING METHOD BY USING NONCONFORMAL FILM AND ETCH BACK FOR FLASH MEMORY AND OTHER SEMICONDUCTOR APPLICATIONS	Spansion LLC	11/653649 1/12/07	20080171416

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SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME	Spansion LLC	11/654704 1/17/07	20080169544
SEMICONDUCTOR MEMORY DEVICE	Spansion LLC & Fujitsu Limited	11/656437 1/23/07	20070114617
DIVISIONBASED SENSING AND PARTITIONING OF ELECTRONIC MEMORY	Spansion LLC	11/687436 3/16/07	20080225607
MEMORY STORAGE VIA AN INTERNAL COMPRESSION ALGORITHM	Spansion, LLC	11/687479 3/16/07	20080228998
STATE CHANGE SENSING	Spansion, LLC	11/687487 3/16/07	20080229122
HIGH ACCURACY ADAPTIVE PROGRAMMING	Spansion, LLC	11/687492 3/16/07	20080225596
MEMORY SYSTEM WITH DEPLETION GATE	Spansion, LLC	11/694,089 3/30/2007	20080150005
DUAL STORAGE NODE MEMORY	Spansion LLC	11/702845 2/5/07	20070205454
FLASH MEMORY CELLS HAVING TRENCHED STORAGE ELEMENTS	Spansion LLC	11/702846 2/5/07	20070205455
DUAL CHARGE STORAGE NODE WITH UNDERCUT GATE OXIDE FOR DEEP SUBMICRON MEMORY CELL	Spansion LLC & Globalfoundries Inc.	11/702847 2/5/07	20080061359
SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME	Spansion LLC	11/712299 2/27/07	20070210373
DIELECTRIC EXTENSION TO MITIGATE SHORT CHANNEL EFFECTS	Spansion LLC & Globalfoundries Inc.	11/724725 3/16/07	20080157199
RESISTANCE CHANGING MEMORY CELL ARCHITECTURE	Spansion LLC	11/724773 3/16/07	20080158935
USING THICK SPACER FOR BITLINE IMPLANT THEN REMOVE	Spansion LLC	11/724775 3/16/07	20080153223
NONVOLATILE RESISTANCE CHANGING FOR ADVANCED MEMORY APPLICATIONS	Spansion LLC	11/724788 3/16/07	20080175035

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METHOD TO OBTAIN MULTIPLE GATE THICKNESSES USING INSITU GATE ETCH MASK APPROACH	Spansion LLC	11/741998 4/30/07	20080268630
TRIPLE POLYSI REPLACEMENT SCHEME FOR MEMORY DEVICES	Spansion LLC	11/742003 4/30/07	20080268650
ADAPTIVE DETECTION OF THRESHOLD LEVELS IN MEMORY	Spansion LLC	11/742371 4/30/07	20080266945
SELF ALIGNED NARROW STORAGE ELEMENTS FOR ADVANCED MEMORY DEVICE	Spansion LLC	11/746122 5/9/07	20080280410
MANAGING FLASH MEMORY BASED UPON USAGE HISTORY	Spansion LLC	11/747608 5/11/07	20080279005
VARIABLE SALICIDE BLOCK FOR RESISTANCE EQUALIZATION IN AN ARRAY	Spansion LLC	11/748215 5/14/07	20080150007
METHODS OF FORMING SILICIDES OF DIFFERENT THICKNESSES ON DIFFERENT STRUCTURES	Spansion LLC & Advanced Micro Devices, Inc.	11/748743 5/15/07	20080286921
SEQUENCE OF ALGORITHMS TO COMPUTE EQUILIBRIUM PRICES IN NETWORKS	Spansion LLC & Microsoft Corporation	11/754877 5/29/07	20080103793
FAULTY DANGLING METAL ROUTE DETECTION	Spansion LLC	11/767620 6/25/07	20080315906
PROCESS APPLYING DIE ATTACH FILM TO SINGULATED DIE	Spansion LLC	11/767623 6/25/07	20080318364
A SEMICONDUCTOR DEVICE FOR STACKING DIES IN A MULTIDIE CHIP PACKING USING FILM OVER WIRE AS WELL AS MULTIDIE CHIP DEVICES THAT INCLUDE FILM OVER WIRE	Spansion LLC	11/770239 6/28/07	20090001599

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AVOIDING FIELD OXIDE GOUGING IN SHALLOW TRENCH ISOLATION (STI) REGIONS DEVICE HAVING A PROTECTIVE CAP FORMED OVER AN ANTIREFLECTIVE COATING LAYER AND OVER AN INSULATING MATERIAL (TITLE ON WEBSITE)	Spansion LLC	11/781551 7/23/07	20070262412
SYSTEM AND METHOD FOR REDUCING PROCESS INDUCED CHARGING	Spansion LLC	11/782,507 7/24/2007	20070267686
SELECTION OF A LOOKUP TABLE WITH DATA MASKED WITH A COMBINATION OF AN ADDITIVE AND MULTIPLICATIVE MASK	Spansion LLC	11/788264 4/19/07	20080260145
EXHAUST SYSTEM	Spansion LLC & Mitsubishi Cable Industries, Ltd & Spansion Japan Ltd. & Osaka Rasenkan Kogyo Co., Ltd.	11/790305 4/24/07	20080072585
MEMORY DEVICE WITH IMPROVED PERFORMANCE	Spansion LLC & Globalfoundries Inc.	11/796073 4/26/07	20080265240
SELFALIGNED PATTERNING METHOD BY USING NONCONFORMAL FILM AND ETCH BACK FOR FLASH MEMORY AND OTHER SEMICONDUCTOR APPLICATIONS	Spansion LLC	11/796582 4/26/07	20080265301
FLASH MEMORY CELL WITH A FLAIR GATE	Spansion LLC	11/801823 5/10/07	20080277712
SELF REFERENCE SENSING SYSTEM AND METHOD	Spansion LLC	11/804170 5/16/07	20080285354
METHOD OF CONSTRUCTING A STACKEDDIE SEMICONDUCTOR STRUCTURE	Spansion LLC	11/821653 6/25/07	20080318348
FUEL CELL USING DEUTERIUM	Spansion LLC	11/829135 7/27/07	20090029202

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USE OF A POLYMER SPACER AND SI TRENCH IN A BITLINE JUNCTION OF A FLASH MEMORY CELL TO IMPROVE TPD CHARACTERISTICS	Spansion LLC	11/835538 8/8/07	20090042378
ORO AND ORPRO WITH BIT LINE TRENCH TO SUPPRESS TRANSPORT PROGRAM DISTURB	Spansion LLC	11/835542 8/8/07	20090039405
CAPACITOR STRUCTURE USED FOR FLASH MEMORY	Spansion LLC	11/838483 8/14/07	20090045445
DIE STACKING IN MULTIDIE STACKS USING DIE SUPPORT MECHANISMS	Spansion LLC	11/842655 8/21/07	20090051043
PROCESS OF FORMING AN ELECTRONIC DEVICE INCLUDING DEPOSITING LAYERS WITHIN OPENINGS	Spansion LLC	11/844518 8/24/07	20090050471
SACRIFICIAL NITRIDE AND GATE REPLACEMENT	Spansion LLC	11/847507 8/30/07	20090061650
MAIN MEMORY IN A SYSTEM WITH A MEMORY CONTROLLER CONFIGURED TO CONTROL ACCESS TO NONVOLATILE MEMORY, AND RELATED TECHNOLOGIES	Spansion LLC	11/847986 8/30/07	20080082731
SYSTEMS AND APPARATUS FOR MAIN MEMORY WITH NONVOLATILE TYPE MEMORY MODULES, AND RELATED TECHNOLOGIES	Spansion LLC	11/848013 8/30/07	20080082732
METHODS FOR MAIN MEMORY WITH NONVOLATILE TYPE MEMORY MODULES, AND RELATED TECHNOLOGIES	Spansion LLC	11/848040 8/30/07	20080082733
METHODS FOR MAIN MEMORY IN A SYSTEM WITH A MEMORY CONTROLLER CONFIGURED TO CONTROL ACCESS TO NONVOLATILE MEMORY, AND RELATED TECHNOLOGIES	Spansion LLC	11/848083 8/30/07	20080082734
GATE REPLACEMENT WITH TOP OXIDE REGROWTH FOR THE TOP OXIDE IMPROVEMENT	Spansion LLC	11/848515 8/31/07	20090061631

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SECURE MODULAR EXPONENTIATION BY RANDOMIZATION OF EXPONENT SCANNING	Spansion LLC	11/852644 9/10/07	20090067617
RANDOMIZED RSABASED CRYPTOGRAPHIC EXPONENTIATION RESISTANT TO SIDE CHANNEL AND FAULT ATTACKS	Spansion LLC	11/870102 10/10/07	20090097637
HYBRID FLASH MEMORY DEVICE	Spansion LLC	11/873810 10/17/07	20090106481
SPLIT CHARGE STORAGE NODE INNER SPACER PROCESS	Spansion LLC	11/873822 10/17/07	20090101963
PHOTOVOLTAIC THIN COATING FOR COLLECTOR GENERATOR	Spansion LLC	11/873824 10/17/07	20090104432
TAMPER REACTIVE MEMORY DEVICE TO SECURE DATA FROM TAMPER ATTACKS	Spansion LLC	11/873980 10/17/07	20090106563
OPTIMIZE PERSONALIZATION CONDITIONS FOR ELECTRONIC DEVICE TRANSMISSION RATES WITH INCREASED TRANSMITTING FREQUENCY	Spansion LLC	11/874001 10/17/07	20090106577
SECURE PERSONALIZATION OF MEMORYBASED ELECTRONIC DEVICES	Spansion LLC	11/874036 10/17/07	20090106483
FAST SINGLE PHASE PROGRAM ALGORITHM FOR QUADBIT	Spansion LLC	11/874076 10/17/07	20090103357
LOWDENSITY PARITYCHECK CODE BASED ERROR CORRECTION FOR MEMORY DEVICE	Spansion LLP	11/877497 10/23/07	20090106626
CONTACT CONFIGURATION FOR UNDERTAKING TESTS ON CIRCUIT BOARD	Spansion LLC	11/881969 7/30/07	20090033334
EXPOSURE SYSTEM, SEMICONDUCTOR DEVICE, AND METHOD FOR FABRICATING THE SEMICONDUCTOR DEVICE	Spansion LLC	11/894,921 8/22/2007	20070290254

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IC CARRIER, IC SOCKET AND METHOD FOR TESTING IC DEVICE	Spansion LLC & Micronics Japan Co., Ltd. & Spansion Japan Limited	11/886139 3/13/08	20080191723
METHOD AND STRUCTURE OF MINIMIZING MOLD BLEEDING ON A SUBSTRATE SURFACE OF A SEMICONDUCTOR PACKAGE	Spansion LLC	11/895901 8/28/07	20090057883
TALINED TUNGSTEN PLUGS FOR TRANSISTORLOCAL HYDROGEN GATHERING	Spansion LLC	11/899575 9/6/07	20090065842
METHOD OF FORMING CONTROLLABLY CONDUCTIVE OXIDE	Spansion	11/899597 9/6/07	20090067213
SPLIT CHARGE STORAGE NODE OUTER SPACER PROCESS	Spansion LLC	11/924169 10/25/07	20090108330
SELECTIVE SILICIDE FORMATION USING RESIST ETCHBACK	Spansion LLC	11/924823 10/26/07	20090111265
SIGNAL DESCRAMBLING DETECTOR	Spansion LLC	11/928372 10/30/07	20090109769
ERROR CORRECTION CODING IN FLASH MEMORY DEVICES	Spansion LLC	11/928434 10/30/07	20090113272
NONVOLATILE MEMORY ARRAY PARTITIONING ARCHITECTURE AND METHOD TO UTILIZE SINGLE LEVEL CELLS AND MULTILEVEL CELLS WITHIN THE SAME MEMORY	Spansion LLC	11/928865 10/30/07	20090113115
CONTROL OF TEMPERATURE SLOPE FOR BAND GAP REFERENCE VOLTAGE IN A MEMORY DEVICE	Spansion LLC	11/929097 10/30/07	20090109742
DETERMINISTIC PROGRAMMING ALGORITHM THAT PROVIDES TIGHTER CELL DISTRIBUTIONS WITH A REDUCED NUMBER OF PROGRAMMING PULSES	Spansion LLC	11/929741 10/30/07	20090109760

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NONVOLATILE MEMORY ARRAY PARTITIONING ARCHITECTURE AND METHOD TO UTILIZE SINGLE LEVEL CELLS AND MULTI LEVEL CELLS WITHIN SAID ARCHITECTURE	Spansion LLC	11/929761 10/30/07	20090109758
FLASH MEMORY DEVICE HAVING IMPROVED PROGRAM RATE	Spansion L.L.C.	11/931992 10/31/07	20080049516
PROCESSES FOR FORMING ELECTRONIC DEVICES INCLUDING POLISHING METALCONTAINING LAYERS	Spansion LLC	11/934628 11/2/07	20090117734
PROCESS OF FORMING AN ELECTRONIC DEVICE INCLUDING DEPOSITING A CONDUCTIVE LAYER OVER A SEED LAYER	Spansion LLC	11/935544 11/6/07	20090114542
CONTROLLED BIT LINE DISCHARGE FOR CHANNEL ERASES IN NONVOLATILE MEMORY	Spansion LLC	11/935717 11/6/07	20090119447
HIGH RELIABLE AND LOW POWER STATIC RANDOM ACCESS MEMORY	Spansion LLC	11/942526 11/19/07	20090129172
MEMORY BUFFERING SYSTEM THAT IMPROVES READ/WRITE PERFORMANCE AND PROVIDES LOW LATENCY FOR MOBILE SYSTEMS	Spansion LLC	11/943544 11/20/07	20090132736
SPI BANK ADDRESSING SCHEME FOR MEMORY DENSITIES ABOVE 128MB	Spansion LLC	11/945292 11/27/07	20090138626
SPI AUTOBOOT MODE	Spansion LLC	11/945316 11/27/07	20090138694
MULTIBUS ARCHITECTURE FOR MASS STORAGE SYSTEMONCHIP CONTROLLERS	Spansion LLC	11/945534 11/27/07	20090138628
ROOM TEMPERATURE DRIFT SUPPRESSION VIA SOFT PROGRAM AFTER ERASE	Spansion LLC	11/945785 11/27/07	20090135659

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WEAVABLE FIBER PHOTOVOLTAIC COLLECTORS	Spansion LLC	11/947424 11/29/07	20090139572
DIRECT INTERCONNECTION BETWEEN PROCESSOR AND MEMORY COMPONENT	Spansion, LLC	11/949521 12/3/07	20090144486
DATA TRANSMISSION SYSTEMONCHIP MEMORY MODEL BASED VALIDATION	Spansion LLC	11/950006 12/4/07	20090144045
METHOD OF OPERATING A PROCESSING CHAMBER USED IN FORMING ELECTRONIC DEVICES	Spansion LLC	11/950339 12/4/07	20090142473
CIRCUIT PRECHARGE TO SENSE A MEMORY LINE	Spansion LLC	11/951262 12/5/07	20090147587
MEMORY ARRAY SEARCH ENGINE	Spansion LLC	11/953501 12/10/07	20090150646
SELECTIVE APPLICATION OF WORD LINE BIAS TO MINIMIZE FRINGE EFFECTS IN ELECTROMAGNETIC FIELDS DURING ERASE OF NONVOLATILE MEMORY	Spansion LLC	11/953689 12/10/07	20090147589
WORK FUNCTION ENGINEERING FOR FN ERASE OF A MEMORY DEVICE WITH MULTIPLE CHARGE STORAGE ELEMENTS IN AN UNDERCUT REGION	Spansion LLC	11/953690 12/10/07	20090146201
POWER SAFE TRANSLATION TABLE OPERATION IN FLASH MEMORY	Spansion, LLC	11/955934 12/13/07	20090158085
PROGRAMMING IN MEMORY DEVICES USING SOURCE BITLINE VOLTAGE BIAS	Spansion LLC	11/956032 12/13/07	20090154246
CLOCK ENCODED PREFETCH TO ACCESS MEMORY DATA IN CLUSTERING NETWORK ENVIRONMENT	Spansion LLC	11/957027 12/14/07	20090158005
REDUCING NOISE AND DISTURBANCE BETWEEN MEMORY STORAGE ELEMENTS USING ANGLED WORDLINES	Spansion LLC	11/957028 12/14/07	20090154215
INTELLIGENT MEMORY DATA MANAGEMENT	Spansion LLC	11/957226 12/14/07	20090157948

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SI TRENCH BETWEEN BITLINE HDP FOR BVDSS IMPROVEMENT	Spansion LLC	11/957737 12/17/07	20090152669
ADAPTIVE SYSTEM BOOT ACCELERATOR FOR COMPUTING SYSTEMS	Spansion LLC	11/957793 12/17/07	20090158023
METHODS OF FORMING ELECTRONIC DEVICES BY ION IMPLANTING	Spansion LLC	11/958223 12/17/07	20090155726
INTEGRATED CIRCUIT SYSTEM WITH MEMORY SYSTEM	Spansion LLC & Globalfoundries Inc.	11/958254 12/17/07	20080150042
REDUCED STATE QUADBIT	Spansion LLC	11/958557 12/18/07	20090154235
INTEGRATED CIRCUIT SYSTEM WITH MEMORY SYSTEM	Spansion LLC & Advanced Micro Devices, Inc.	11/958646 12/18/07	20080150011
EFFICIENT MEMORY HIERARCHY IN SOLID STATE DRIVE DESIGN	Spansion LLC	11/960601 12/19/07	20090164700
ELECTRONIC DEVICE INCLUDING A SILICON NITRIDE LAYER AND A PROCESS OF FORMING THE SAME	Spansion LLC	11/961757 12/20/07	20090159958
EXTENDING FLASH MEMORY DATA RETENSION VIA REWRITE REFRESH	Spansion LLC	11/961772 12/20/07	20090161466
FREQUENCY DISTRIBUTED FLASH MEMORY ALLOCATION BASED ON FREE PAGE TABLES	Spansion LLC	11/962514 12/21/07	20090164702
ELECTRONIC DEVICES WITH ULTRAVIOLET BLOCKING LAYERS AND PROCESSES OF FORMING THE SAME	Spansion LLC	11/962714 12/21/07	20090159321
COMMAND QUEUING FOR NEXT OPERATIONS OF MEMORY DEVICES	Spansion LLC	11/962918 12/21/07	20090165020
RANDOM NUMBER GENERATION THROUGH USE OF MEMORY CELL ACTIVITY	Spansion LLC	11/962955 12/21/07	20090165086
ERROR CORRECTION IN FLASH MEMORY ARRAY	Spansion LLC	11/963078 12/21/07	20090164836

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DATA COMMIT ON MULTICYCLE PASS COMPLETE WITHOUT ERROR	Spansion LLC	11/963200 12/21/07	20090164750
FLEXIBLE FLASH INTERFACE	Spansion LLC	11/963241 12/21/07	20090164703
BIT MAP CONTROL OF ERASE BLOCK DEFECT LIST IN A MEMORY	Spansion LLC	11/963286 12/21/07	20090161430
PHYSICAL BLOCK ADDRESSING OF ELECTRONIC MEMORY DEVICES	Spansion LLC	11/963306 12/21/07	20090164696
SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME	Spansion LLC	11/963400 12/21/07	20080191321
METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE	Spansion LLC	11/963415 12/21/07	20080166853
HIGH PERFORMANCE FLASH CHANNEL INTERFACE	Spansion LLC	11/963466 12/21/07	20090164704
CONTROLLING AC DISTURBANCE WHILE PROGRAMMING	Spansion LLC	11/963508 12/21/07	20090161462
AUTHENTICATED MEMORY AND CONTROLLER SLAVE	Spansion LLC	11/963538 12/21/07	20090164789
TRANSLATION MANAGEMENT OF LOGICAL BLOCK ADDRESSES AND PHYSICAL BLOCK ADDRESSES	Spansion LLC	11/966919 12/28/07	20090172345
RELOCATING DATA IN A MEMORY DEVICE	Spansion LLC	11/966923 12/28/07	20090172250
METHOD FOR PROTECTING DATA AGAINST DIFFERNTIAL FAULT ANALYSIS INVOLVED IN RIVEST, SHAMIR, AND ADLEMAN CRYPTOGRAPHY USING THE CHINESE REMAINDER THEOREM	Spansion LLC	11/969106 1/3/08	20090175441
LOWH PLASMA TREATMENT WITH N2 ANNEAL FOR ELECTRONIC MEMORY DEVICES	Spansion LLC	11/971331 1/9/08	20090176369
NONVOLATILE MEMORY DEVICE AND METHODS OF USING	Spansion LLC	11/972312 1/10/08	20090180330

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SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE SAME	Spansion LLC	11/974295 10/11/07	20080098165
ERASE, PROGRAMMING AND LEAKAGE CHARACTERISTICS OF A RESISTIVE MEMORY DEVICE	Spansion LLC	11/980116 10/30/07	20090109727
METALINSULATORMETAL (MIM) DEVICE AND METHOD OF FORMATION THEREOF	Spansion LLC	11/980213 10/30/07	20090109598
CONTROLLING A SEMICONDUCTOR DEVICE	Spansion LLC	11/982,864	20080140880
REDUCTION OF PACKAGE HEIGHT IN A STACKED DIE CONFIGURATION	Spansion LLC	11/983041 11/5/07	20090115033
NONVOLATILE STORAGE DEVICE AND CONTROL METHOD THEREOF	Spansion LLC	11/986331 11/20/07	20080144388
MEMORY CELL ARRAY WITH LOW RESISTANCE COMMON SOURCE AND HIGH CURRENT DRIVABILITY	Spansion LLC	11/983,864 11/13/2007	20080298115
MEMORY CELL ARRAY WITH LOW RESISTANCE COMMON SOURCE AND HIGH CURRENT DRIVABILITY	Spansion LLC	11/985,018 11/13/2007	20080061283
MEMORY DEVICE AND PASSWORD STORING METHOD THEREOF	Spansion LLC	11/986332 11/20/07	20080147967
SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME	Spansion LLC	11/986370 11/20/07	20080157331
MEMORY DEVICE WITH BARRIER LAYER	Spansion LLC	11/997464 7/21/06 1/31/2008 (On Website)	20080191269
CONVEX SHAPED THINFILM TRANSISTOR DEVICE	Spansion LLC	12/002728 12/17/07	20080157183

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METHOD TO PREVENT ALLOY FORMATION WHEN FORMING LAYERED METAL OXIDES BY METAL OXIDATION	Spansion LLC	12/004124 12/20/07	20090163018
REDUCTION OF DEFECTS FORMED ON THE SURFACE OF A SILICON OXYNITRIDE FILM	Spansion LLC	12/004676 12/20/07	20090023299
SEMICONDUCTOR DEVICE, METHOD OF CONTROLLING THE SAME, AND METHOD OF MANUFACTURING THE SAME	Spansion LLC	12/004919 12/21/07	20080157259
SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME	Spansion LLC	12/004920 12/21/07	20090026609
HEAT DISSIPATION METHODS AND STRUCTURES FOR SEMICONDUCTOR DEVICE	Spansion LLC	12/004960 12/20/07	20080211079
METHODS AND STRUCTURES FOR DISCHARGING PLASMA FORMED DURING THE FABRICATION OF SEMICONUCTOR DEVICE	Spansion LLC	12/004969 12/20/07	20090026570
SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME	Spansion LLC	12/005869 12/28/07	20090020799
SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME	Spansion LLC	12/005870 12/28/07	20090020885
TABLE LOOKUP VOLTAGE COMPENSATION FOR MEMORY CELLS	Spansion LLC	12/006744 1/4/08	20090175112
FLIPCHIP PACKAGE COVERED WITH TAPE	Spansion, LLC	12/012388 2/1/08	20090039531
PROGRAM AND ERASE DIABLING CONTROL OF WPCAM BY DOUBLE CONTROLS	Spansion LLC	12/012390 2/1/08	20090049253
SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME	Spansion, LLC	12/012849 2/5/08	20080185628
VOLTAGE BOOSTER BY ISOLATION AND DELAYED SEQUENTIAL DISCHARGE	Spansion LLC	12/014454 1/15/08	20090180345

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RETARGETING OF A WRITE OPERATION RETRY IN THE EVENT OF A WRITE OPERATION FAILURE	Spansion LLC	12/016674 1/18/08	20090187700
ELECTRONIC DEVICE INCLUDING A GATE ELECTRODE HAVING PORTIONS WITH DIFFERENT CONDUCTIVITY TYPES AND A PROCESS OF FORMING THE SAME	Spansion LLC	12/020316 1/25/08	20090189202
TRANSLATION TABLE COHERENCY MECAHANISM USING CACHE WAY AND SET INDEX WRITE BUFFERS	Spansion, LLC	12/020698 1/28/08	20090193193
ELECTRONIC DEVICE HAVING A DOPED REGION WITH A GROUP 13 ATOM	Spansion LLC	12/022795 1/30/08	20090189212
EXPANSION SLOTS FOR FLASH MEMORY BASED MEMORY SUBSYSTEM	Spansion LLC	12/026296 2/5/08	20090198871
HARDWARE BASED WEAR LEVELING MECHANISM	Spansion LLC	12/026299 2/5/08	20090198872
PARTIAL ALLOCATE PAGING MECHANISM	Spansion LLC	12/026302 2/5/08	20090198873
MITIGATE FLASH WRITE LATENCY AND BANDWIDTH LIMITATION	Spansion LLC	12/026362 2/5/08	20090198874
SEMICONDUCTOR DEVICE AND METHOD FOR ADJUSTING REFERENCE LEVELS OF REFERENCE CELLS	Spansion LLC	12/026417 2/5/08	20080192537
SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME	Spansion LLC	12/026421 2/5/08	20080217673
SEMICONDUCTOR MANUFACTURING EQUIPMENT AND MANUFACTURING METHOD OF THE SAME	Spansion LLC	12/026425 2/5/08	20080210170
MEMORY DEVICE AND METHOD THEREOF	Spansion LLC	12/030485 2/13/08	20090201724

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METHOD OF FORMING AN ELECTRONIC DEVICE INCLUDING FORMING FEATURES WITHIN A MASK AND A SELECTIVE REMOVAL PROCESS	Spansion LLC	12/031458 2/14/08	20090209107
SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME	Spansion, LLC	12/032444 2/15/08	20090051051
DECODING SYSTEM CAPABLE OF CHARGING PROTECTION FOR FLASH MEMORY DEVICES	Spansion LLC	12/034316 2/20/08	20090206386
SECURE DATA TRANSFER AFTER AUTHENTICATION BETWEEN MEMORY AND A REQUESTER	Spansion LLC	12/038059 2/27/08	20090217058
SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME	Spansion LLC	12/039511 2/28/08	20090072394
MEMORY DEVICE AND CHIP SET PROCESSOR PAIRING	Spansion LLC	12/039941 2/29/08	20090222910
SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME	Spansion LLC	12/044851 3/7/08	20080217792
USING LPDDR1 BUS AS TRANSPORT LAYER TO COMMUNICATE TO FLASH	Spansion LLC	12/048474 3/14/08	20090235012
METHOD OF FORMING BIT LINES FOR SEMICONDUCTOR DEVICES	Spansion LLC	12/048549 3/14/08	20080157187
SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THEREOF	Spansion LLC	12/049089 3/14/08	20080224275
SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THEREOF	Spansion LLC	12/049900 3/17/08	20080230898
WIRELESS MASS STORAGE FLASH MEMORY	Spansion LLC	12/050544 3/18/08	20090239468
DUAL BIT FLASH MEMORY DEVICES AND METHODS FOR FABRICATING THE SAME	Spansion LLC	12/054,081 3/24/2008	20080169502

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SECURE MANAGEMENT OF MEMORY REGIONS IN A MEMORY	Spansion LLC	12/054740 3/25/08	20090249014
FUEL CELL CATALYST REGENERATION	Spansion LLC	12/056562 3/27/08	20090246584
BITLINE VOLTAGE DRIVER	Spansion, LLC	12/057203 3/27/08	20090244989
NONVOLATILE MEMORY DEVICE, NONVOLATILE MEMORY SYSTEM AND CONTROL METHOD FOR THE NONVOLATILE MEMORY DEVICE	Spansion LLC	12/058471 3/28/08	20080247233
OPERATING SYSTEM BASED DRAM / FLASH MANAGEMENT SCHEME	Spansion LLC	12/059784 3/31/08	20090249015
MEMORY RESOURCE MANAGEMENT FOR A FLASH AWARE KERNEL	Spansion LLC	12/059795 3/31/08	20090248957
FLASH MEMORY USABILITY ENHANCEMENTS IN MAIN MEMORY APPLICATION	Spansion LLC	12/059809 3/31/08	20090248958
FLASH MEMORY AND OPERATING SYSTEM KERNEL	Spansion LLC	12/059816 3/31/08	20090248959
NONVOLATILE MEMORY DEVICE AND METHOD TO CONTROL THE SAME	Spansion, LLC	12/060710 4/1/08	20080266934
DIODE AND RESISTIVE MEMORY DEVICE STRUCTURES	Spansion LLC	12/072588 2/27/08	20090212283
CONNECTIONS FOR ELECTRONIC DEVICES ON DOUBLESIDED CIRCUIT BOARD	Spansion LLC	12/080311 4/2/08	20090250255
METHOD OF IMPROVING ADHESION OF DIELECTRIC CAP TO COPPER	Spansion LLC	12/082988 4/16/08	20090260759
SEMICONDUCTOR DEVICE SEALED IN A RESIN SECTION AND METHOD FOR MANUFACTURING THE SAME	Spansion LLC	12/098248 4/4/08	20090020890

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METHOD OF FORMING AN ELECTRONIC DEVICE INCLUDING FORMING A CHARGE STORAGE ELEMENT IN A TRENCH OF A WORKPIECE	Spansion LLC	12/102488 4/14/08	20090256242
USE OF SILICONRICH NITRIDE IN A FLASH MEMORY DEVICE	Spansion LLC	12/105208 4/17/08	20090261406
OPTICAL ERASE MEMORY STRUCTURE	Spansion LLC	12/106180 4/18/08	20090261367
NONVOLATILE STORAGE DEVICE AND BIAS CONTROL METHOD THEREOF	Spansion, LLC	12/109239 4/24/08	20080316821
STRUCTURES AND METHODS FOR STACK TYPE SEMICONDUCTOR PACKAGING	Spansion LLC	12/110181 4/25/08	20090115044
METHODS FOR FABRICATING MEMORY CELLS HAVING FIN STRUCTURES WITH SEMICIRCULAR TOP SURFACES AND ROUNDED TOP CORNERS AND EDGES	Spansion, LLC	12/110974 4/28/08	20090269916
METHODS FOR FABRICATING MEMORY CELLS HAVING FIN STRUCTURES WITH SMOOTH SIDEWALLS AND ROUNDED TOP CORNERS AND EDGES	Spansion, LLC	12/111122 4/28/08	20090269918
WORDLINE RESISTANCE REDUCTION METHOD AND STRUCTURE IN AN INTEGRATED CIRCUIT MEMORY DEVICE	Spansion, LLC	12/111886 4/29/08	20090268500
BITCELL CURRENT SENSE DEVICE AND METHOD THEREOF	Spansion LLC	12/114966 5/5/08	20090273998
MEMORY DEVICE INTERCONNECTS AND METHOD OF MANUFACTURING	Spansion LLC	12/116200 5/6/08	20090278173
STRUCTURE, METHOD AND SYSTEM FOR ASSESSING BONDING OF ELECTRODES IN FCB PACKAGING	Spansion LLC	12/122556 5/16/08	20080303144
MULTIPLE PROGRAMMING OF SPARE MEMORY REGION FOR NONVOLATILE MEMORY	Spansion LLC	12/126686 5/23/08	20090129147

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ADDRESS CACHING STORED TRANSLATION	Spansion LLC	12/127919 5/28/08	20090300318
ENHANCED ERASING OPERATION FOR NONVOLATILE MEMORY	Spansion LLC	12/129530 5/29/08	20080298136
INSTANT HARDWARE ERASE FOR CONTENT RESET AND PSEUDORANDOM NUMBER GENERATION	Spansion LLC	12/129737 5/30/08	20090300312
METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE	Spansion LLC	12/130537 5/30/08	20090004838
SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME AND SEMICONDUCTOR MANUFACTURING DEVICE	Spansion LLC	12/130577 5/30/08	20080316790
SEMICONDUCTOR DEVICE AND CONTROLLING METHOD FOR THE SAME	Spansion LLC	12/130583 5/30/08	20090010076
ULTRAVIOLET BLOCKING STRUCTURE AND METHOD FOR SEMICONDUCTOR DEVICE	Spansion LLC	12/133689 6/5/08	20090174041
PRECISION TRENCH FORMATION FOR SEMICONDUCTOR DEVICE	Spansion LLC	12/134087 6/5/08	20080305614
MEMORY DEVICE AND METHOD	Spansion LLC	12/134898 6/6/08	20090303793
MEMORY DEVICE AND METHOD	Spansion LLC	12/134902 6/6/08	20090303795
MEMORY DEVICE AND METHOD	Spansion LLC	12/134905 6/6/08	20090303798
SHADOW WRITE AND TRANSFER SCHEMES FOR MEMORY DEVICES	Spansion LLC	12/137443 6/11/08	20090150701
COMMAND CONTROL FOR SYNCHRONOUS MEMORY DEVICE	Spansion LLC	12/138307 6/12/08	20090150635
SEMICONDUCTOR DEVICE AND METHOD FOR CONTROLLING THEREOF	Spansion LLC	12/139274 6/13/08	20080320208

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ERROR CORRECTION SCHEME FOR NONVOLATILE MEMORY	Spansion LLC	12/139650 6/16/08	20090158123
SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THEREOF	Spansion LLC	12/165331 6/30/08	20090121361
SEMICONDUCTOR DEVICE AND METHOD FOR CONTROLLING A SEMICONDUCTOR DEVICE	Spansion LLC	12/166288 7/1/08	20090010069
METHOD AND APPARATUS FOR MANUFACTURING SEMICONDUCTOR DEVICE	Spansion LLC	12/166290 7/1/08	20090011600
CARRIER FOR STACKED TYPE SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING STACKED TYPE SEMICONDUCTOR DEVICES	Spansion LLC	12/166,293 7/1/2008	20080274591
PROBE APPARATUS, A PROCESS OF FORMING A PROBE HEAD, AND A PROCESS OF FORMING AN ELECTRONIC DEVICE	Spansion LLC	12/174743 7/17/08	20100013504
SYNCHRONOUS MEMORY DEVICES AND CONTROL METHODS FOR PERFORMING BURST WRITE OPERATIONS	Spansion LLC	12/176997 7/21/08	20090207672
NONVOLATILE MEMORY DEVICE HAVING A PLURALITY OF MEMORY BLOCKS	Spansion LLC	12/177039 7/21/08	20090034334
FLASH MEMORY DEVICE WITH WORD LINES OF UNIFORM WIDTH AND METHOD FOR MANUFACTURING THEREOF	Spansion LLC	12/179400 7/24/08	20090184427
STACKED DIE PACKAGE HAVING REDUCED HEIGHT AND METHOD OF MAKING SAME	Spansion LLC	12/180,185 7/25/2008	20100019392
LATERAL CHARGE STORAGE REGION FORMATION FOR SEMICONDUCTOR WORDLINE	Spansion LLC	12/180306 7/25/08	20090184361
THERMOELECTRIC DEVICE FOR USE WITH STIRLING ENGINE	Spansion LLC	12/180910 7/28/08	20100018202
SELFALIGNED CHARGE STORAGE REGION FORMATION FOR SEMICONDUCTOR DEVICE	Spansion LLC	12/183756 7/31/08	20090032864

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APPARATUS AND METHOD FOR A MEMORY ARRAY WITH SHALLOW TRENCH ISOLATION REGIONS BETWEEN BIT LINES FOR INCREASED PROCESS MARGINS	Spansion LLC	12/187,276 8/6/2008	20090047762
MIRROR BIT MEMORY DEVICE APPLYING A GATE VOLTAGE ALTERNATELY TO GATE	Spansion LLC	12/192923 8/15/08	20090212348
USHAPED SONOS MEMORY HAVING AN ELEVATED SOURCE AND DRAIN	Spansion LLC	12/192945 8/15/08	20090200599
METHOD FOR MANUFACTURING SONOS FLASH MEMORY	Spansion LLC	12/193266 8/18/08	20090209076
PLASMA TREATED METAL SILICIDE LAYER FORMATION	Spansion LLC	12/195307 8/20/08	20090053867
SEPERATION METHODS FOR SEMICONDUCTOR CHARGE ACCUMULATION LAYERS AND STRUCTURES THEREOF	Spansion LLC	12/195324 8/20/08	20090206388
SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THEREOF	Spansion LLC	12/196156 8/21/08	20090206462
STACKED SOLDER BALLS FOR INTEGRATED CIRCUIT DEVICE PACKAGING AND ASSEMBLY	Spansion LLC	12/196210 8/21/08	20090212423
METHOD AND APPARATUS FOR ADDRESS ALLOTTING AND VERIFICATION IN A SEMICONDUCTOR DEVICE	Spansion Inc.	12/199,684 8/27/2008	20080316787
MANUFACTURING STACKED SEMICONDUCTOR DEVICE	Spansion LLC	12/210113 9/12/08	20090230533
SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THEREOF	Spansion LLC	12/217096 7/1/08	20090008747
SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREOF	Spansion LLC	12/233577 9/18/08	20090251970
SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF	Spansion LLC	12/234337 9/19/08	20090236721

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SONOS DEVICE WITH INSULATING STORAGE LAYER AND PN JUNCTION ISOLATION	Spansion LLC	12/235321 9/22/08	20090237990
SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR	Spansion LLC	12/239566 9/26/08	20090250800
SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREFOR	Spansion LLC	12/240767 9/29/08	20090250697
SYSTEM AND METHOD OF OPERATION FOR RESISTIVE CHANGE MEMORY	Spansion LLC	12/243836 10/1/08	20090251945
METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE BY CONSIDERING THE EXTINCTION COEFFICIENT DURING ETCHING OF AN INTERLAYER INSULATING FILM	Spansion LLC	12/253035 10/16/08	20090269864
SEMICONDUCTOR MEMORY DEVICE WITH STACKED MEMORY CELL STRUCTURE	Spansion LLC	12/253619 10/17/08	20090262569
SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THEREOF	Spansion LLC	12/256333 10/22/08	20090302469
SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF	Spansion LLC	12/258067 10/24/08	20090267207
SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THEREOF	Spansion LLC	12/259100 10/27/08	20090289336
SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE SAME	Spansion LLC	12/275,121 11/20/2008	20090109757
SEMICONDUCTOR DEVICE AND ITS CONTROL METHOD	Spansion LLC	12/283,721 9/15/2008	20090034335
SEMICONDUCTOR DEVICE AND ITS CONTROL METHOD	Spansion LLC	12/283,722 9/15/2008	20090016109
RESISTIVE MEMORY CELL ARRAY WITH COMMON PLATE	Spansion LLC	12/290,179 10/28/2008	20090059652

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TEST STUCTURES FOR DEVELOPMENT OF METALINSULATORMETAL (MIM) DEVICES	Spansion LLC	12/313,089 11/17/2008	20090072234
CARRIER STRUCTURE FOR STACKEDTYPE SEMICONDUCTOR DEVICE, METHOD OF PRODUCING THE SAME, AND METHOD OF FABRICATING STACKEDTYPE SEMICONDUCTOR DEVICE	Spansion LLC	12/315,417 12/3/2008	20090093085
DIE OFFSET DIE TO BONDING	Spansion LLC	12/316,041 12/9/2008	7,674,653 3/9/2010
DIE OFFSET DIE TO DIE BONDING	Spansion LLC	12/316,042 12/9/2008	20090091043
STACKED ORGANIC MEMORY DEVICES AND METHODS OF OPERATING AND FABRICATING	Spansion LLC	12/327040 12/3/08	20090081824
FLASH MEMORY DEVICE WITH STRAIGHT WORD LINES	Spansion LLC	12/327,641 12/3/2008	20090138570
METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE	Spansion LLC	12/332,146 12/10/2008	20090311831
ELECTRONIC CIRCUIT	Spansion LLC	12/334221 12/12/08	20090153125
SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING	Spansion LLC	12/336757 12/17/08	20090315097
STACKED SEMICONDUCTOR DEVICES AND A METHOD FOR FABRICATING THE SAME	Spansion LLC	12/337396 12/17/08	20090315166
SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING	Spansion LLC	12/337461 12/17/08	20090315098
FORMING METALSEMICONDUCTOR FILMS HAVING DIFFERENT THICKNESSES WITHIN DIFFERENT REGIONS OF AN ELECTRONIC DEVICE	Spansion LLC	12/340274 12/19/08	20090140325

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SEMICONDUCTOR DEVICE HAVING A SIMPLIFIED STACK AND METHOD FOR MANUFACTURING THEREOF	Spansion LLC	12/341863 12/22/08	20090321958
SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THEREOF	Spansion LLC	12/341874 12/22/08	20090321812
SEMICONDUCTOR DEVICE AND METHOD FOR CONTROLLING	Spansion LLC	12/341879 12/22/08	20100002517
TIME REDUCTION OF ADDRESS SETUP/HOLD TIME FOR SEMICONDUCTOR MEMORY	Spansion LLC	12/341886 12/22/08	20090323435
FLIP CHIP PACKAGE WITH SHELF AND METHOD OF MANUFACTURING THE SAME	Spansion LLC	12/343348 12/23/08	20090200684
SONOSNAND DEVICE HAVING A STORAGE REGION SEPARATED BETWEEN CELLS	Spansion LLC	12/343998 12/24/08	20100001336
HIGH K STACK FOR NONVOLATILE MEMORY	Spansion LLC	12/351553 1/9/09	20090155992
SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD	Spansion LLC	12/404,146 3/13/2009	20090174057
METHOD AND ARCHITECTURE FOR FAST FLASH MEMORY PROGRAMMING	Spansion LLC	12/405,947 3/17/2009	20090175088
SEMICONDUCTOR DEVICE AND METHOD FOR BOOSTING WORD LINE	Spansion LLC	12/406,845 3/18/2009	20090175096
SWITCHABLE MEMORY DIODE A NEW MEMORY DEVICE	Spansion LLC	12/470825 5/22/09	20090233422
IMAGING DEVICE	Spansion LLC	12/472735 5/27/09	20090302203
SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD	Spansion LLC	12/491,092 6/24/2009	20090256250
SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME	Spansion LLC	12/491,970 6/25/2009	20090300275
AUTOMATED LOADING/UNLOADING OF DEVICES FOR BURNIN TESTING	Spansion LLC	12/492,922 6/26/2009	20090255915

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AUTOMATED LOADING/UNLOADING OF DEVICES FOR BURNIN TESTING	Spansion LLC	12/492,968 6/26/2009	20090261854
SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME	Spansion LLC	12/502,891 7/14/2009	20090325354
SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME	Spansion LLC	12/508,319 7/23/2009	20090279358
SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME	Spansion LLC	12/512,638 7/30/2009	20090285019
MEMORY DEVICE PERIPHERAL INTERCONNECTS AND METHOD OF MANUFACTURING	Spansion LLC	12/512960 7/30/09	20090289369
SEMICONDUCTOR CONTACT FORMATION SYSTEM AND METHOD	Spansion LLC	12/539,480 8/11/2009	20090294969
SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR	Spansion LLC	12/543,404 8/18/2009	20100001333
READING ELECTRONIC MEMORY UTILIZING RELATIONSHIPS BETWEEN CELL STATE DISTRIBUTIONS	Spansion LLC	12/550642 8/31/09	20090316481
SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME	Spansion LLC	12/556,408 9/9/2009	20090325346
METHOD AND APPARATUS FOR ADAPTIVE MEMORY CELL OVERERASE COMPENSATION	Spansion LLC	12/574,079 10/6/2009	20100020607
SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME	Spansion LLC	12/574,413 10/6/2009	20100020214
SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME	Spansion LLC	12/574,427 10/6/2009	20100020598
NON-VOLATILE SONOSTYPE MEMORY DEVICE	Spansion LLC	12/574,884 10/7/2009	20100022081

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
SEMICONDUCTOR DEVICE, FABRICATION METHOD THEREOF, AND PHOTOMASK	Spansion LLC	12/575,122 10/7/2009	20100019241
IMAGING DEVICE	Spansion LLC	61/060,001 6/9/2008	20090302203
BACKTOBACK CAPACITOR CHARGE PUMPS	Spansion LLC	07/505292 4/5/90	5,008,799 4/16/91
HIGH VOLTAGE CHARGE PUMPS WITH SERIES CAPACITORS	Spansion LLC	07/505335 4/5/90	5,059,815 10/22/91
EPROM ELEMENT EMPLOYING SELFALIGNING PROCESS	Spansion LLC	07/581341 9/12/90	5,091,326 2/25/92
POWER CONTROL CIRCUIT	Spansion LLC	07/563061 8/6/90	5,113,373 5/12/92
METHOD OF PAGEMODE PROGRAMMING FLASH EEPROM CELL ARRAYS	Spansion LLC	07/668608 3/13/91	5,191,556 3/2/93
DRAIN POWER SUPPLY	Spansion LLC	07/964697 10/22/92	5,263,000 11/16/93
NEGATIVE POWER SUPPLY	Spansion LLC	07/964807 10/22/92	5,282,170 1/25/94
VPP POWER SUPPLY HAVING A REGULATOR CIRCUIT FOR CONTROLLING A REGULATED POSITIVE POT	Spansion LLC	07/964684 10/22/92	5,291,446 3/1/94
FLASH EEPROM ARRAY WITH HIGH ENDURANCE	Spansion LLC	08/057583 5/6/93	5,335,198 8/2/94
SECTORBASED REDUNDANCY ARCHITECTURE	Spansion LLC	08/112033 8/26/93	5,349,558 9/20/94
SYSTEM FOR ALLOWING A CONTENT ADDRESSABLE MEMORY TO OPERATE WITH MULTIPLE POWER VOLTAGE LEVELS	Spansion LLC	08/083736 6/25/93	5,357,458 10/18/94
INDEPENDENT ARRAY GROUNDS FOR FLASH EEPROM ARRAY WITH PAGED ERASE ARCHITECTURE	Spansion LLC	08/109887 8/23/93	5,365,484 11/15/94
OUTPUT BUFFER CIRCUIT FOR A LOW VOLTAGE EPROM Q	Spansion LLC	08/078711 6/17/93	5,367,206 11/22/94

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METHOD OF MAKING A FLASH EPROM DEVICE UTILIZING A SINGLE MASKING STEP FOR ETCHING AND IMPLANTING SOURCE REGIONS WITHIN THE EPROM CORE AND REDUNDANCY AREAS	Spansion LLC	08/165445 12/10/93	5,376,573 12/27/94
POWERON RESET CIRCUIT	Spansion LLC	07/964806 10/22/92	5,376,835 12/27/94
METHOD FOR MANUFACTURING A NONVOLATILE, VIRTUAL GROUND MEMORY ELEMENT	Spansion LLC	08/266744 6/28/94	5,384,272 1/24/95
DISTRIBUTED NEGATIVE GATE POWER SUPPLY	Spansion LLC	08/109881 8/23/93	5,406,517 4/11/95
NONVOLATILE MEMORY STRUCTURE INCLUDING PROTECTION AND STRUCTURE FOR MAINTAINING THRESHOLD STABILITY	Spansion LLC	08/322811 10/13/94	5,457,336 10/10/95
SELFALIGNED BURIED CHANNEL/JUNCTION STACKED GATE FLASH MEMORY CELL	Spansion LLC	08/299868 9/1/94	5,468,981 11/21/95
METHOD PROTECTING A STACKED GATE EDGE IN A SEMICONDUCTOR DEVICE FROM SELF ALIGNED SOURCE (SAS) ETCH	Spansion LLC	08/233174 4/25/94	5,470,773 11/28/95
MEMORY ARCHITECTURE FOR A THREE VOLT FLASH EEPROM	Spansion LLC	08/135224 10/13/93	5,477,499 12/19/95
METHOD FOR TIGHTENING VT DISTRIBUTION OF 5 VOLTONLY FLASH EEPROMS	Spansion LLC	08/362346 12/22/94	5,481,494 1/2/96
METHOD OF MAKING FLASH EEPROM MEMORY WITH REDUCED COLUMN LEAKAGE CURRENT	Spansion LLC	08/403460 3/14/95	5,482,881 1/9/96
METHOD FOR ELIMINATING OF CYCLINGINDUCED ELECTRON TRAPPING IN THE TUNNELING OXIDE OF 5 VOLT ONLY FLASH EEPROMS	Spansion LLC	08/320368 10/11/94	5,485,423 1/16/96

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
METHODS FOR BULK (OR BYTE) CHARGING AND DISCHARGING AN ARRAY OF FLASH EEPROM MEMORY CELLS	Spansion LLC	08/393636 2/24/95	5,491,657 2/13/96
BOOSTED AND REGULATED GATE POWER SUPPLY WITH REFERENCE TRACKING FOR MULTIDENSITY AND LOW VOLTAGE SUPPLY MEMORIES	Spansion LLC	08/160578 12/1/93	5,511,026 4/23/96
METHOD AND SYSTEM FOR PROTECTING A STACKED GATE EDGE IN A SEMI CONDUCTOR DEVICE FROM SELF ALIGNED SOURCE (SAS) ETCH IN A SEMI CONDUCTOR DEVICE	Spansion LLC	08/460603 6/1/95	5,517,443 5/14/96
METHOD AND APPARATUS FOR PROGRAMMING MEMORY DEVICES	Spansion LLC	08/227755 4/14/94	5,530,803 6/25/96
METHOD FOR PROTECTING A STACKED GATE EDGE IN A SEMICONDUCTOR DEVICE FROM SELF ALIGNED SOURCE (SAS) ETCH	Spansion LLC	08/433267 5/2/95	5,534,455 7/9/96
LAYERED LOW DIELECTRIC CONSTANT TECHNOLOGY	Spansion LLC	08/330871 10/28/94	5,534,731 7/9/96
HIGH ENERGY BURIED LAYER IMPLANT TO PROVIDE A LOW RESISTANCE PWELL IN A FLASH EPROM ARRAY	Spansion LLC	08/269478 7/1/94	5,541,875 7/30/96
NONVOLATILE MEMORY ARRAY WITH OVERERASE CORRECTION	Spansion LLC	08/487252 6/13/95	5,546,340 8/13/96
NOVEL PROCESSING TECHNIQUES FOR ACHIEVING PRODUCTIONWORTHY, LOW DIELECTRIC, LOW INTERCONNECT RESISTANCE AND HIGH PERFORMANCE ICS	Spansion LLC	08/360856 12/21/94	5,550,405 8/27/96
PROCESS FOR SELFALIGNED SOURCE FOR HIGH DENSITY MEMORY	Spansion LLC	08/500648 7/11/95	5,552,331 9/3/96

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NONVOLATILE MEMORY CELL FORMED USING SELF ALIGNED SOURCE IMPLANT	Spansion LLC	08/484580 6/7/95	5,553,018 9/3/96
FLASH EEPROM ARRAY WITH FLOATING SUBSTRATE ERASE OPERATION	Spansion LLC	08/508425 7/31/95	5,561,620 10/1/96
SELFALIGNED BURIED CHANNEL/JUNCTION STACKED GATE FLASH MEMORY CELL	Spansion LLC	08/299876 9/1/94	5,574,685 11/12/96
MULTISTEPPED THRESHOLD CONVERGENCE FOR A FLASH MEMORY ARRAY	Spansion LLC	08/269540 7/1/94	5,576,991 11/19/96
REDUCED COLUMN LEAKAGE DURING PROGRAMMING FOR A FLASH MEMORY ARRAY	Spansion LLC	08/426716 4/21/95	5,579,261 11/26/96
A SENSE CIRCUIT FOR A FLASH EEPROM CELL HAVING A NEGATIVE DELTA THRESHOLD VOLTAGE	Spansion LLC	08/483038 6/6/95	5,579,274 11/26/96
METHOD FOR READING A NONVOLATILE MEMORY ARRAY	Spansion LLC	08/432623 5/2/95	5,581,502 12/3/96
CHANNEL HOTCARRIER PAGE WRITE	Spansion LLC	08/493138 6/21/59	5,590,076 12/31/96
METHOD FOR DECREASING THE DISCHARGE TIME OF A FLASH EPROM CELL	Spansion LLC	08/450167 5/25/95	5,596,531 1/21/97
FLASH EEPROM ARRAY WITH FLOATING SUBSTRATE ERASE OPERATION	Spansion LLC	08/484252 6/7/95	5,598,369 1/28/97
CORRECTION METHOD LEADING TO A UNIFORM THRESHOLD VOLTAGE DISTRIBUTION FOR A FLASH EPROM	Spansion LLC	08/534141 9/26/95	5,608,672 3/4/97
FLASH EEPROM MEMORY WITH IMPROVED DISCHARGE SPEED USING SUBSTRATE BIAS AND METHOD THEREFOR	Spansion LLC	08/420989 4/7/95	5,617,357 4/1/97
FLASH EEPROM MEMORY WITH SEPARATE REFERENCE ARRAY	Spansion LLC	08/543684 10/16/95	5,629,892 5/13/97

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SYSTEM FOR CONSTANT FIELD ERASURE IN A FLASH EPROM	Spansion LLC	08/634512 4/18/96	5,629,893 5/13/97
NONVOLATILE MEMORY ARRAY CONTROLLER CAPABLE OF CONTROLLING MEMORY BANKS HAVING VARIABLE BIT WIDTHS	Spansion LLC	08/166124 12/10/93	5,630,099 5/13/97
PARALLEL PAGE BUFFER VERIFY OR READ OF CELLS ON A WORD LINE USING A SIGNAL FROM A REFERENCE CELL IN A FLASH MEMORY DEVICE	Spansion LLC	08/630919 4/5/96	5,638,326 6/10/97
OVERERASE CORRECTION FOR FLASH MEMORY WHICH LIMITS OVERERASE AND PREVENTS ERASE VERIFY ERRORS	Spansion LLC	08/547494 10/24/95	5,642,311 6/24/97
PROGRAM ALGORITHM FOR LOW VOLTAGE SINGLE POWER SUPPLY FLASH MEMORIES	Spansion LLC	08/551705 11/1/95	5,644,531 7/1/97
METHOD OF INHIBITING DEGRADATION OF ULTRA SHORT CHANNEL CHARGECARRYING DEVICES DURING DISCHARGE	Spansion LLC	08/486192 6/7/95	5,650,964 7/22/97
TEMPERATURE COMPENSATED REFERENCE FOR OVERERASE CORRECTION CIRCUITRY IN A FLASH MEMORY	Spansion LLC	08/551422 11/1/95	5,650,966 7/22/97
A FLASH EEPROM MEMORY WITH REDUCED COLUMN LEAKAGE CURRENT AND METHOD THEREFOR	Spansion LLC	08/684920 7/22/96	5,652,447 7/29/97
NONVOLATILE MEMORY CELL FORMED USING SELF ALIGNED SOURCE IMPLANT	Spansion LLC	08/474879 6/7/95	5,656,513 8/12/97
METHOD OF ERASING UPROM TRANSISTORS	Spansion LLC	08/371704 1/12/95	5,656,521 8/12/97
METHOD OF MAKING NONVOLATILE MEMORY CELL WITH VERICAL GATE OVERLAP AND ZERO BIRDS'BEAKS	Spansion LLC	08/474610 6/7/95	5,661,055 8/26/97

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ERASE METHOD FOR PAGE MODE MULTIPLE BITSPERCELL FLASH EEPROM	Spansion LLC	08/701288 8/22/96	5,675,537 10/7/97
NOVEL PROCESSING TECHNIQUES FOR ACHIEVING PRODUCTIONWORTHY, LOW DIELECTRIC, LOW INTERCONNECT RESISTANCE AND HIGH PERFORMANCE IC	Spansion LLC	08/463448 6/5/95	5,679,608 10/21/97
NONVOLATILE MEMORY CELL WITH VERTICAL GATE OVERLAP AND ZERO BIRDS BEAKS	Spansion LLC	08/469953 6/6/95	5,680,345 10/21/97
POWER SUPPLY INDEPENDENT CURRENT SOURCE FOR FLASH EPROM ERASURE	Spansion LLC	08/566204 12/1/95	5,680,348 10/21/97
LAYERED LOW DIELECTRIC CONSTANT TECHNOLOGY	Spansion LLC	08/459957 6/2/95	5,693,566 12/2/97
SEMICONDUCTOR DEVICE FROM SELFALIGNED SOURCE (SAS) ETCH IN A SEMICONDUCTOR DEVICE	Spansion LLC	08/769178 12/18/96	5,693,972 12/2/97
FAST 3STATE BOOSTER CIRCUIT	Spansion LLC	08/560459 11/17/95	5,708,387 1/13/98
FLASH EEPROM MEMORY WITH IMPROVED DISCHARGED SPEED USING SUBSTRATE BIAS AND METHOD THEREFOR	Spansion LLC	08/464024 6/5/95	5,708,588 1/13/98
MULTIPLE BITS PERCELL FLASH EEPROM CAPABLE OF CONCURRENTLY PROGRAMMING AND VERIFYING MEMORY CELLS AND REFERENCE CELLS	Spansion LLC	08/635995 4/22/96	5,712,815 1/27/98
BIAS SCHEME OF PROGRAM INHIBIT FOR RANDOM PROGRAMMING IN A NAND FLASH MEMORY	Spansion LLC	08/686641 7/24/96	5,715,194 2/3/98
APPARATUS AND METHOD FOR MULTIPLELEVEL STORAGE IN NONVOLATILE MEMORIES	Spansion LLC	08/757988 11/27/96	5,717,632 2/10/98
MULTIPLE BITSPERCELL FLASH SHIFT REGISTER PAGE BUFFER	Spansion LLC	08/669116 6/24/96	5,724,284 3/3/98

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WATCHDOG SYSTEM HAVING DATA DIFFERENTIATING MEANS FOR USE IN MONITORING OF SEMICONDUCTOR WAFER TESTING LINE	Spansion LLC	08/537116 9/29/95	5,726,920 3/10/98
DEVICE INCLUDING MEANS FOR PREVENTING TUNGSTEN SILICIDE LIFTING, AND METHOD OF FABRICATION THEREOF	Spansion LLC	08/744962 11/7/96	5,747,882 5/5/98
METHOD OF SCREENING HOT TEMPERATURE ERASE REJECTS AT ROOM TEMPERATURE	Spansion LLC	08/655357 5/24/96	5,751,633 5/12/98
A BIT LINE DISCHARGE METHOD FOR READING A MULTIPLE BITSPERCELL FLASH EEPROM	Spansion LLC	08/884547 6/27/97	5,754,475 5/19/98
BLOCK SELECT TRANSISTOR AND METHOD OF FABRICATION	Spansion LLC	08/745278 11/8/96	5,763,307 6/9/98
ELECTRICALLY ERASABLE REFERENCE CELL FOR ACCURATELY DETERMINING THRESHOLD VOLTAGE OF A NONVOLATILE MEMORY AT A PLURALITY OF THRESHOLD VOLTAGE LEVELS	Spansion LLC	08/757987 11/27/96	5,774,395 6/30/98
SIMPLIFIED PROCESS FOR FABRICATING FLASH EEPROM CELLS	Spansion LLC	08/582720 1/4/96	5,776,811 7/7/98
METHOD OF ELIMINATING OR REDUCING POLY1 OXIDATION AT STACKED GATE EDGE IN FLASH EPROM PROCESS	Spansion LLC	08/559082 11/17/95	5,789,295 8/4/98
MULTIPLE BITS PER CELL FLASH EEPROM MEMORY CELLS WITH WIDE PROGRAM AND ERASE VT WINDOW	Spansion LLC	08/853185 5/9/97	5,790,456 8/4/98
SYSTEM FOR PROVIDING TIGHT PROGRAM/ERASE SPEEDS THAT ARE INSENSITIVE TO PROCESS VARIATIONS	Spansion LLC	08/723558 9/30/96	5,793,249 8/11/98

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USING FLOATING GATE DEVICES AS SELECT GATE DEVICES FOR NAND FLASH MEMORY AND ITS BIAS SCHEME	Spansion LLC	08/668632 6/18/96	5,793,677 8/11/98
METHOD FOR ANNEALING DAMAGED SEMICONDUCTOR REGIONS ALLOWING FOR ENHANCED OXIDE GROWTH	Spansion LLC	08/799236 2/14/97	5,795,627 8/18/98
MEMORY DEVICE USING A REDUCED WORD LINE VOLTAGE DURING READ OPERATIONS AND A METHOD OF ACCESSING SUCH A MEMORY DEVICE	Spansion LLC	08/858589 5/19/97	5,796,651 8/18/98
METHOD OF MAKING NONVOLATILE MEMORY DEVICE HAVING A FLOATING GATE WITH ENHANCED CHARGE RETENTION	Spansion LLC	08/393138 2/21/95	5,801,076 9/1/98
HIGH VOLTAGE NMOS PASS GATE FOR INTEGRATED CIRCUIT WITH HIGH VOLTAGE GENERATOR	Spansion LLC	08/808,237 2/28/1997	5,801,579 9/1/1998
NONVOLATILE MEMORY DEVICE HAVING A FLOATING GATE WITH ENHANCED CHARGE RETENTION	Spansion LLC	08/815835 3/12/97	5,805,013 9/8/98
CHANNEL HOTCARRIER PAGE WRITE FOR NAND APPLICATIONS	Spansion LLC	08/810164 2/28/97	5,805,499 9/8/98
SYSTEM FOR CONSTANT FIELD ERASURE IN A FLASH EPROM	Spansion LLC	08/795024 2/4/97	5,805,502 9/8/98
WAFER CLEANING PROCEDURE USEFUL IN THE MANUFACTURE OF A NONVOLATILE MEMORY DEVICE	Spansion LLC	08/578178 12/29/95	5,811,334 9/22/98
SOURCELESS FLOATING GATE MEMORY DEVICE AND METHOD OF STORING DATA	Spansion LLC	08/589750 1/22/96	5,814,853 9/29/98
OPTIMIZED BIASING SCHEME FOR NAND READ AND HOTCARRIER WRITE OPERATIONS	Spansion LLC	08/810170 2/28/97	5,815,438 9/29/98

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E2PROM DEVICE HAVING ERASE GATE IN OXIDE ISOLATION REGION IN SHALLOW TRENCH AND METHOD OF MANUFACTURE THEREOF	Spansion LLC	08/610688 3/4/96	5,818,082 10/6/98
HIGH-VOLTAGE CMOS LEVEL SHIFTER	Spansion LLC	08/799,074 2/11/1997	5,821,800 10/13/1998
PROGRAMMED REFERENCE	Spansion LLC	08/160582 12/1/93	5,828,601 10/27/98
METHOD OF PROGRAMMING A MEMORY CELL TO CONTAIN MULTIPLE VALUES	Spansion LLC	08/745596 11/8/96	5,831,901 11/3/98
HIGH VOLTAGE NMOS PASS GATE HAVING SUPPLY RANGE, AREA, AND SPEED ADVANTAGES	Spansion LLC	08/914543 8/19/97	5,844,840 12/1/98
NONVOLATILE STORAGE DEVICE REFRESH TIME DETECTOR	Spansion LLC	08/801305 2/18/97	5,852,582 12/22/98
METHOD AND SYSTEM FOR PROVIDING A DOUBLE DIFFUSE IMPLANT JUNCTION IN A FLASH DEVICE	Spansion LLC	08/658038 6/4/96	5,854,108 12/29/98
MEMORY CELL PROGRAMMING WITH CONTROLLED CURRENT INJECTION	Spansion LLC	08/831571 4/9/97	5,856,946 1/5/99
PROGRAMMING OF MEMORY CELLS USING CONNECTED FLOATING GATE ANALOG REFERENCE CELL	Spansion LLC	08/991466 12/16/97	5,859,796 1/12/99
BANK ARCHITECTURE FOR A NONVOLATILE MEMORY ENABLING SIMULTANEOUS READING AND WRITING	Spansion LLC	08/772,131 12/20/1996	5,867,430 2/2/1999
SELECTIVELY OXIDIZED FIELD OXIDE REGION	Spansion LLC	08/569704 12/8/95	5,869,385 2/9/99
METHOD OF SCREENING MEMORY CELLS AT ROOM TEMPERATURE THAT WOULD BE REJECTED DURING HOT TEMPERATURE PROGRAMMING TESTS	Spansion LLC	08/653211 5/24/96	5,870,407 2/9/99

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METHOD FOR PROGRAMMING FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READONLY MEMORY	Spansion LLC	09/085705 5/27/98	5,875,130 2/23/99
MEMORY BLOCK SELECT USING MULTIPLE WORD LINES TO ADDRESS A SINGLE MEMORY CELL ROW	Spansion LLC	08/938048 9/26/97	5,883,826 3/16/99
SELECTIVE BIT LINE RECOVERY IN A MEMORY ARRAY	Spansion LLC	08/938292 9/26/97	5,883,841 3/16/99
NONUNIFORM THRESHOLD VOLTAGE ADJUSTMENT IN FLASH EPROMS THROUGH GATE WORK FUNCTION ALTERATION	Spansion LLC	09/023241 2/13/98	5,888,867 3/30/99
MEMORY CELL FABRICATION EMPLOYING AN INTERPOLY GATE DIELECTRIC ARRANGED UPON A POLISHED FLOATING GATE	Spansion LLC	08/955794 10/22/97	5,888,870 3/30/99
MULTILAYER FLOATING GATE FIELD EFFECT TRANSISTOR STRUCTURE FOR USE IN INTEGRATED CIRCUIT DEVICES	Spansion LLC	08/837556 4/21/97	5,889,302 3/30/99
MEMORY CELL FOR STORING AT LEAST THREE LOGIC STATES	Spansion LLC	08/947123 10/8/97	5,889,697 3/30/99
SIMPLIFIED FILE MANAGEMENT SCHEME FOR FLASH MEMORY	Spansion LLC	08/651261 5/23/96	5,896,393 4/20/99
METHOD FOR ERASING FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READONLY MEMORY (EEPROM)	Spansion LLC	09/085552 5/27/98	5,901,090 5/4/99
METHOD TO IMPROVE TESTING SPEED OF MEMORY	Spansion LLC	08/992077 12/17/97	5,907,561 5/25/99
HIGH VOLTAGE NMOS PASS GATE HAVING SUPPLY RANGE, AREA, AND SPEED ADVANTAGES	Spansion LLC	09/127991 8/3/98	5,909,396 6/1/99
A DUAL SOURCE SIDE POLYSILICON SELECT GATE STRUCTURE UTILIZING SINGLE TUNNEL OXIDE FOR NAND ARRAY FLASH MEMORY	Spansion LLC	08/940,674 9/30/1997	5,912,489 6/15/1999

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DOUBLE DENSITY V NONVOLATILE MEMORY CELL	Spansion LLC	09/026358 2/19/98	5,923,063 7/13/99
PAGE BUFFER FOR A MULTILEVEL FLASH MEMORY WITH A LIMITED NUMBER OF LATCHES PER MEMORY CELL	Spansion LLC	09/103041 6/23/98	5,930,172 7/27/99
REDUCTION OF ONO FENCE DURING SELFALIGNED ETCH TO ELIMINATE POLY STRINGERS	Spansion LLC	08/986953 12/8/97	5,933,729 8/3/99
METHOD OF SPACER FORMATION AND SOURCE PROTECTION AFTER SELF ALIGNED SOURCE IS FORMED AND DEVICE PROVIDED BY SUCH A METHOD	Spansion LLC	08/813562 3/7/97	5,933,730 8/3/99
AN IMPROVED ULTRATHIN OXYNITRIDE STRUCTURE AND PROCESS FOR VLSI APPLICTIONS	Spansion LLC	08/708428 9/5/96	5,939,763 8/17/99
METHOD AND SYSTEM FOR SOURCE ONLY REOXIDATION AFTER JUNCTION IMPLANT FOR FLASH MEMORY DEVICES	Spansion LLC	08/993599 12/18/97	5,940,709 8/17/99
REDUCTION OF CHARGE LOSS IN NONVOLATILE MEMORY CELLS BY PHOSPHORUS IMPLANTATION INTO PECVD NITRIDE/OXYNITRIDE FILMS	Spansion LLC	08/917149 8/25/97	5,940,735 8/17/99
THREEDIMENSIONAL NONVOLATILE MEMORY	Spansion LLC	08/510118 8/1/95	5,945,705 8/31/99
METHOD OF SOFTLANDING GATE ETCHING TO PREVENT GATE OXIDE DAMAGE	Spansion LLC	09/092924 6/8/98	5,948,703 9/7/99
METHOD AND SYSTEM FOR SELECTED SOURCE DURING READ AND PROGRAMMING OF FLASH MEMORY	Spansion LLC	08/992622 12/17/97	5,949,718 9/7/99
METHOD OF FABRICATING AN EPROM TYPE DEVICE WITH REDUCED PROCESS RESIDUES	Spansion Inc.	08/878,119 6/18/1997	5,950,086 9/7/1999
SUPPLY VOLTAGEINDEPENDENT REFERENCE VOLTAGE CIRCUIT	Spansion LLC	08/265583 6/23/94	5,955,874 9/21/99

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METHOD OF MAKING A SEMICONDUCTOR DEVICE WITH ADJUSTABLE THRESHOLD VOLTAGE	Spansion LLC	08/891422 7/9/97	5,963,824 10/5/99
NOVEL PROCESSING TECHNIQUES FOR ACHIEVING PRODUCTIONWORTHY, LOW DIELECTRIC, LOW INTERCONNECT RESISTANCE AND HIGH PERFORMANCE ICS	Spansion LLC	08/681141 7/22/96	5,965,934 10/12/99
METHOD FOR PREVENTING P1 PUNCHTHROUGH	Spansion LLC	09/002783 1/5/98	5,972,749 10/26/99
METHODS AND ARRANGEMENTS FOR INTRODUCING NITROGEN INTO A TUNNEL OXIDE IN A NONVOLATILE SEMICONDUCTOR MEMORY DEVICE	Spansion LLC	09/143090 8/28/98	5,972,751 10/26/99
METHODS AND ARRANGEMENTS FOR FORMING A TAPERED FLOATING GATE IN NONVOLATILE MEMORY SEMICONDUCTOR DEVICES	Spansion LLC	08/992951 12/18/97	5,973,353 10/26/99
INTERLACED STORAGE AND SENSE TECHNIQUE FOR FLASH MULTILEVEL DEVICES	Spansion LLC	09/103046 6/23/98	5,973,958 10/26/99
LOW SUPPLY VOLTAGE NEGATIVE CHARGE PUMP	Spansion LLC	08/774307 12/26/96	5,973,979 10/26/99
METHOD FOR ETCHING MEMORY GATE STACK USING THIN RESIST LAYER	Spansion LLC	09/118377 7/17/98	5,977,601 11/2/99
BIT LINE BIASING METHOD TO ELIMATE PROGRAM DISTURBANCE IN A NONVOLATILE MEMORY DEVICE AND MEMORY DEVICE EMPLOYING THE SAME	Spansion LLC	09/175,647 10/20/1998	5,978,267 11/2/1999
TUBE FOR FLASH MINIATURE CARD	Spansion LLC	08/870045 6/5/97	5,979,660 11/9/99

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NARROWER ERASE DISTRIBUTION FOR FLASH MEMORY BY SMALLER POLY GRAIN SIZE	Spansion LLC	09/045013 3/20/98	5,981,339 11/9/99
SIDEWALL SPACER FOR PROTECTING TUNNEL OXIDE DURING ISOLATION TRENCH FORMATION IN SELFALIGNED FLASH MEMORY CORE	Spansion LLC	08/986160 12/5/97	5,981,341 11/9/99
METHOD OF FORMING A SILICON GATE TO PRODUCE SILICON DEVICES WITH IMPROVED PERFORMANCE	Spansion LLC	08/568195 12/6/95	5,981,364 11/9/99
TRENCHED GATE NONVOLATILE SEMICONDUCTOR DEVICE AND METHOD WITH CORNER DOPING AND SIDEWALL DOPING	Spansion LLC	09/052062 3/30/98	5,990,515 11/23/99
METHOD FOR REDUCING PROGRAM DISTURB DURING SELFBOOSTING IN A NAND FLASH MEMORY	Spansion LLC	09/161423 9/24/98	5,991,202 11/23/99
MANUFACTURING PROCESS TO ELIMINATE POLYSTRINGERS IN HIGH DENSITY NANDTYPE FLASH MEMORY DEVICES	Spansion LLC	08/993343 12/18/97	5,994,239 11/30/99
SEMICONDUCTOR DEVICE WITH MULTIPLE CONTACT SIZES	Spansion LLC	08/991052 12/16/97	5,994,780 11/30/99
SCHEME FOR PAGE ERASE AND ERASE VERIFY IN A NON VOLATILE MEMORY ARRAY	Spansion LLC	09/175,646 10/20/1998	5,995,417 11/30/1999
DUAL SOURCE SIDE POLYSILICON SELECT GATE STRUCTURE AND PROGRAMMING METHOD UTILIZING SINGLE TUNNEL OXIDE FOR NAND ARRAY FLASH MEMORY	Spansion LLC	09/063,688 4/21/1998	5,999,452 12/7/1999
BIOS MEMORY AND MULTIMEDIA DATA STORAGE COMBINATION	Spansion LLC	08/976303 11/21/97	5,999,476 12/7/99

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
METHOD OF ELIMINATING POLY STRINGER IN A MEMORY DEVICE	Spansion LLC	08/986860 12/8/97	6,001,688 12/14/99
PROCESS FOR FABRICATING A FLASH MEMORY WITH DUAL FUNCTION CONTROL LINES	Spansion LLC	09/008415 1/16/98	6,001,689 12/14/99
METHODS FOR FORMING NITROGENRICH REGIONS IN A FLOATING GATE AND INTERPOLY DIELECTRIC LAYER IN A NONVOLATILE SEMICONDUCTOR MEMORY DEVICE	Spansion LLC	09/154074 9/16/98	6,001,713 12/14/99
NON VOLATILE TRENCH SEMICONDUCTOR DEVICE	Spansion LLC	08/993890 12/18/97	6,002,151 12/14/99
SEMICONDUCTOR ISOLATION PROCESS TO MINIMIZE WEAK OXIDE PROBLEMS	Spansion LLC	08/989820 12/12/97	6,002,160 12/14/99
MEMORY ADDRESS DECODING CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE	Spansion LLC	09/159,342 9/23/1998	6,005,803 12/21/1999
SPLIT VOLTAGE FOR NAND FLASH	Spansion LLC	08/993634 12/18/97	6,005,804 12/21/99
METAL OXIDE STACK FOR FLASH MEMORY APPLICATION	Spansion LLC	09/154073 9/16/98	6,011,289 1/4/00
METHOD FOR SENSING STATE OF ERASURE OF A FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READONLY MEMORY (EEPROM)	Spansion LLC	09/132347 8/12/98	6,011,721 1/4/00
METHOD AND SYSTEM FOR GATE STACK REOXIDATION CONTROL	Spansion LLC	08/993787 12/19/97	6,015,736 1/18/00
METHOD FOR FORMING A LOW BARRIER HEIGHT OXIDE LAYER ON A SILICON SUBSTRATE	Spansion LLC	08/982186 12/17/97	6,017,786 1/25/00

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METHOD OF FABRICATING A HIGH DIELECTRIC CONSTANT INTERPOLYSILICON DIELECTRIC STRUCTURE FOR A LOW VOLTAGE NONVOLATILE MEMORY	Spansion LLC	08/978107 11/25/97	6,020,238 2/1/00
METHOD OF FABRICATING AN OXYNITRIDECAPPED HIGH DIELECTRIC CONSTANT INTERPOLYSILICON DIELECTRIC STRUCTURE FOR A LOW VOLTAGE NONVOLATILE MEMORY	Spansion LLC	08/978398 11/25/97	6,025,228 2/15/00
METHOD AND SYSTEM FOR USING A SPACER TO OFFSET IMPLANT DAMAGE AND REDUCE LATERAL DIFFUSION IN FLASH MEMORY DEVICES	Spansion LLC	08/993600 12/18/97	6,025,240 2/15/00
METHOD FOR FULLY PLANARIZED CONDUCTIVE LINE FOR A STACK GATE	Spansion LLC	08/992536 12/17/97	6,027,998 2/22/00
ELIMINATION OF OXYNITRIDE (ONO) ETCH RESIDUE AND POLYSILICON STRINGERS THROUGH ISOLATION OF FLOATING GATES ON ADJACENT BITLINES BY POLYSILICON OXIDATION	Spansion LLC	09/033916 3/3/98	6,030,868 2/29/00
METHOD OF MAKING FLEXIBLY PARTITIONED METAL LINE SEGMENTS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE	Spansion LLC	09/159,023 9/23/1998	6,033,955 3/7/2000
METHODS AND ARRANGEMENTS FOR FORMING A FLOATING GATE IN NONVOLATILE MEMORY SEMICONDUCTOR DEVICES	Spansion LLC	08/992950 12/18/97	6,034,394 3/7/00
A SEMICONDUCTOR DEVICE HAVING A REDUCED HEIGHT FLOATING GATE	Spansion LLC	09/092352 6/5/98	6,034,395 3/7/00

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ELIMINATION OF OXYNITRIDE (ONO) ETCH RESIDUE AND POLYSILICON STRINGERS THROUGH ISOLATION OF FLOATING GATES ON ADJACENT BITLINES BY POLYSILICON OXIDATION	Spansion LLC	09/033723 3/3/98	6,043,120 3/28/00
THREEDIMENSIONAL NONVOLATILE MEMORY	Spansion LLC	09/334393 6/16/99	6,043,122 3/28/00
ELIMINATION OF POLY STRINGERS WITH STRAIGHT POLY PROFILE	Spansion LLC	08/986951 12/8/97	6,046,085 4/4/00
CIRCUIT IMPLEMENTATION TO QUENCH BIT LINE LEAKAGE CURRENT IN PROGRAMMING AND OVERERASE CORRECTION MODES IN FLASH EEPROM	Spansion LLC	09/417273 10/13/99	6,046,932 4/4/00
FLASH MEMORY DEVICE HAVING HIGH PERMITTIVITY STACKED DIELECTRIC AND FABRICATION THEREOF	Spansion LLC	09/172410 10/14/98	6,048,766 4/11/00
OPERATIONAL APPROACH FOR THE SUPPRESSION OF BIDIRECTIONAL TUNNEL OXIDE STRESS OF A FLASH CELL	Spansion LLC	09/404080 9/23/99	6,049,479 4/11/00
METHOD FOR TIGHTENING ERASE THRESHOLD VOLTAGE DISTRIBUTION IN FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READONLY MEMORY (EEPROM)	Spansion LLC	09/132981 8/12/98	6,052,310 4/18/00
ELIMINATION OF POLY CAP FOR EASY POLY1 CONTACT FOR NAND PRODUCT	Spansion Technology Inc.	09/061,515 4/16/1998	6,057,193 5/2/2000
STACKED GATE STRUCTURE FOR FLASH MEMORY APPLICATION	Spansion LLC	09/154072 9/16/98	6,060,741 5/9/00
METHODS FOR FORMING A CONTROL GATE APPARATUS IN NONVOLATILE MEMORY SEMICONDUCTOR DEVICES	Spansion LLC	08/993409 12/18/97	6,063,662 5/16/00

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RTCVD OXIDE AND N2O ANNEAL FOR TOP OXIDE OF ONO FILM	Spansion LLC	09/098292 6/16/98	6,063,666 5/16/00
METHOD AND APPARATUS FOR PREVENTING P1 PUNCHTHROUGH	Spansion LLC	09/271330 3/18/99	6,066,873 5/23/00
INTERLEVEL DIELECTRIC THICKNESS MONITOR FOR COMPLEX SEMICONDUCTOR CHIPS	Spansion LLC	08/991299 12/16/97	6,072,191 6/6/00
LPCVD OXIDE AND RTA FOR TOP OXIDE OF ONO FILM TO IMPROVE RELIABILITY FOR FLASH MEMORY DEVICES	Spansion LLC	09/189227 11/11/98	6,074,917 6/13/00
METHODS FOR PREVENTING SILICIDE RESIDUE FORMATION IN A SEMICONDUCTOR DEVICE	Spansion LLC	09/076663 5/12/98	6,074,956 6/13/00
SEMICONDUCTOR DEVICE CONTAINING PHDP INTERDIELECTRIC LAYER	Spansion LLC	09/199265 11/25/98	6,080,639 6/27/00
METHODOLOGY FOR ACHIEVING DUAL GATE OXIDE THICKNESSES	Spansion LLC	08/993716 12/18/97	6,080,682 6/27/00
EEPROM DECODER BLOCK HAVING A PWELL COUPLED TO A CHARGE PUMP FOR CHARGING THE PWELL AND METHOD OF PROGRAMMING WITH THE EEPROM DECODER BLOCK	Spansion LLC	09/232023 1/14/99	6,081,455 6/27/00
FLASH MEMORY ARCHITECTURE EMPLOYING THREE LAYER METAL INTERCONNECT FOR WORD LINE DECODING	Spansion LLC	09/379479 8/23/99	6,088,287 7/11/00
MULTICHIP PACKAGING USING BUMP TECHNOLOGY	Spansion LLC	09/032398 2/27/98	6,091,138 7/18/00
PROGRAM/VERIFY TECHNIQUE FOR MULTILEVEL FLASH CELLS ENABLING DIFFERENT THRESHOLD LEVELS TO BE SIMULTANEOUSLY PROGRAMMED	Spansion LLC	09/108529 7/1/98	6,091,631 7/18/00

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MULTIPURPOSE GRADED SILICON OXYNITRIDE CAP LAYER	Spansion LLC	09/134525 8/14/98	6,100,559 8/8/00
MULTIPLE CHIP HYBRID PACKAGE USING BUMP TECHNOLOGY	Spansion LLC	09/032362 2/27/98	6,100,593 8/8/00
VT REFERENCE VOLTAGE FOR EXTREMELY LOW POWER SUPPLY	Spansion LLC	09/128,024 8/3/1998	6,100,754 8/8/2000
METHOD AND SYSTEM FOR PROVIDING A DRAIN SIDE POCKET IMPLANT	Spansion LLC	08/992618 12/17/97	6,103,602 8/15/00
METHOD FOR FABRICATING A DOPED POLYSILICON FEATURE IN A SEMICONDUCTOR DEVICE	Spansion LLC	09/134526 8/14/98	6,107,169 8/22/00
METHOD AND STRUCTURE OF ETCHING A MEMORY CELL POLISILICON GATE LAYER USING RESIST MASK AND ETCHED SILICON OXYNITRIDE	Spansion LLC	09/118382 7/17/98	6,110,779 8/29/00
ELIMINATION OF OXYNITRIDE (ONO) ETCH RESIDUE AND POLYSILICON STRI NGERS THROUGH ISOLATION OF FLOATING GATES ON ADJACENT BITLINES BY POLYSILICON OXIDATION	Spansion LLC	09/033836 3/3/98	6,110,833 8/29/00
ADDRESS TRANSISTION DETECT TIMING ARCHITECTURE FOR A SIMULTANEOUS OPERATION FLASH MEMORY	Spansion LLC	09/421,776 10/19/1999	6,111,787 8/29/2000
NITROGEN ION IMPLANTED AMORPHOUS SILICON TO PRODUCE OXIDATION RESISTANT AND FINER GRAIN POLYSILICON BASED FLOATING GATES	Spansion LLC	08/993443 12/18/97	6,114,230 9/5/00
INTEGRATED METHOD BY USING HIGH TEMPERATURE OXIDE FOR TOP OXIDE AND PERIPHERY GATE OXIDE	Spansion LLC	09/427,402 10/25/1999	6,117,730 9/12/2000

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
DOUBLE DENSITY NONVOLATILE MEMEORY CELLS	Spansion LLC	09/110446 7/7/98	6,118,147 9/12/00
DISTRIBUTING CFI DEVICES IN EXISTING DECODERS	Spansion LLC	09/417731 10/14/99	6,118,694 9/12/00
OUTPUT MULTIPLEXING IMPLEMENTATION FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	Spansion LLC	09/422,199 10/19/1999	6,118,698 9/12/2000
SOURCE BIAS COMPENSATION FOR PAGE MODE READ OPERATION IN A FLASH MEMORY DEVICE	Spansion LLC	09/421151 10/19/99	6,118,702 9/12/00
BIT BY BIT APDE VERIFY FOR FLASH MEMORY APPLICATIONS	Spansion LLC	09/413182 10/5/99	6,122,198 9/19/00
NONVOLATILE TRENCH SEMICONDUCTOR DEVICE HAVING A SHALLOW DRAIN REGION	Spansion LLC	08/992961 12/18/97	6,124,608 9/26/00
SCALABLE AND RELIABLE INTEGRATED CIRCUIT INTERLEVEL DIELECTRIC	Spansion LLC	09/144506 8/31/98	6,124,640 9/26/00
SECTOR WRITE PROTECT CAMS FOR A SIMULTANEOUS OPERATION FLASH MEMORY	Spansion LLC	09/421,105 10/19/1999	6,125,055 9/26/2000
NONSELFALIGNED SIDE CHANNEL IMPLANTS FOR FLASH MEMORY CELLS	Spansion LLC	08/991687 12/16/97	6,127,222 10/3/00
REDUCTION OF SILICON OXYNITRIDE FILM DELAMINATION IN INTEGRATED CIRCUIT INTERLEVEL DIELECTRICS	Spansion LLC	09/144521 8/31/98	6,133,619 10/17/00
WORDLINE DRIVER FOR FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READONLY MEMORY (EEPROM)	Spansion LLC	09/166,385 10/5/1998	6,134,146 10/17/2000
METHOD FOR REMOVING ANTIREFLECTIVE COATING LAYER USING PLASMA ETCH PROCESS AFTER CONTACT CMP	Spansion LLC	09/416389 10/12/99	6,136,649 10/24/00

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FLOATING GATE CAPACITOR FOR USE IN VOLTAGE REGULATORS	Spansion LLC	09/023497 2/13/98	6,137,153 10/24/00
REDUCTION OF OXIDE STRESS THROUGH THE USE OF FORWARD BIASED BODY VOLTAGE	Spansion LLC	09/490353 1/24/00	6,137,727 10/24/00
IN SITU P DOPED AMORPHOUS SILICON BY NH3 TO FORM OXIDATION RESISTANT AND FINER GRAIN FLOATING GATES	Spansion LLC	08/993444 12/18/97	6,140,246 10/31/00
MULTI LEVEL SENSING OF NAND MEMORY CELLS BY EXTERNAL BIAS CURRENT	Spansion LLC	09/388696 9/2/99	6,141,244 10/31/00
1 TRANSISTOR CELL FOR EEPROM APPLICATION	Spansion LLC	09/389161 9/2/99	6,141,255 10/31/00
BARRIER LAYER DECREASES NITROGEN CONTAMINATION OF PERIPHERAL GATE REGIONS DURING TUNNEL OXIDE NITRIDATION	Spansion LLC	09/283,308 3/31/1999	6,143,608 11/7/2000
METHOD AND SYSTEM FOR BIDIRECTIONAL VOLTAGE REGULATION DETECTION	Spansion LLC	09/417732 10/14/99	6,144,606 11/7/00
METHOD FOR MANUFACTURING MEMORY DEVICES	Spansion LLC	09/146032 9/2/98	6,146,795 11/14/00
LARGE ANGLE IMPLANTATION TO PREVENT FIELD TURNON UNDER SELECT GATE TRANSISTOR FIELD OXIDE REGION FOR NONVOLATILE MEMORY DEVICES	Spansion LLC	09/039783 3/16/98	6,146,944 11/14/00
FULLY RECESSED SEMICONDUCTOR DEVICE	Spansion LLC	09/052061 3/30/98	6,147,377 11/14/00
FULLY RECESSED SEMICONDUCTOR DEVICE AND METHOD FOR LOW POWER APPLICATIONS WITH SINGLE WRAP AROUND BURIED DRAIN REGION	Spansion LLC	09/052060 3/30/98	6,147,378 11/14/00
METHOD AND SYSTEM FOR SAVING OVERHEAD PROGRAM TIME IN A MEMORY DEVICE	Spansion LLC	09/419,695 10/14/1999	6,147,906 11/14/2000

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
BIASING SCHEME TO REDUCE STRESS ON NONSELECTED CELLS DURING READ	Spansion LLC	09/430336 10/29/99	6,147,907 11/14/00
METHOD FOR SIMULTANEOUS DEPOSITION AND SPUTTERING OF TEOS	Spansion LLC	09/099057 6/17/98	6,150,285 11/21/00
FLOATING GATE ENGINEERING TO IMPROVE TUNNEL OXIDE RELIABILITY FOR FLASH MEMORY DEVICES	Spansion LLC	09/374059 8/12/99	6,153,470 11/28/00
NEW APPROACH FOR THE FORMATION OF SEMICONDUCTOR DEVICES WHICH REDUCES BANDTOBAND TUNNELING CURRENT AND SHORTCHANNEL EFFECTS	Spansion LLC	09/040107 3/17/98	6,153,487 11/28/00
METHOD FOR ERASING FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READONLY MEMORY(EEPROM)	Spansion LLC	09/085680 5/27/98	6,157,572 12/5/00
METHODS FOR REMOVING SILICIDE RESIDUE IN A SEMICONDUCTOR DEVICE	Spansion LLC	09/076662 5/12/98	6,159,794 12/12/00
LOW VOLTAGE JUNCTION AND HIGH VOLTAGE JUNCTION OPTIMIZATION FOR FLASH MEMORY	Spansion LLC	09/109,664 7/2/1998	6,159,795 12/12/2000
METHOD FOR ETCHING LAYERS ON A SEMICONDUCTOR WAFER IN A SINGLE ETCHING CHAMBER	Spansion LLC	09/118375 7/17/98	6,159,860 12/12/00
METHOD OF SPACER FORMATION AND SOURCE PROTECTION AFTER SELFALIGNED SOURCE FORMED AND A DEVICE PROVIDED BY SUCH A METHOD	Spansion LLC	09/336057 6/18/99	6,160,317 12/12/00
METHOD TO PROVIDE A REDUCED CONSTANT EFIELD DURING ERASE OF EEPROMS FOR RELIABILITY IMPROVEMENT	Spansion LLC	09/490351 1/24/00	6,160,740 12/12/00

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
NOISE REDUCTION DURING SIMULTANEOUS OPERATION OF A FLASH MEMORY DEVICE	Spansion LLC	09/498205 2/4/00	6,160,750 12/12/00
AMMONIA ANNEALED AND WET OXIDIZED LPCVD OXIDE TO REPLACE ONO FILMS FOR HIGH INTEGRATED FLASH MEMORY DEVICES	Spansion LLC	09/266714 3/11/99	6,162,684 12/19/00
METHOD OF FORMING A COMPOSITE INTERPOLY GATE DIELECTRIC	Spansion LLC	09/170061 10/13/98	6,163,049 12/19/00
COMMON FLASH INTERFACE IMPLEMENTATION FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	Spansion LLC	09/421,774 10/19/1999	6,163,478 12/19/2000
FLASH MEMORY WORDLINE TRACKING ACROSS WHOLE CHIP	Spansion LLC	09/431,296 10/29/1999	6,163,481 12/19/2000
A LOW DIELECTRIC CONSTANT MATERIAL AND METHOD OF APPLICATION TO ISOLATE CONDUCTIVE LINES	Spansion LLC	09/000739 12/30/97	6,166,439 12/26/00
MULTI STATE SENSING OF NAND MEMORY CELLS BY APPLYING REVERSEBIAS VOLTAGE	Spansion LLC	09/370010 8/6/99	6,166,951 12/26/00
PROCESS FOR FABRICATING A SEMICONDUCTOR DEVICE HAVING A GRADED JUNCTION	Spansion LLC	09/487922 1/19/00	6,168,993 1/2/01
RAMPED GATE TECHNIQUE FOR SOFT PROGRAMMING TO TIGHTEN THE VT DISTRIBUTION	Spansion LLC	09/370380 8/9/99	6,172,909 1/9/01
CONCURRENT ERASE VERIFY SCHEME FOR FLASH MEMORY APPLICATIONS	Spansion LLC	09/404078 9/23/99	6,172,914 1/9/01
LOW TEMPERATURE PHOTORESIST REMOVAL FOR REWORK DURING METAL MASK FORMATION	Spansion LLC	09/119777 7/21/98	6,174,819 1/16/01

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READ OPERATION SCHEME FOR A HIGHDENSITY, LOW VOLTAGE, AND SUPERIOR RELIABILITY NAND FLASH MEMORY DEVICE	Spansion LLC	09/408846 9/30/99	6,175,522 1/16/01
PRECHARGING MECHANISM AND METHOD FOR NANDBASED FLASH MEMORY DEVICES	Spansion LLC	09/433187 10/25/99	6,175,523 1/16/01
POST BARRIER METAL CONTACT IMPLANTATION TO MINIMIZE OUT DIFFUSION FOR NAND DEVICE	Spansion LLC	09/412278 10/5/99	6,177,316 1/23/01
HIGH VOLTAGE TRANSISTOR WITH HIGH GATED DIODE BREAKDOWN VOLTAGE	Spansion LLC	09/177817 10/23/98	6,177,322 1/23/01
BACKGROUND CORRECTION FOR CHARGE GAIN AND LOSS	Spansion LLC	09/490352 1/24/00	6,178,117 1/23/01
SEPARATE OUTPUT POWER SUPPLY TO REDUCE OUTPUT NOISE FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	Spansion LLC	09/421762 10/19/99	6,178,129 1/23/01
METHOD FOR FORMING FLASH MEMORY DEVICES	Spansion LLC	09/430765 10/29/99	6,180,454 1/30/01
PROCESS FOR FABRICATING AN ONO FLOATINGGATE ELECTRODE IN A TWOBIT EEPROM DEVICE USING RAPIDTHERMALCHEMICALVAP ORDEPOSITION	Spansion LLC	09/426240 10/25/99	6,180,538 1/30/01
GLOBAL ERASE/PROGRAM VERIFICATION APPARATUS AND METHOD	Spansion LLC	09/414750 10/6/99	6,181,605 1/30/01
METHOD TO ELIMATE SILICIDE CRACKING FOR NAND TYPE FLASH MEMORY DEVICES BY IMPLANTING A POLISH RATE IMPROVER INTO THE SECOND POLYSILICON LAYER AND POLISHING IT	Spansion LLC	09/263701 3/5/99	6,184,084 2/6/01

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
REFERENCE CELL FOURWAY SWITCH FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	Spansion LLC	09/421,984 10/19/1999	6,185,128 2/6/2001
PROGRAMMABLE CURRENT SOURCE	Spansion LLC	09/420209 10/18/99	6,185,130 2/6/01
DEVICE INITIALIZING SYSTEM WITH PROGRAMMABLE ARRAY LOGIC CONFIGURED TO CAUSE NONVOLATILE MEMORY TO OUTPUT ADDRESS AND DATA INFORMATION TO THE DEVICE IN A PRESCRIBED SEQUENCE	Spansion LLC	08/993062 12/18/97	6,185,630 2/6/01
METHOD AND APPARATUS FOR CONTROLLING THE THICKNESS OF A GATE OXIDE IN A SEMICONDUCTOR MANUFACTURING PROCESS	Spansion LLC	09/033642 3/3/98	6,187,092 2/13/01
FLASH EPROM CELL WITH REDUCED SHORT CHANNEL EFFECT AND METHOD FOR PROVIDING SAME	Spansion LLC	09/006757 1/14/98	6,188,101 2/13/01
MULTI STATE SENSING OF NAND MEMORY CELLS BY VARYING SOURCE BIAS	Spansion LLC	09/369600 8/6/99	6,188,606 2/13/01
RAMPED OR STEPPED GATE CHANNEL ERASE FOR FLASH MEMORY APPLICATION	Spansion LLC	09/307259 5/6/99	6,188,609 2/13/01
METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE WITH REDUCED MASKING AND WITHOUT ARC LOSS IN PERIPHERAL CIRCUITRY REGION	Spansion LLC	09/417130 10/13/99	6,197,635 3/6/01
APDE SCHEME FOR FLASH MEMORY APPLICATION	Spansion LLC	09/495215 1/31/00	6,198,664 3/6/01
METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE WITHOUT ARC LOSS IN PERIPHERAL CIRCUIT REGION	Spansion LLC	09/417132 10/13/99	6,200,857 3/13/01

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APPARATUS AND METHOD TO CHARACTERIZE THE THRESHOLD DISTRIBUTION IN AN NROM VIRTUAL GROUND ARRAY	Spansion LLC	09/558,764 4/26/2000	6,201,737 3/13/2001
METHOD AND APPARATUS FOR MEASURING SUBTHRESHOLD CURRENT IN A MEMORY ARRAY	Spansion LLC	09/409542 9/30/99	6,201,747 3/13/01
LATCHING CAM DATA IN A FLASH MEMORY DEVICE	Spansion LLC	09/421,142 10/19/1999	6,201,753 3/13/2001
METHOD OF FORMING SELECT GATE TO IMPROVE RELIABILITY AND PERFORMANCE FOR NAND TYPE FLASH MEMORY DEVICES	Spansion LLC	09/349603 7/9/99	6,204,159 3/20/01
DYNAMIC MEMORY CELL PROGRAMMING VOLTAGE	Spansion LLC	09/512854 2/25/00	6,205,055 3/20/01
SYSTEM AND METHOD FOR DETECTING FLASH MEMORY THRESHOLD VOLTAGES	Spansion LLC	09/504558 2/15/00	6,205,057 3/20/01
METHOD FOR ERASING FLASH ELECTRICALLY ERASABLE PROGRAMMABLE READONLY MEMORY (EEPROM)	Spansion LLC	09/166384 10/5/98	6,205,059 3/20/01
TEMPERATURECOMPENSATED BIAS GENERATOR	Spansion LLC	09/610764 7/6/00	6,205,074 3/20/01
METHOD OF USING SOURCE/DRAIN NITRIDE FOR PERIPHERY FIELD OXIDE AND BITLINE OXIDE	Spansion LLC	09/426255 10/25/99	6,207,502 3/27/01
FLASH MEMORY CELLS HAVING A MODULATION DOPED HETEROJUNCTION STRUCTURE	Spansion LLC	09/516472 3/1/00	6,207,978 3/27/01
ADDRESS TRANSITION DETECT TIMING ARCHITECTURE FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	Spansion LLC	09/547,556 4/12/2000	6,208,556 3/27/2001
METHOD TO REDUCE CAPACTIVE LOADING IN FLASH MEMORY XDECODER FOR ACCURATE VOLTAGE CONTROL AT WORDLINES AND SELECT LINES	Spansion LLC	09/593,303 6/13/2000	6,208,561 3/27/2001

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PROCESS FOR FABRICATING A COMMON SOURCE REGION IN MEMORY DEVICES	Spansion LLC	09/177294 10/22/98	6,211,020 4/3/01
SEMICONDUCTOR DEVICE WITH MULTIPLE CONTACT SIZES	Spansion LLC	09/353781 7/15/99	6,211,058 4/3/01
METHODS AND ARRANGEMENTS FOR REDUCING STRESS AND PREVENTING CRACKING IN A SILICIDE LAYER	Spansion LLC	09/076584 5/12/98	6,211,074 4/3/01
VOLTAGE PROTECTION OF WRITE PROTECT CAMS	Spansion LLC	09/602095 6/22/00	6,212,098 4/3/01
DISTRIBUTED VOLTAGE CHARGE CIRCUITS TO REDUCE SENSING TIME IN A MEMORY DEVICE	Spansion LLC	09/490,340 1/24/2000	6,212,108 4/3/2001
METHOD OF MAINTAINING CONSTANT ERASING SPEEDS FOR NONVOLATILE MEMORY CELLS	Spansion LLC	09/504696 2/16/00	6,215,702 4/10/01
SIMULTANEOUS PROGRAM, PROGRAMVERIFY SCHEME	Spansion LLC	09/501448 2/10/00	6,215,705 4/10/01
METHOD TO GENERATE A MONOS TYPE FLASH CELL USING POLYCRYSTALLINE SILICON AS AN ONO TOP LAYER	Spansion LLC	09/426,239 10/25/1999	6,218,227 4/17/2001
METHOD FOR FABRICATING A HIGHDENSITY AND HIGHRELIABILITY EEPROM DEVICE	Spansion LLC	09/198654 11/24/98	6,218,245 4/17/01
METHOD FOR PROVIDING A DOPANT LEVEL FOR POLYSILICON FOR FLASH MEMORY DEVICES	Spansion LLC	09/369638 8/6/99	6,218,689 4/17/01
MULTILEVEL CELL PROGRAMMING	Spansion LLC	09/513643 2/25/00	6,219,276 4/17/01
USE OF IMPLANTED IONS TO REDUCE OXIDENITRIDEOXIDE (ONO) ETCH RESIDUE AND POLYSTRINGERS	Spansion LLC	09/257733 2/25/99	6,221,768 4/24/01

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AUTO ADJUSTING WINDOW PLACEMENT SCHEME FOR AN NROM VIRTUAL GROUND ARRAY	Spansion LLC	09/557832 4/26/00	6,222,768 4/24/01
FULLY RECESSED SEMICONDUCTOR METHOD FOR LOW POWER APPLICATIONS WITH SINGLE WRAP AROUND BURIED DRAIN REGION	Spansion LLC	09/470568 12/22/99	6,225,161 5/1/01
INTEGRATED CIRCUIT INCORPORATING A MEMORY CELL AND A TRANSISTOR ELEVATED ABOVE AN INSULATING BASE	Spansion LLC	09/483557 1/14/00	6,225,646 5/1/01
TRENCHED GATE SEMICONDUCTOR DEVICE AND METHOD FOR LOW POWER APPLICATIONS	Spansion LLC	09/052058 3/30/98	6,225,659 5/1/01
HIGH SPEED, HIGH PRECISION, POWER SUPPLY AND PROCESS INDEPENDENT BOOST LEVEL CLAMPING TECHNIQUE	Spansion LLC	09/512617 2/25/00	6,225,849 5/1/01
METHODOLOGY FOR ACHIEVING DUAL FIELD OXIDE THICKNESSES	Spansion LLC	08/993149 12/18/97	6,228,746 5/8/01
CORE FIELD ISOLATION FOR A NAND FLASH MEMORY	Spansion LLC	09/309,994 5/11/1999	6,228,782 5/8/2001
BURST READ MODE WORD LINE BOOSTING	Spansion LLC	09/638,055 8/11/2000	6,229,735 5/8/2001
METHODOLOGY FOR ACHIEVING DUAL GATE OXIDE THICKNESSES	Spansion LLC	09/562442 5/1/00	6,232,244 5/15/01
LIGHT FLOATING GATE DOPING TO IMPROVE TUNNEL OXIDE RELIABILITY	Spansion LLC	09/348583 7/7/99	6,232,630 5/15/01
DOUBLE DENSITY NONVOLATILE MEMORY CELLS	Spansion LLC	09/436503 11/9/99	6,232,632 5/15/01
NEW METHOD TO FABRICATE A HIGH COUPLING FLASH CELL WITH LESS SILICIDE SEAM PROBLEM	Spansion LLC	09/543991 4/6/00	6,232,635 5/15/01

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
SHALLOW TRENCH ISOLATION FILLED WITH THERMAL OXIDE	Spansion Technology Inc.	09/082,607 5/20/1998	6,232,646 5/15/2001
SELFLIMITING MULTILEVEL PROGRAMMING STATES	Spansion LLC	09/693650 10/21/00	6,233,175 5/15/01
METHOD AND SYSTEM FOR REDUCING SHORT CHANNEL EFFECTS IN A MEMORY DEVICE	Spansion LLC	09/412544 10/5/99	6,235,584 5/22/01
THIN FLOATING GATE AND CONDUCTIVE SELECT GATE IN SITU DOPED AMORPHOUS SILICON MATERIAL FOR NAND TYPE FLASH MEMORY DEVICE APPLICATIONS	Spansion LLC	09/352801 7/13/99	6,235,586 5/22/01
METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE WITH REDUCED ARC LOSS IN PERIPHERAL CIRCUITRY REGION	Spansion LLC	09/417131 10/13/99	6,235,587 5/22/01
TRUNGSTEN PLUG FORMATION	Spansion LLC	09/006495 1/13/98	6,235,632 5/22/01
BIASING METHOD AND STRUCTURE FOR REDUCING BANDTOBAND AND/OR AVALANCHE CURRENTS DURING THE ERASE OF FLASH MEMORY DEVICES	Spansion LLC	09/461376 12/15/99	6,236,596 5/22/01
HIGH SPEED CHARGING OF CORE CELL DRAIN LINES IN A MEMORY DEVICE	Spansion LLC	09/489232 1/21/00	6,236,603 5/22/01
METHOD FOR IMPROVING ELECTROSTATIC DISCHARGE (ESD) ROBUSTNESS	Spansion LLC	09/199772 11/25/98	6,238,975 5/29/01
USE OF ETCH TO BLUNT GATE CORNERS	Spansion LLC	09/476584 1/3/00	6,238,978 5/29/01
METHOD TO REDUCE READ GATE DISTURB FOR FLASH EEPROM APPLICATION	Spansion LLC	09/495214 1/31/00	6,240,016 5/29/01

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
REDUCTION OF VOLTAGE STRESS ACROSS A GATE OXIDE AND ACROSS A JUNCTION WITHIN A HIGH VOLTAGE TRANSISTOR OF AN ERASABLE MEMORY DEVICE	Spansion LLC	09/353267 7/14/99	6,240,017 5/29/01
METHOD OF BITLINE SHIELDING IN CONJUNCTION WITH A PRECHARGING SCHEME FOR NANDBASED FLASH MEMORY DEVICES	Spansion LLC	09/427406 10/25/99	6,240,020 5/29/01
MULTIPLE BANK SIMULTANEOUS OPERATION FOR A FLASH MEMORY	Spansion LLC	09/526,239 3/15/2000	6,240,040 5/29/2001
PROCESS FOR FABRICATING A BITLINE USING BURIED DIFFUSION ISOLATION	Spansion LLC	09/427,404 10/25/1999	6,242,305 6/5/2001
DUAL BIT ISOLATION SCHEME FOR FLASH MEMORY DEVICES HAVING POLYSILICON FLOATING GATES	Spansion LLC	09/627565 7/28/00	6,242,306 6/5/01
SELFALIGNING POLY 1 ONO DIELECTRIC FOR NONVOLATILE MEMORY	Spansion LLC	09/163310 9/30/98	6,242,773 6/5/01
USING POLYSILICON FUSE FOR IC PROGRAMMING	Spansion LLC	09/385550 8/30/99	6,242,790 6/5/01
TWOSTAGE PIPELINE SENSING FOR PAGE MODE FLASH MEMORY	Spansion LLC	09/504186 2/15/00	6,243,291 6/5/01
SUBSTRATE HOLE INJECTION FOR NEUTRALIZING SPILLOVER CHARGE GENERATED DURING PROGRAMMING OF A NONVOLATILE MEMORY CELL	Spansion LLC	09/505259 2/16/00	6,243,300 6/5/01
VOLTAGE BOOST RESET CIRCUIT FOR A FLASH MEMORY	Spansion LLC	09/501,159 2/9/2000	6,243,316 6/5/2001
NOVEL PROCESS FOR RELIABLE ULTRATHIN OXYNITRIDE FORMATION	Spansion LLC	09/252854 9/8/98	6,245,689 6/12/01

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LOW DIELECTRIC SEMICONDUCTOR DEVICE WITH RIGID, CONDUCTIVELY LINED INTERCONNECTION SYSTEM	Spansion LLC	09/252185 2/18/99	6,246,118 6/12/01
SYMMETRICAL PROGRAM AND ERASE SCHEME TO IMPROVE ERASE TIME DEGRADATION IN NAND DEVICES	Spansion LLC	09/511652 2/22/00	6,246,610 6/12/01
SYSTEM FOR ERASING A MEMORY CELL	Spansion LLC	09/514560 2/28/00	6,246,611 6/12/01
METHOD FOR PROTECTING GATE EDGES FROM CHARGE GAIN/LOSS IN SEMICONDUCTOR DEVICE	Spansion LLC	09/376658 8/18/99	6,248,627 6/19/01
METHOD OF FABRICATING AN ONO DIELECTRIC BY NITRIDATION FOR MNOS MEMORY CELLS	Spansion LLC	09/426,430 10/25/1999	6,248,628 6/19/2001
PROCESS FOR FABRICATING A FLASH MEMORY DEVICE	Spansion LLC	09/040823 3/18/98	6,248,629 6/19/01
PROCESS FOR FABRICATING A BITLINE IN A MONOS DEVICE USING A DUAL LAYER HARD MASK	Spansion LLC	09/426,205 10/25/1999	6,248,635 6/19/2001
STEPPER ALIGNMENT MARK FORMATION WITH DUAL FIELD OXIDE PROCESS	Spansion TechnologyInc.	09/044,389 3/18/1998	6,249,036 6/19/2001
VIABLE MEMORY CELL FORMED USING RAPID THERMAL ANNEALING	Spansion LLC	09/163315 9/30/98	6,251,717 6/26/01
NONVOLATILE SEMICONDUCTOR MEMORY DEVICE INCLUDING ASSYMETRICALLY NITROGEN DOPED GATE OXIDE	Spansion LLC	09/377183 8/19/99	6,252,276 6/26/01
AUTOMATIC PROGRAM DISTURB WITH INTELLIGENT SOFT PROGRAMMING FOR FLASH CELLS	Spansion LLC	09/692881 10/23/00	6,252,803 6/26/01
NITRIDE PLUG TO REDUCE GATE EDGE LIFTING	Spansion LLC	09/420220 10/18/99	6,255,165 7/3/01

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
METHODS AND ARRANGEMENTS FOR IMPROVED FORMATION OF CONTROL AND FLOATING GATES IN NONVOLATILE MEMORY SEMICONDUCTOR DEVICES	Spansion LLC	08/992960 12/18/97	6,258,669 7/10/01
SENSE AMPLIFIER ARCHITECTURE FOR SLIDING BANKS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	Spansion LLC	09/422,198 10/19/1999	6,259,633 7/10/2001
MATCHING LOADING BETWEEN SENSING REFERENCE AND MEMORY CELL WITH REDUCED TRANSISTOR COUNT IN A DUALBANK FLASH MEMORY	Spansion LLC	09/557728 4/26/00	6,259,645 7/10/01
DUAL BIT ISOLATION SCHEME FOR FLASH DEVICES	Spansion LLC	09/596449 6/19/00	6,261,904 7/17/01
CAPACITOR FOR USE IN A CAPACITOR DIVIDER THAT HAS A FLOATING GATE TRANSISTOR AS A CORRESPONDING CAPACITOR	Spansion LLC	09/047237 3/25/98	6,262,469 7/17/01
HIGH TEMPERATURE OXIDE DEPOSITION PROCESS FOR FABRICATING AN ONO FLOATINGGATE ELECTRODE IN A TWO BIT EEPROM DEVICE	Spansion LLC	09/426,672 10/25/1999	6,265,268 7/24/2001
DUAL SOURCE SIDE POLYSILICON SELECT GATE STRUCTURE AND PROGRAMMING METHOD UTILIZING SINGLE TUNNEL OXIDE FOR NAND ARRAY FLASH MEMORY	Spansion LLC	09/410,512 9/30/1999	6,266,275 7/24/2001
METHOD OF ERASING NONVOLATILE MEMORY CELLS	Spansion LLC	09/504695 2/16/00	6,266,281 7/24/01
OUTPUT BUFFER FOR EXTERNAL VOLTAGE	Spansion LLC	09/661,356 9/14/2000	6,266,284 7/24/2001

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
METHOD FOR INHIBITING TUNNEL OXIDE GROWTH AT THE EDGES OF A FLOATING GATE DURING SEMICONDUCOR DEVICE PROCESSING	Spansion LLC	09/364982 7/31/99	6,268,624 7/31/01
METHOD OF PROGRAMMING A NONVOLATILE MEMORY CELL USING A CURRENT LIMITER	Spansion LLC	09/694729 10/23/00	6,269,023 7/31/01
MEMORY SYSTEM HAVING A PROGRAM AND ERASE VOLTAGE MODIFIER	Spansion LLC	09/500699 2/9/00	6,269,025 7/31/01
CHARGE SHARING TO HELP BOOST THE WORDLINES DURING APDE VERIFY	Spansion LLC	09/547747 4/12/00	6,269,026 7/31/01
METHOD FOR FORMING SELFALIGNED CONTACTS AND LOCAL INTERCONNECTS USING SELFALIGNED LOCAL INTERCONNECTS	Spansion LLC	09/685968 10/10/00	6,271,087 8/7/01
METHOD AND APPARATUS FOR CONTROLLING THE THICKNESS OF A GATE OXIDE IN A SEMICONDUCTOR MANUFACTURING PROCESS	Spansion LLC	08/885140 6/30/97	6,271,151 8/7/01
APPARATUS AND METHOD OF DIRECT CURRENT SENSING FROM SOURCE SIDE IN A VIRTUAL GROUND ARRAY	Spansion LLC	09/602328 6/23/00	6,272,043 8/7/01
METHODS AND ARRANGEMENTS FOR FORMING A FLOATING GATE IN NONVOLATILE MEMORY SEMICONDUCTOR DEVICES	Spansion LLC	09/476121 1/3/00	6,274,433 8/14/01
MULTIPLE BYTE CHANNEL HOT ELECTRON PROGRAMMING USING RAMPED GATE AND SOURCE BIAS VOLTAGE	Spansion LLC	09/416563 10/12/99	6,275,415 8/14/01
CHIP ENABLE INPUT BUFFER	Spansion LLC	09/661,358 9/14/2000	6,275,421 8/14/2001

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
REDUCTION OF VOLTAGE STRESS ACROSS A GATE OXIDE AND ACROSS A JUNCTION WITHIN A HIGH VOLTAGE TRANSISTOR OF AN ERASABLE MEMORY DEVICE	Spansion LLC	09/774509 1/31/01	6,275,424 8/14/01
BANK SELECTOR CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE	Spansion LLC	09/159,489 9/23/1998	6,275,894 8/14/2001
ELIMINATION OF N+ IMPLANT FROM FLASH TECHNOLOGIES BY REPLACEMENT WITH STANDARD MEDIUMDOPEDDRAIN (MDD) IMPLANT	Spansion LLC	09/708982 11/1/00	6,277,690 8/21/01
MANUFACTURING PROCESS TO ELIMINATE ONO FENCE MATERIAL IN HIGH DENSITY NANDTYPE FLASH MEMORY DEVICES	Spansion LLC	08/993344 12/18/97	6,281,078 8/28/01
SPECIES IMPLANTATION FOR MINIMIZING INTERFACE DEFECT DENSITY IN FLASH MEMORY DEVICES	Spansion LLC	09/609468 7/3/0	6,284,600 9/4/01
PROCESS TO REDUCE POST CYCLING PROGRAM VT DISPERSION FOR NAND FLASH MEMORY DEVICES	Spansion LLC	09/399526 9/20/99	6,284,602 9/4/01
TRENCHED GATE NONVOLATILE SEMICONDUCTOR DEVICE WITH THE SOURCE/DRAIN REGIONS SPACED FROM THE TRENCH BY SIDEWALL DOPINGS	Spansion LLC	09/052057 3/30/98	6,285,054 9/4/01
HIGH SPEED SENSING TO DETECT WRITE PROTECT STATE IN A FLASH MEMORY DEVICE	Spansion LLC	09/506351 2/17/00	6,285,583 9/4/01
OUTPUT SWITCHING IMPLEMENTATION FOR A FLASH MEMORY DEVICE	Spansion LLC	09/421,471 10/19/1999	6,285,585 9/4/2001

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
ERASE SCHEME TO TIGHTEN THE THRESHOLD VOLTAGE DISTRIBUTION OF EEPROM FLASH MEMORY CELLS	Spansion LLC	09/495216 1/31/00	6,285,588 9/4/01
WORDLINE VOLTAGE PROTECTION	Spansion LLC	09/523816 3/13/00	6,285,594 9/4/01
PROCESS FOR FABRICATING AN MNOS FLASH MEMORY DEVICE	Spansion LLC	09/392675 9/8/99	6,287,917 9/11/01
ADDRESS TRANSITION DETECTOR ARCHITECTURE FOR A HIGH DENSITY FLASH MEMORY DEVICE	Spansion LLC	09/663,909 9/18/2000	6,285,627 9/4/2001
METHOD AND APPARATUS FOR CONTINUOUSLY REGULATING A CHARGE PUMP OUTPUT VOLTAGE USING A CAPACITOR DIVIDER	Spansion LLC	09/675940 9/29/00	6,288,951 9/11/01
METHOD FOR REMOVING ANTIREFLECTIVE COATING LAYER USING PLASMA ETCH PROCESS BEFORE CONTACT CMP	Spansion LLC	09/416382 10/12/99	6,291,296 9/18/01
POWER SAVING ON THE FLY DURING READING OF DATA FROM A MEMORY DEVICE	Spansion LLC	09/696652 10/25/00	6,292,425 9/18/01
NITRIDIZATION OF THE PREDDI SCREEN OXIDE	Spansion LLC	09/495213 1/31/00	6,294,430 9/25/01
SEMICONDUCTOR MANUFACTURING METHOD USING A HIGH EXTINCTION COEFFICIENT DIELECTRIC PHOTOMASK	Spansion LLC	09/586254 5/31/00	6,294,460 9/25/01
SYSTEM FOR PROGRAMMING MEMORY CELLS	Spansion LLC	09/514933 2/28/00	6,295,228 9/25/01
SHARED MEMORY APPARATUS AND METHOD FOR MULTIPROCESSOR SYSTEMS	Spansion LLC	09/273430 3/19/99	6,295,571 9/25/01
PROCESS FOR FORMING A BITLINE IN A MONOS DEVICE	Spansion LLC	09/426743 10/25/99	6,297,143 10/2/01
MODE INDICATOR FOR MULTILEVEL MEMORY	Spansion LLC	09/513402 2/25/00	6,297,988 10/2/01

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
ACCELERATION VOLTAGE IMPLEMENTATION FOR A HIGH DENSITY FLASH MEMORY DEVICE	Spansion LLC	09/712,382 11/13/2000	6,297,993 10/2/2001
METHOD AND APPARATUS FOR ELIMINATING FALSE DATA IN A PAGE MODE MEMORY DEVICE	Spansion LLC	09/652,742 8/31/2000	6,298,007 10/2/2001
METHOD FOR REDUCED GATE ASPECT RATIO TO IMPROVE GAPFILL AFTER SPACER ETCH	Spansion LLC	09/368073 8/3/99	6,300,658 10/9/01
A TRENCHED GATE NONVOLATILE SEMICONDUCTOR DEVICE AND METHOD FOR LOW POWER APPLICATIONS WITH CORNER DOPING AND SIDEWALL DOPING	Spansion LLC	09/632536 8/4/00	6,303,437 10/16/01
REGISTER DRIVEN MEANS TO CONTROL PROGRAMMING VOLTAGES	Spansion LLC	09/514404 2/28/00	6,304,487 10/16/01
METHOD AND SYSTEM FOR FABRICATING A FLASH MEMORY ARRAY	Spansion LLC	09/538922 3/30/00	6,306,706 10/23/01
DOUBLE LAYER HARD MASK PROCESS TO IMPROVE OXIDE QUALITY FOR NONVOLATILE FLASH MEMORY PRODUCTS	Spansion LLC	09/716659 11/20/00	6,306,707 10/23/01
METHOD FOR FORMING SELFALIGNED CONTACTS AND LOCAL INTERCONNECTS FOR SALICIDED GATES USING A SECONDARY SPACER	Spansion LLC	09/799469 3/5/01	6,306,713 10/23/01
MULTIPURPOSE GRADED SILICON OXYNITRIDE CAP LAYER	Spansion LLC	09/567534 5/10/00	6,306,758 10/23/01
FLASH MEMORY HAVING A TREATMENT LAYER DISPOSED BETWEEN AN INTERPOLY DIELECTRIC STRUCTURE AND METHOD OF FORMING	Spansion LLC	09/595166 6/15/00	6,306,777 10/23/01
DESCENDING STAIRCASE READ TECHNIQUE FOR A MULTILEVEL CELL NAND FLASH MEMORY DEVICE	Spansion LLC	09/794485 2/26/01	6,307,783 10/23/01

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
NEGATIVE GATE ERASE	Spansion LLC	09/795856 2/28/01	6,307,784 10/23/01
METHOD OF FORMING HIGH K TANTALUM PENTOXIDE TA205 INSTEAD OF ONO STACKED FILMS TO INCREASE COUPLING RATIO AND IMPROVE RELIABILITY FOR FLASH MEMORY DEVICES	Spansion LLC	09/263983 3/5/99	6,309,927 10/30/01
SEMICONDUCTOR ISOLATION PROCESS TO MINIMIZE WEAK OXIDE PROBLEMS	Spansion LLC	09/440934 11/16/99	6,309,949 10/30/01
ARCHITECTURE FOR A DUALBANK PAGE MODE MEMORY WITH REDUNDANCY	Spansion LLC	09/676,902 10/2/2000	6,310,805 10/30/2001
ELIMINATION OF POLY CAP FOR EASY POLY 1 CONTACT FOR NAND PRODUCT	Spansion Technology Inc.	09/531,582 3/21/2000	6,312,991 11/6/200
A METHOD OF FORMING A NAND TYPE FLASH MEMORY DEVICE H AVING A NONSTACKED SELECT GATE TRANSISTOR STRUCTURE	Spansion LLC	09/531749 3/20/00	6,316,293 11/13/01
NITRIDATION PROCESS FOR FABRICATING AN ONO FLOATINGGATE ELECTRODE IN A TWOBIT EEPROM DEVICE	Spansion LLC	09/433037 10/25/99	6,319,775 11/20/01
METHOD FOR MONITORING SECOND GATE OVERETCH IN A SEMICONDUCTOR DEVICE	Spansion LLC	09/368247 8/3/99	6,323,047 11/27/01
FLASH MEMORY DEVICE AND FABRICATION METHOD HAVING A HIGH COUPLING RATIO	Spansion LLC	09/390052 9/3/99	6,323,516 11/27/01
2BIT/CELL TYPE NONVOLATILE SEMICONDUCTOR MEMORY	Spansion Inc.	09/721,656 11/27/2000	6,324,099 11/27/2001
APPLICATION OF EXTERNAL VOLTAGE DURING ARRAY VT TESTING	Spansion LLC	09/667,891 9/22/2000	6,324,108 11/27/2001
METHOD OF FABRICATING A MONOS FLASH CELL USING SHALLOW TRENCH ISOLATION	Spansion LLC	09/426427 10/25/99	6,326,268 12/4/01

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
REFERENCE CELL BITLINE PATH ARCHITECTURE FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	Spansion LLC	09/421,775 10/19/1999	6,327,181 12/4/2001
NONLINEAR STEPPED PROGRAMMING VOLTAGE	Spansion LLC	09/480868 1/10/00	6,327,183 12/4/01
PRECISE REFERENCE WORDLINE LOADING COMPENSATION FOR A HIGH DENSITY FLASH MEMORY DEVICE	Spansion LLC	09/644,358 8/23/2000	6,327,194 12/4/2001
METHOD FOR LATERALLY PEAKED SOURCE DOPING PROFILES FOR BETTER ERASE CONTROL IN FLASH MEMORY DEVICES	Spansion LLC	08/994140 12/19/97	6,329,257 12/11/01
SOLIDSOURCE DOPING FOR SOURCE/DRAIN TO ELIMINATE IMPLANT DAMAGE	Spansion LLC	09/430410 10/29/99	6,329,273 12/11/01
TWO BIT FLASH CELL WITH TWO FLOATING GATE REGIONS	Spansion LLC	09/492,353 1/27/2000	6,329,687 12/11/2001
WRITE PROTECT INPUT IMPLEMENTATION FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	Spansion LLC	09/421,757 10/19/1999	6,331,950 12/18/2001
METHOD AND SYSTEM FOR EMBEDDED CHIP ERASE VERIFICATION	Spansion LLC	09/717550 11/21/00	6,331,951 12/18/01
POSITIVE GATE ERASURE FOR NONVOLATILE MEMORY CELLS	Spansion LLC	09/697810 10/26/00	6,331,952 12/18/01
INTELLIGENT RAMPED GATE AND RAMPED DRAIN ERASURE FOR NONVOLATILE MEMORY CELLS	Spansion LLC	09/697813 10/26/00	6,331,953 12/18/01
METHOD FOR INHIBITING TUNNEL OXIDE GROWTH AT THE EDGES OF A FLOATING GATE DURING SEMICONDUCTOR DEVICE PROCESSING	Spansion LLC	09/824841 4/2/01	6,337,246 1/8/02

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
IN LINE YIELD PREDICTION USING ADC DETERMINED KILL RATIOS DIE HEALTH STATISTICS AND DIE STACKING	Spansion LLC	09/255108 2/22/99	6,338,001 1/8/02
METHOD AND SYSTEM FOR PROVIDING REDUCEDSIZED CONTACTS IN A SEMICONDUCTOR DEVICE	Spansion LLC	09/404395 9/23/99	6,342,415 1/29/02
VARIABLE PULSE WIDTH MEMORY PROGRAMMING	Spansion LLC	09/511874 2/25/00	6,343,033 1/29/02
FULLY RECESSED SEMICONDUCTOR METHOD FOR LOW POWER APPLICATIONS	Spansion LLC	09/620339 7/20/00	6,344,393 2/5/02
DATA RETENTION CHARACTERISTICS AS A RESULT OF HIGH TEMPERATURE BAKE	Spansion LLC	09/795849 2/28/01	6,344,994 2/5/02
PLANARIZATION OF A POLYSILICON LAYER SURFACE BY CHEMICAL MECHANICAL POLISH TO IMPROVE LITHOGRAPHY AND SILICIDE FORMATION	Spansion LLC	09/538168 3/30/00	6,346,466 2/12/02
METHOD OF MAKING TUNGSTEN GATE MOS TRANSISTOR AND MEMORY CELL BY ENCAPSULATING	Spansion LLC	09/649,027 8/28/2000	6,346,467 2/12/2002
SHALLOW TRENCH ISOLATION PROCESS PARTICULARLY SUITED FOR HIGH VOLTAGE CIRCUITS	Spansion LLC	09/109,755 7/2/1998	6,346,737 2/12/2002
WORD LINE DECODING ARCHITECTURE IN A FLASH MEMORY	Spansion LLC	09/690,554 10/17/2000	6,347,052 2/12/2002
METHOD AND APPARATUS FOR DETERMINING THE ROBUSTNESS OF MEMORY CELLS TO ALPHAPARTICLE/COSMIC RAY INDUCED SOFT ERRORS	Spansion LLC	09/664636 9/19/00	6,348,356 2/19/02
METHOD OF FORMING SELFALIGNED CONTACTS USING CONSUMABLE SPACERS	Spansion LLC	09/502153 2/11/00	6,348,379 2/19/02

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
METHOD FOR USING A LOW DIELECTRIC CONSTANT LAYER AS A SEMICONDUCTOR ANTIREFLECTIVE COATING	Spansion LLC	09/586264 5/31/00	6,348,406 2/19/02
SELECTIVE ERASURE OF A NONVOLATILE MEMORY CELL OF A FLASH MEMORY DEVICE	Spansion LLC	09/686693 10/11/00	6,349,062 2/19/02
INTERLEVEL DIELECTRIC THICKNESS MONITOR FOR COMPLEX SEMICONDUCTOR CHIPS	Spansion LLC	09/548741 4/13/00	6,350,627 2/26/02
HIGH VOLTAGE TRANSISTOR WITH MODIFIED FIELD IMPLANT MASK	Spansion LLC	09/533057 3/22/00	6,351,017 2/26/02
VOLTAGE BOOST LEVEL CLAMPING CIRCUIT FOR A FLASH MEMORY	Spansion LLC	09/595,519 6/16/2000	6,351,420 2/26/2002
SYSTEM AND METHOD FOR TRACKING SENSING SPEED BY AN EQUALIZATION PULSE FOR A HIGH DENSITY FLASH MEMORY DEVICE	Spansion LLC	09/663,552 9/18/2000	6,353,566 3/5/2002
DUAL BIT ISOLATION SCHEME FOR FLASH DEVICES	Spansion LLC	09/597358 6/19/00	6,355,514 3/12/02
EFFECT OF DOPED AMORPHOUS SI THICKNESS ON BETTER POLY 1 CONTACT RESISTANCE PERFORMANCE FOR NAND TYPE FLASH MEMORY DEVICES	Spansion LLC	09/263699 3/5/99	6,355,522 3/12/02
USING NEGATIVE GATE ERASE VOLTAGE TO SIMULTANEOUSLY ERASE TWO BITS FROM A NONVOLATILE MEMORY CELL WITH AN OXIDENITRIDEOXIDE (ONO) GATE STRUCTURE	Spansion LLC	09/657029 9/7/00	6,356,482 3/12/02
METHOD FOR FORMING SELFALIGNED CONTACTS AND INTERCONNECTION LINES USING DUAL DAMASCENE TECHNIQUES	Spansion LLC	09/493436 1/29/00	6,359,307 3/19/02

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
LOW VOLTAGE READ CASCODE FOR 2V/3V AND DIFFERENT BANK COMBINATIONS WITHOUT METAL OPTIONS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	Spansion LLC	09/421,985 10/19/1999	6,359,808 3/19/2002
ACTIVATION OF WORDLINE DECODERS TO TRANSFER A HIGH VOLTAGE SUPPLY	Spansion LLC	09/592474 6/9/00	6,359,824 3/19/02
METHOD OF FORMING ONO FLASH MEMORY DEVICES USING LOW ENERGY NITROGEN IMPLANTATION	Spansion LLC	09/648,361 8/25/2000	6,362,051 3/26/2002
USE OF AN ETCH TO REDUCE THE THICKNESS AND ROUND THE EDGES OF A RESIST MASK DURING THE CREATION OF A MEMORY CELL	Spansion LLC	09/627567 7/28/00	6,362,052 3/26/02
LOW COLUMN LEAKAGE NOR FLASH ARRAY SINGLE CELL IMPLEMENTATION	Spansion LLC	09/694688 10/23/00	6,363,014 3/26/02
SUBMICRON SEMICONDUCTOR DEVICE HAVING A SELFALIGNED CHANNEL STOP REGION	SPANSION TECHNOLOGY INC.	09/563,024 5/2/2000	6,365,945 4/2/2002 (TO BE ASSIGNED TO STI)
SELECTIVE ERASURE OF A NONVOLATILE MEMORY CELL OF A FLASH MEMORY DEVICE	Spansion LLC	09/686686 10/11/00	6,366,501 4/2/02
METHOD FOR FABRICATING NONVOLATILE SEMICONDUCTOR MEMORY DEVICE	Spansion Inc.	09/534,507 3/24/2000	6,368,916 4/9/2002
SEMICONDUCTOR DEVICE WITH CONTACTS HAVING A SLOPED PROFILE	Spansion LLC	09/404394 9/23/99	6,369,416 4/9/02
EEPROM HAVING STACKED DIELECTRIC TO INCREASE PROGRAMMING SPEED	Spansion LLC	09/106177 6/29/98	6,369,421 4/9/02
HIGH VOLTAGE TRANSISTOR WITH LOW BODY EFFECT AND LOW LEAKAGE	Spansion LLC	09/182525 10/30/98	6,369,433 4/9/02

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
CEILING TEST MODE TO CHARACTERIZE THE THRESHOLD VOLTAGE DISTRIBUTION OF OVER PROGRAMMED MEMORY CELLS	Spansion LLC	09/884,583 6/19/2001	6,370,061 4/9/2002
SERIAL SEQUENCING OF AUTOMATIC PROGRAM DISTURB ERASE VERIFY DURING A FAST ERASE MODE	Spansion LLC	09/667347 9/22/00	6,370,065 4/9/02
METHOD FOR TRIMMING A PHOTORESIST PATTERN LINE FOR MEMORY GATE ETCHING	Spansion LLC	09/286464 4/6/99	6,372,651 4/16/02
TWO SIDE DECODING OF A MEMORY ARRAY	Spansion LLC	09/689,036 10/12/2000	6,373,742 4/16/2002
PROCESS FOR FABRICATING AN EEPROM DEVICE HAVING A POCKET SUBSTRATE REGION	Spansion LLC	09/487073 1/19/00	6,376,308 4/23/02
METHOD FOR REDUCED GATE ASPECT RATIO TO IMPROVE GAPFILL AFTER SPACER ETCH	Spansion LLC	09/811288 3/16/01	6,376,309 4/23/02
FORMATION OF NONVOLATILE MEMORY DEVICE COMPRISED OF AN ARRAY OF VERTICAL FIELD EFFECT TRANSISTOR STRUCTURES	Spansion LLC	09/817628 3/26/01	6,376,312 4/23/02
OPTIMIZATION OF THERMAL CYCLE FOR THE FORMATION OF POCKET IMPLANTS	Spansion LLC	09/627584 7/28/00	6,376,341 4/23/02
METHOD FOR ELIMINATING ANTIREFLECTIVE COATING IN SEMICONDUCTORS	Spansion LLC	09/588117 5/31/00	6,376,389 4/23/02
DOUBLE SELFALIGNING SHALLOW TRENCH ISOLATION SEMICONDUCTOR AND MANUFACTURING METHOD THEREFOR	Spansion LLC	09/513260 2/24/00	6,376,877 4/23/02
FASTERASE MEMORY DEVICES AND METHOD FOR REDUCING ERASING TIME IN A MEMORY DEVICE	Spansion LLC	09/645623 8/24/00	6,377,488 4/23/02

PATENT
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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
METHOD OF FORMING ONO STACKED FILMS AND DCS TUNGSTEN SILICIDE GATE TO IMPROVE POLYCIDE GATE PERFORMANCE FOR FLASH MEMORY DEVICES	Spansion LLC	09/205899 12/4/98	6,380,029 4/30/02
PROCESS TO IMPROVE READ DISTURB FOR NAND FLASH MEMORY DEVICES	Spansion LLC	09/399414 9/20/99	6,380,033 4/30/02
METHOD FOR CREATING PARTIALLY UV TRANSPARENT ANTIREFLECTIVE COATING FOR SEMICONDUCTORS	Spansion LLC	09/588119 5/31/00	6,380,067 4/30/02
METHODS AND APPARATUS FOR READING A CAM CELL USING BOOSTED AND REGULATED GATE VOLTAGE	Spansion LLC	09/873,927 6/4/2001	6,381,163 4/30/2002
USING A NEGATIVE GATE ERASE TO INCREASE THE CYCLING ENDURANCE OF A NONVOLATILE MEMORY CELL WITH AN OXIDENITRIDEOXIDE (ONO) STRUCTURE	Spansion LLC	09/656675 9/7/00	6,381,179 4/30/02
METHOD OF UTILIZING FAST CHIP ERASE TO SCREEN ENDURANCE REJECTS	Spansion LLC	09/322195 5/28/99	6,381,550 4/30/02
METHOD FOR ETCHING MEMORY GATE STACK USING THIN RESIST LAYER	Spansion LLC	09/375504 8/17/99	6,383,939 5/7/02
I/O PARTITIONING SYSTEM AND METHODOLOGY TO REDUCE BANDTOBAND TUNNELING CURRENT DURING ERASE	Spansion LLC	09/822,995 3/30/2001	6,385,093 5/7/2002
METHOD AND SYSTEM FOR PROVIDING LOCALIZED GATE EDGE ROUNDING WITH MINIMAL ENCROACHMENT AND GATE EDGE LIFTING	Spansion LLC	08/992616 12/17/97	6,387,755 5/14/02
PROCESS FOR FABRICATING SHALLOW POCKET REGIONS IN A NONVOLATILE SEMICONDUCTOR DEVICE	Spansion LLC	09/670229 9/25/00	6,391,730 5/21/02

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REEL: 024522 FRAME: 0474

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
METHOD OF FORMING ONO FLASH MEMORY DEVICES USING RAPID THERMAL OXIDATION	Spansion LLC	09/648,077 8/25/2000	6,395,654 5/28/2002
DUALPORTED CAMS FOR A SIMULTANEOUS OPERATION FLASH MEMORY	Spansion LLC	09/829657 4/10/01	6,396,749 5/28/02
REDUNDANT DUAL BANK ARCHITECTURE FOR A SIMULTANEOUS OPERATION FLASH MEMORY	Spansion LLC	09/632,390 8/4/2000	6,397,313 5/28/2002
PROCESS FOR FABRICATING HIGH DENSITY MEMORY CELLS USING A METALLIC HARD MASK	Spansion LLC	09/429722 10/29/99	6,399,446 6/4/02
SPECIES IMPLANTATION FOR MINIMIZING INTERFACE DEFECT DENSITY IN FLASH MEMORY DEVICES	Spansion LLC	09/882242 6/15/01	6,399,984 6/4/02
ACCURATE VERIFY APPARATUS AND METHOD FOR NOR FLASH MEMORY CELLS IN THE PRESENCE OF HIGH COLUMN LEAKAGE	Spansion LLC	09/842288 4/25/01	6,400,608 6/4/02
CONFIGURE REGISTERS AND LOADS TO TAILOR A MULTILEVEL CELL FLASH DESIGN	Spansion LLC	09/794479 2/26/01	6,400,624 6/4/02
POWERSAVING MODES FOR MEMORIES	Spansion LLC	09/675,372 9/29/2000	6,400,633 6/4/2002
WORDLINE DRIVER FOR FLASH MEMORY READ MODE	Spansion LLC	09/680,344 10/5/2000	6,400,638 6/4/2002
NITROGEN IMPLANT AFTER BITLINE FORMATION FOR ONO FLASH MEMORY DEVICES	Spansion LLC	09/627664 7/28/00	6,403,420 6/11/02
PROCESS FOR FABRICATING AN ONO STRUCTURE HAVING A SILICONRICH SILICON NITRIDE LAYER	Spansion LLC	09/433041 10/25/99	6,406,960 6/18/02

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REEL: 024522 FRAME: 0475

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
ARRANGEMENT FOR PROGRAMMING SELECTED DEVICE REGISTERS DURING INITIALIZATION FROM AN EXTERNAL MEMORY	Spansion LLC	09/654831 9/1/00	6,407,960 6/18/02
PROCESS FOR OPTIMIZING POCKET IMPLANT PROFILE BY RTA IMPLANT ANNEALING FOR A NONVOLATILE SEMICONDUCTOR DEVICE	Spansion LLC	09/620480 7/20/00	6,410,388 6/25/02
METHOD FOR REMOVING SEMICONDUCTOR ARC USING ARC CMP BUFFING	Spansion LLC	09/507810 2/22/00	6,410,443 6/25/02
FLASH MEMORY DEVICE WITH MONITOR STRUCTURE FOR MONITORING SECOND GATE OVERETCH	Spansion LLC	09/774327 1/31/01	6,410,949 6/25/02
METHOD AND SYSTEM FOR USING A SPACER TO OFFSET IMPLANT DAMAGE AND REDUCE LATERAL DIFFUSION IN FLASH MEMORY DEVICES	Spansion LLC	09/478864 1/7/00	6,410,956 6/25/02
CONTINOUS CAPACITOR DIVIDER SAMPLED REGULATION SCHEME	Spansion LLC	09/387018 8/31/99	6,411,069 6/25/02
METHOD OF FORMING A COMPOSITE INTERPOLY GATE DIELECTRIC	Spansion LLC	09/725843 11/30/00	6,413,820 7/2/02
PROCESS FOR REDUCTION OF CAPACITANCE OF A BITLINE FOR A NONVOLATILE MEMORY CELL	Spansion LLC	09/721066 11/22/00	6,417,081 7/9/02
SEMICONDUCTOR STRUCTURE	Spansion LLC	09/651,684 8/30/2000	6,417,082 7/9/2002
HIGH DENSITY MEMORY CELL ASSEMBLY AND METHODS	Spansion LLC	09/128864 8/4/98	6,417,539 7/9/02
PIGGYBACK PROGRAMMING USING GRADUATED STEPS FOR MULTILEVEL CELL FLASH MEMORY DESIGNS	Spansion LLC	09/779225 2/8/01	6,418,053 7/9/02

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EMBEDDED METHODOLOGY TO PROGRAM/ERASE REFERENCE CELLS USED IN SENSING FLASH CELLS	Spansion LLC	09/387421 8/13/99	6,418,054 7/9/02
STEPPER ALIGNMENT MARK FORMATION WITH DUAL FIELD OXIDE PROCESS	Spansion Technology Inc.	09/836,064 4/16/2001	6,420,224 7/16/2002
SEMICONDUCTOR DEVICE WITH SELFALIGNED CONTACTS USING A LINER OXIDE LAYE	Spansion LLC	09/502163 2/11/00	6,420,752 7/16/02
PROGRAM RECONNAISSANCE TO ELIMINATE VARIATIONS IN VT DISTRIBUTIONS OF MULTILEVEL CELL FLASH MEMORY DESIGNS	Spansion LLC	09/779864 2/8/01	6,424,566 7/23/02
USER SELECTABLE CELL PROGRAMMING	Spansion LLC	09/513027 2/25/00	6,424,569 7/23/02
MODULATED CHARGE PUMP WHICH USES AN ANALOG TO DIGITAL CONVERTER TO COMPENSATE FOR SUPPLY VOLTAGE VARIATIONS	Spansion LLC	09/892189 6/26/01	6,424,570 7/23/02
NONVOLATILE MEMORY DEVICE WITH ENCAPSULATED TUNGSTEN GATE AND METHOD OF MAKING SAME	Spansion LLC	09/652,136 8/31/2000	6,429,108 8/6/2002
NAND FLASH MEMORY WITH SPECIFIED GATE OXIDE THICKNESS	Spansion LLC	09/522247 3/9/00	6,429,479 8/6/02
TRIMMING METHOD AND SYSTEM FOR WORDLINE BOOSTER TO MINIMIZE PROCESS VARIATION OF BOOSTED WORDLINE VOLTAGE	Spansion LLC	09/547660 4/12/00	6,430,087 8/6/02
METHOD FOR FORMING HIGH QUALITY MULTIPLE THICKNESS OXIDE LAYERS BY REDUCING DESCUM INDUCED DEFECTS	Spansion LLC	09/535,255 3/23/2000	6,432,618 8/13/2002
METHODS AND ARRANGEMENTS FOR FORMING A SINGLE INTERPOLY DIELECTRIC LAYER IN A SEMICONDUCTOR DEVICE	Spansion LLC	09/357333 7/20/99	6,433,383 8/13/02

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
PROCESS FOR FABRICATING HIGH DENSITY MEMORY CELLS USING A POLYSILICON HARD MASK	Spansion LLC	09/430493 10/29/99	6,436,766 8/20/02
SOURCE DRAIN IMPLANT DURING ONO FORMATION FOR IMPROVED ISOLATION OF SONOS DEVICES	Spansion LLC	09/893,279 6/27/2011	6,436,768 8/20/2002
NOVEL REOXIDATION APPROACH TO IMPROVE PERIPHERAL GATE OXIDE INTEGRITY IN A TUNNEL NITRIDE OXIDATION PROCESS	Spansion LLC	09/879738 6/12/01	6,436,778 8/20/02
METHOD OF DEGASSING LOW K DIELECTRIC FOR METAL DEPOSITION	Spansion LLC	09/652132 8/31/00	6,436,850 8/20/02
METHOD OF PROGRAMMING A NONVOLATILE MEMORY CELL USING A SUBSTRATE BIAS	Spansion LLC	09/697815 10/26/00	6,438,031 8/20/02
THRESHOLD VOLTAGE COMPACTING FOR NONVOLATILE SEMICONDUCTOR MEMORY DESIGNS	Spansion LLC	09/851773 5/9/01	6,438,037 8/20/02
NEGATIVE VOLTAGE REGULATION	Spansion LLC	09/668,100 9/22/2000	6,438,041 8/20/2002
METHOD OF DUAL USE OF NONVOLATILE MEMORY FOR ERROR CORRECTION	Spansion LLC	09/314575 5/18/99	6,438,726 8/20/02
PHOTORESIST SPACER PROCESS SIMPLIFICATION TO ELIMINATE THE STANDARD POLYSILICON OR OXIDE SPACER PROCESS FOR FLASH MEMORY CIRCUITS	Spansion LLC	09/704026 11/1/00	6,440,789 8/27/02
NITRIDE BARRIER LAYER FOR PROTECTION OF ONO STRUCTURE FROM TOP OXIDE LOSS IN A FABRICATION OF SONOS FLASH MEMORY	Spansion LLC	09/966702 9/28/01	6,440,797 8/27/02
SPACER NARROWED, DUAL WIDTH CONTACT FOR CHARGE GAIN REDUCTION	Spansion LLC	09/430848 11/1/99	6,441,418 8/27/02

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
TAILORED ERASE METHOD USING HIGHER PROGRAM VT AND HIGHER NEGATIVE GATE ERASE	Spansion LLC	09/795854 2/28/01	6,442,074 8/27/02
METHOD FOR PRODUCING A SHALLOW TRENCH ISOLATION FILLED WITH THERMAL OXIDE	Spansion Technology Inc.	09/784,892 2/15/2001	6,444,539 9/3/2002
FLASH MEMORY ERASE SPEED BY FLUORINE IMPLANT OR FLUORINATION	Spansion LLC	09/772,600 1/30/2001	6,445,030 9/3/2002
METHOD AND SYSTEM FOR PROVIDING CONTACTS WITH GREATER TOLERANCE FOR MISALIGNMENT IN A FLASH MEMORY	Spansion LLC	09/563797 5/2/00	6,445,051 9/3/02
METHOD AND SYSTEM FOR PROCESSING A SEMICONDUCTOR DEVICE	Spansion LLC	09/539307 3/30/00	6,448,594 9/10/02
SEMICONDUCTOR WITH INCREASED GATE COUPLING COEFFICIENT	Spansion LLC	09/513261 2/24/00	6,448,606 9/10/02
NOVEL CAPPING LAYER	Spansion LLC	09/631894 8/4/00	6,448,608 9/10/02
METHOD AND SYSTEM FOR PROVIDINNG A POLYSILICON STRINGER MONITOR	Spansion LLC	09/429,244 10/28/1999	6,448,609 9/10/2002
LOW COLUMN LEAKAGE NOR FLASH ARRAYDOUBLE CELL IMPLEMENTATION	Spansion LLC	09/884565 6/19/01	6,449,188 9/10/02
ADAPTIVE REFERENCE CELLS FOR A MEMORY DEVICE	Spansion LLC	09/764965 1/17/01	6,449,190 9/10/02
METHOD AND STRUCTURE OF ETCHING A MEMORY CELL POLYSILICON GATE LAYER USING RESIST MASK AND ETCHED SILICON OXYNITRIDE	Spansion LLC	09/617820 7/17/00	6,452,225 9/17/02
LOW THRESHOLD VOLTAGE DEVICE WITH CHARGE PUMP FOR REDUCING STANDBY CURRENT IN AN INTEGRATED CIRCUIT HAVING REDUCED SUPPLY VOLTAGE	Spansion LLC	09/411169 10/1/99	6,452,441 9/17/02

PATENT
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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
FEEDBACK METHOD TO OPTIMIZE ELECTRIC FIELD DURING CHANNEL ERASE OF FLASH MEMORY DEVICES	Spansion LLC	09/693649 10/21/00	6,452,840 9/17/02
ADDRESS BROADCASTING TO A PAGED MEMORY DEVICE TO ELIMINATE ACCESS LATENCY PENALTY	Spansion LLC	09/794478 2/26/01	6,452,869 9/17/02
SEMICONDUCTOR DEVICE HAVING GATE EDGES PROTECTED FROM CHARGE GAIN/LOSS	Spansion LLC	09/834419 4/12/01	6,455,373 9/24/02
ELIMINATION OF OXYNITRIDE (ONO) ETCH RESIDUE AND POLYSILICON STRINGERS THROUGH ISOLATION OF FLOATING GATES ON ADJACENT BITLINES BY POLYSILICON OXIDATION	Spansion LLC	09/506298 2/17/00	6,455,888 9/24/02
METHOD OF DRAIN AVALANCHE PROGRAMMING OF A NONVOLATILE MEMORY CELL	Spansion LLC	09/884402 6/19/01	6,456,531 9/24/02
HIGHER PROGRAM VT AND FASTER PROGRAMMING RATES BASED ON IMPROVED ERASE METHODS	Spansion LLC	09/796282 2/28/01	6,456,533 9/24/02
METHOD OF PROGRAMMING A NONVOLATILE MEMORY CELL USING A SUBSTRATE BIAS	Spansion LLC	09/884409 6/19/01	6,456,536 9/24/02
PROCESS FOR CREATING A FLASH MEMORY CELL USING A PHOTORESIST FLOW OPERATION	Spansion LLC	09/628130 7/28/00	6,458,656 10/1/02
PROCESS FOR FABRICATING AN ONO STRUCTURE	Spansion LLC	09/433186 10/25/99	6,458,677 10/1/02
METHOD OF PROGRAMMING A NONVOLATILE MEMORY CELL USING A DRAIN BIAS	Spansion LLC	09/880367 6/13/01	6,459,618 10/1/02
THREE METAL PROCESS FOR OPTIMIZING LAYOUT DENSITY	Spansion LLC	09/767341 1/23/01	6,459,625 10/1/02

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
SYSTEM AND METHOD TO FACILITATE STABILIZATION OF REFERENCE VOLTAGE SIGNALS IN MEMORY DEVICES	Spansion LLC	09/824166 4/2/01	6,459,628 10/1/02
DUMMY GATE PROCESS TO REDUCE THE VSS RESISTANCE OF FLASH PRODUCTS	Spansion LLC	10/081246 2/22/02	6,461,905 10/8/02
METHOD FOR FORMING HIGH QUALITY MULTIPLE THICKNESS OXIDE LAYERS BY REDUCING DESCUM INDUCED DEFECTS	Spansion LLC	09/535,256 3/23/2000	6,461,973 10/8/2002
POWER SAVING SCHEME FOR BURST MODE IMPLEMENTATION DURING READING OF DATA FROM A MEMORY DEVICE	Spansion LLC	09/729,388 12/4/2000	6,463,003 10/8/2002
VARIABLE SECTOR SIZE FOR A HIGH DENSITY FLASH MEMORY DEVICE	Spansion LLC	09/663,765 9/18/2000	6,463,516 10/8/2002
METHOD OF MANUFACTURING SPACER ETCH MASK FOR SILICONOXIDENITRIDEOXIDESILICON (SONOS) TYPE NONVOLATILE MEMORY	Spansion LLC	09/885490 6/20/01	6,465,303 10/15/02
SIMULTANEOUS FORMATION OF CHARGE STORAGE AND BITLINE TO WORDLINE ISOLATION	Spansion LLC	09/723,635 11/28/2000	6,465,306 10/15/2002
CHARGE GAIN/CHARGE LOSS JUNCTION LEAKAGE PREVENTION FOR FLASH TECHNOLOGY BY USING DOUBLE ISOLATION/CAPPING LAYER BETWEEN LIGHTLY DOPED DRAIN AND GATE	Spansion LLC	09/487964 1/18/00	6,465,835 10/15/02
PIGGYBACK PROGRAMMING USING TIMING CONTROL FOR MULTILEVEL CELL FLASH MEMORY DESIGNS	Spansion LLC	09/779792 2/8/01	6,466,483 10/15/02
SHARED MEMORY APPARATUS AND METHOD FOR MULTIPROCESSOR SYSTEMS	Spansion LLC	09/859193 5/15/01	6,467,011 10/15/02

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
METHOD FOR MANUFACTURING NONVOLATILE SEMICONDUCTOR MEMORY AND NONVOLATILE SEMICONDUCTOR MEMORY MANUFACTURED THEREBY	Spansion Inc.	09/738,760 12/18/2000	6,468,861 10/22/2002
METHOD OF SIMULTANEOUS FORMATION OF BITLINE ISOLATION AND PERIPHEY OXIDE	Spansion LLC	09/723,653 11/28/2000	6,468,865 10/22/2002
FLASH MEMORY DEVICE WITH INCREASE OF EFFICIENCY DURING AN APDE (AUTOMATIC PROGRAM DISTURB AFTER ERASE) PROCESS	Spansion LLC	09/969572 10/1/01	6,469,939 10/22/02
METHOD AND SYSTEM FOR ETCHING TUNNEL OXIDE TO REDUCE UNDERCUTTING DURING MEMORY ARRAY FABRICATION	Spansion LLC	09/925205 8/8/01	6,472,327 10/29/02
METHOD AND SYSTEM FOR TESTING A SEMICONDUCTOR MEMORY DEVICE	Spansion LLC	09/718986 11/22/00	6,472,898 10/29/02
METHOD FOR FORMING A SEMICONDUCTOR DEVICE WITH SELFALIGNED CONTACTS USING A LINER OXIDE LAYER	Spansion LLC	10/109526 3/27/02	6,475,847 11/5/02
METHOD FOR FABRICATING SELFALIGNED GATE OF FLASH MEMORY CELL	Spansion LLC	10/150556 5/17/02	6,475,863 11/5/02
OXYGEN IMPLANTATION FOR REDUCTION OF JUNCTION CAPACITANCE IN MOS TRANSISTORS	Spansion LLC	09/640082 8/17/00	6,475,868 11/5/02
ONO ETCH USING CL2/HE CHEMISTRY	Spansion LLC	09/420687 10/19/99	6,475,915 11/5/02
SELECT TRANSISTOR ARCHITECTURE FOR A VIRTUAL GROUND NONVOLATILE MEMORY CELL AR	Spansion LLC	09/686685 10/11/00	6,477,083 11/5/02
METHOD OF MAKING MEMORY WORDLINE HARD MASK EXTENSION	Spansion LLC	10/109,516 3/27/2002	6,479,348 11/12/2002

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
METHOD FOR FORMING HIGH QUALITY MULTIPLE THICKNESS OXIDE USING HIGH TEMPERATURE DESCUM	Spansion LLC	09/532,347 3/21/2000	6,479,411 11/12/2002
METHOD AND APPARATUS FOR A SEMICONDUCTOR DEVICE WITH ADJUSTABLE THRESHOLD VOLTAGE	Spansion LLC	09/307312 5/7/99	6,479,858 11/12/02
SEMICONDUCTOR MEMORY DEVICE HAVING SOURCE AREAS OF MEMORY CELLS SUPPLIED WITH A COMMON VOLTAGE	Spansion Inc.	09/818,652 3/28/2001	6,480,420 11/12/2002
PSEUDOCONCURRENCY BETWEEN A VOLATILE MEMORY AND A NONVOLATILE MEMORY ON A SAME DATA BUS	Spansion LLC	09/184270 10/31/98	6,480,929 11/12/02
METHOD FOR FORMING SELFALIGNED CONTACTS AND LOCAL INTERCONNECTS USING DECOUPLED LOCAL INTERCONNECT PROCESS	Spansion LLC	09/685972 10/10/00	6,482,699 11/19/02
INTEGRATION OF AN ION IMPLANT HARD MASK STRUCTURE INTO A PROCESS FOR FABRICATING HIGH DENSITY MEMORY CELLS	Spansion LLC	09/627563 7/28/00	6,486,029 11/26/02
FLASH MEMORY WITH LESS SUSCEPTIBILITY TO CHARGE GAIN AND CHARGE LOSS	Spansion LLC	09/532293 3/23/00	6,486,506 11/26/02
DETERMINATION OF DIELECTRIC CONSTANTS OF THIN DIELECTRIC MATERIALS IN A MOS (METAL OXIDE SEMICONDUCTOR) STACK	Spansion LLC	09/904736 7/13/01	6,486,682 11/26/02
METHOD OF PROGRAMMING A NONVOLATILE MEMORY CELL USING A VERTICAL ELECTRIC FIELD	Spansion LLC	09/899721 7/5/01	6,487,121 11/26/02
METHOD OF FORMING A VOIDFREE INTERLAYER DIELECTRIC (ILD0) FOR 0.18UM FLASH MEMORY TECHNOLOGY AND SEMICONDUCTOR DEVICE THEREBY FORMED	Spansion LLC	09/788045 2/16/01	6,489,253 12/3/02

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
METHOD OF ERASING A NONVOLATILE MEMORY CELL USING A SUBSTRATE BIAS	Spansion LLC	09/697814 10/26/00	6,490,205 12/3/02
FLASH MEMORY ARRAY WITH DUAL FUNCTION CONTROL LINES AND ASYMMETRICAL SOURCE AND DRAIN JUNCTIONS	Spansion LLC	09/008162 1/16/98	6,492,675 12/10/02
NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND FABRICATION PROCESS THEREOF	Spansion Inc.	09/963,632 9/27/2001	6,492,677 12/10/2002
SINGLE BIT ARRAY EDGES	Spansion LLC	09/795865 2/28/01	6,493,261 12/10/02
SOFT PROGRAM AND SOFT PROGRAM VERIFY OF THE CORE CELLS IN FLASH MEMORY ARRAY	Spansion LLC	09/829,193 4/9/2001	6,493,266 12/10/2002
SELFALIGNED GATE SEMICONDUCTOR	Spansion LLC	09/636333 8/10/00	6,495,853 12/17/02
CONCURRENT PROGRAM RECONNAISSANCE WITH PIGGYBACK PULSES FOR MULTILEVEL CELL FLASH MEMORY DESIGNS	Spansion LLC	09/779764 2/8/01	6,496,410 12/17/02
NONVOLATILE SEMICONDUCTOR MEMORY	Spansion Inc.	10/043,114 1/14/2002	6,496,414 12/17/2002
METHOD FOR REPAIRING DAMAGE TO CHARGE TRAPPING DIELECTRIC LAYER FROM BIT LINE IMPLANTATION	Spansion LLC	10/023349 12/20/01	6,500,713 12/31/02
METHOD FOR SELECTIVE REMOVAL OF ONO LAYER	Spansion LLC	09/699531 10/30/00	6,500,768 12/31/02
USING A LOW DRAIN BIAS DURING ERASE VERIFY TO ENSURE COMPLETE REMOVAL OF RESIDUAL CHARGE IN THE NITRIDE IN SONOS NONVOLATILE MEMORIES	Spansion LLC	09/684694 10/4/00	6,501,681 12/31/02
DOUBLE BOOSTING SCHEME FOR NAND TO IMPROVE PROGRAM INHIBIT CHARACTERISTICS	Spansion LLC	09/922415 8/3/01	6,504,757 1/7/03

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MULTIPLE CHANNEL IMPLANTATION TO FORM RETROGRADE CHANNEL PROFILE AND TO ENGINEER THRESHOLD VOLTAGE AND SUBSURFACE PUNCHTHROUGH	Spansion LLC	09/667686 9/22/00	6,506,640 1/14/03
INSITU PROCESS FOR FABRICATING A SEMICONDUCTOR DEVICE WITH INTEGRAL REMOVAL OF ANTIREFLECTION AND ETCH STOP LAYERS	Spansion LLC	09/413621 10/6/99	6,506,683 1/14/03
FLASH MEMORY DEVICE AND A FABRICATION PROCESS THEREOF	Spansion Inc.	09/160,046 9/25/1998	6,507,068 1/14/2003
MEMORY LINE DISCHARGE BEFORE SENSING	Spansion LLC	09/698,614 10/27/2000	6,507,527 1/14/2003
METHOD AND SYSTEM FOR QUALIFYING AN ONO LAYER IN A SEMICONDUCTOR DEVICE	Spansion LLC	09/875073 6/5/01	6,509,202 1/21/03
METHOD FOR FORMING SELFALIGNED CONTACTS USING CONSUMABLE SPACERS	Spansion LLC	09/850484 5/7/01	6,509,229 1/21/03
FORMATION OF STI (SHALLOW TRENCH ISOLATION) STRUCTURES WITHIN CORE AND PERIPHERY AREAS OF FLASH MEMORY DEVICE	Spansion LLC	09/969573 10/1/01	6,509,232 1/21/03
NOVEL NITRIDATION BARRIERS FOR NITRIDATED TUNNEL OXIDE FOR CIRCUITRY FOR FLASH TECHNOLOGY AND FOR LOCOS/STI ISOLATION	Spansion LLC	09/491457 1/26/00	6,509,604 1/21/03
DRAIN SIDE SENSING SCHEME FOR VIRTUAL GROUND FLASH EPROM ARRAY WITH ADJACENT BIT CHARGE AND HOLD	Spansion LLC	09/999,869 10/23/2001	6,510,082 1/21/2003
METHOD OF CHANNEL HOT ELECTRON PROGRAMMING FOR SHORT CHANNEL NOR FLASH ARRAYS	Spansion LLC	09/861031 5/18/01	6,510,085 1/21/03

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FLASH MEMORY HAVING PREINTERPOLY DIELECTRIC TREATMENT LAYER AND METHOD OF	Spansion LLC	09/594207 6/14/00	6,512,264 1/28/03
ERASE METHOD FOR DUAL BIT VIRTUAL GROUND FLASH	Spansion LLC	09/886861 6/21/01	6,512,701 1/28/03
METHOD AND SYSTEM FOR REDUCING THINNING OF FIELD ISOLATION STRUCTURES IN A FLASH MEMORY DEVICE	Spansion LLC	09/844692 4/27/01	6,514,822 2/4/03
METHOD OF MANUFACTURING HIGH VOLTAGE TRANSISTOR WITH MODIFIED FIELD IMPLANT MASK	Spansion LLC	10/044510 1/11/02	6,514,830 2/4/03
SEMICONDUCTOR DEVICES WITH REDUCED CONTROL GATE DIMENSIONS	Spansion LLC	09/244429 2/4/99	6,515,328 2/4/03
THIN OXIDE ANTIFUSE	Spansion LLC	09/698485 10/30/00	6,515,344 2/4/03
METHOD AND APPARATUS FOR BOOSTING BITLINES FOR LOW VCC READ	Spansion LLC	09/873643 6/4/01	6,515,902 2/4/03
NEGATIVE PUMP REGULATOR USING MOS CAPACITOR	Spansion LLC	10/050254 1/16/02	6,515,903 2/4/03
DEPOSITED SCREEN OXIDE FOR REDUCING GATE EDGE LIFTING	Spansion LLC	09/476906 1/3/00	6,518,072 2/11/03
USING HOT CARRIER INJECTION TO CONTROL OVERPROGRAMMING IN A NONVOLATILE MEMORY CELL HAVING AN OXIDENITRIDEOXIDE (ONO) STRUCTURE	Spansion LLC	09/902332 7/10/01	6,519,182 2/11/03
SHARED MEMORY APPARATUS AND METHOD FOR MULTIPROCESSOR SYSTEMS	Spansion LLC	09/854351 5/10/01	6,519,672 2/11/03
SOURCE SIDE BORON IMPLANTING AND DIFFUSING DEVICE ARCHITECTURE FOR DEEP SUB 0.18 MICRON FLASH MEMORY	Spansion LLC	09/699972 10/30/02	6,524,914 2/25/03

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HIGH DENSITY FLASH EEPROM ARRAY WITH SOURCE SIDE INJECTION	Spansion LLC	09/892685 6/27/01	6,525,368 2/25/03
NOR ARRAY WITH BURIED TRENCH SOURCE LINE	Spansion LLC	09/917178 7/30/01	6,525,959 2/25/03
METHOD AND APPARATUS FOR ADJUSTING ONCHIP CURRENT REFERENCE FOR EEPROM SENSING	Spansion LLC	10/010985 12/5/01	6,525,966 2/25/03
DECODER APPARATUS AND METHODS FOR PRECHARGING BIT LINES	Spansion LLC	09/928,059 8/10/2001	6,525,969 2/25/2003
PROCESS FOR FABRICATING A NONVOLATILE MEMORY DEVICE	Spansion LLC	09/798,667 3/2/2001	6,528,390 3/4/2003
NAND ARRAY STRUCTURE AND METHOD WITH BURIED LAYER	Spansion LLC	09/665916 9/20/00	6,529,410 3/4/03
SOURCE SIDE SENSING SCHEME FOR VIRTUAL GROUND READ OF FLASH EPROM ARRAY WITH ADJACENT BIT PRECHARGE	Spansion LLC	10/050257 1/16/02	6,529,412 3/4/03
DEVICE MODELING AND CHARACTERIZATION STRUCTURE WITH MULTIPLEXED PADS	Spansion LLC	09/366369 8/3/99	6,530,068 3/4/03
USE OF GASEOUS SILICON HYDRIDES AS A REDUCING AGENT TO REMOVE RESPUTTERED SILICON OXIDE	Spansion LLC	09/543484 4/6/00	6,530,997 3/11/03
METHOD AND APPARATUS FOR SOFT PROGRAM VERIFICATION IN A MEMORY DEVICE	Spansion LLC	10/050650 1/16/02	6,532,175 3/11/03
HIGH VOLTAGE OXIDATION METHOD FOR HIGHLY RELIABLE FLASH MEMORY DEVICES	Spansion LLC	09/803400 3/12/01	6,534,363 3/18/03
METHOD OF HIGH DENSITY PLASMA METAL ETCHING	Spansion LLC	09/548616 4/13/00	6,534,411 3/18/03
MIXED MODE MULTI LEVEL MODE INDICTOR	Spansion LLC	09/905421 7/13/01	6,535,419 3/18/03

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VOLTAGE BOOST CIRCUIT USING SUPPLY VOLTAGE DETECTION TO COMPENSATE FOR SUPPLY VOLTAGE VARIATIONS IN READ MODE VOLTAGES	Spansion LLC	09/915,018 7/25/2001	6,535,424 3/18/2003
METHOD OF FORMING NARROW INSULATING SPACERS FOR USE IN REDUCING MINIMUM COMPONENT SIZE	Spansion LLC	09/691,643 10/18/2000	6,537,866 3/25/2003
PROCESS FOR FABRICATING A NONVOLATILE MEMORY DEVICE	Spansion LLC	09/688504 10/16/00	6,537,881 3/25/03
STAGGERED BITLINE STRAPPING OF A NONVOLATILE MEMORY CELL	Spansion LLC	09/721031 11/22/00	6,538,270 3/25/03
STAIRCASE PROGRAM VERIFY FOR MULTILEVEL CELL FLASH MEMORY DESIGNS	Spansion LLC	09/794482 2/26/01	6,538,923 3/25/03
LOW DEFECT DENSITY PROCESS FOR DEEP SUB0.18UM FLASH MEMORY TECHNOLOGIES	Spansion LLC	09/917182 7/30/01	6,541,338 4/1/03
PLANAR STRUCTURE FOR NONVOLATILE MEMORY DEVICES	Spansion Technology Inc.	09/893,026 6/27/2001	6,541,816 4/1/2003
PIGGYBACK PROGRAMMING USING VOLTAGE CONTROL FOR MULTILEVEL CELL FLASH MEMORY DESIGNS	Spansion LLC	09/779821 2/8/01	6,542,403 4/1/03
METHOD AND APPARATUS FOR EQUALIZATION OF ADDRESS TRANSITION DETECTION PULSE WIDTH	Spansion LLC	09/531871 3/21/00	6,542,435 4/1/03
ERASE VERIFY MODE TO EVALUATE NEGATIVE VT'S	Spansion LLC	09/727656 11/30/00	6,545,912 4/8/03
NOVEL CAPPING LAYER	Spansion LLC	10/179061 6/24/02	6,548,334 4/15/03
PLANARIZATION OF A POLYSILICON LAYER SURFACE BY CHEMICAL MECHANICAL POLISH TO IMPROVE LITHOGRAPHY AND SILICIDE FORMATION	Spansion LLC	10/067765 2/8/02	6,548,336 4/15/03

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NONVOLATILE MEMORY DIELECTRIC AS CHARGE PUMP DIELECTRIC	Spansion LLC	10/147622 5/16/02	6,548,855 4/15/03
USING A NEGATIVE GATE ERASE VOLTAGE APPLIED IN STEPS OF DECREASING AMOUNTS TO REDUCE ERASE TIME FOR A NONVOLATILE MEMORY CELL WITH AN OXIDENITRIDEOXIDE (ONO) STRUCTURE	Spansion LLC	09/657143 9/7/00	6,549,466 4/15/03
SYSTEM AND METHOD TO FACILITATE STABILIZATION OF REFERENCE VOLTAGE SIGNALS IN MEMORY DEVICES	Spansion LLC	10/223486 8/19/02	6,549,477 4/15/03
ARRAY VT MODE IMPLEMENTATION FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	Spansion LLC	09/421,470 10/19/1999	6,550,028 4/15/2003
DUAL WIDTH CONTACT FOR CHARGE GAIN REDUCTION	Spansion LLC	09/430845 11/1/99	6,551,923 4/22/03
PIGGYBACK PROGRAMMING USING AN EXTENDED FIRST PULSE FOR MULTILEVEL CELL FLASH MEMORY DESIGNS	Spansion LLC	09/779794 2/8/01	6,552,929 4/22/03
SIMULTANEOUS FORMATION OF CHARGE STORAGE AND BITLINE TO WORDLINE ISOLATION	Spansion LLC	10/223,195 8/19/2002	6,555,436 4/29/2003
FLASH MEMORY GATE COUPLING USING HSG POLYSILICON	Spansion LLC	08/991448 12/16/97	6,555,867 4/29/03
NONVOLATILE SEMICONDUCTOR MEMORY AND ITS DRIVING METHOD	Spansion Inc.	09/927,387 8/13/2001	6,559,500 5/6/2003
AUTOMATED DETERMINATION AND DISPLAY OF THE PHYSICAL LOCATION OF A FAILED CELL IN AN ARRAY OF MEMORY CELLS	Spansion LLC	09/609793 7/3/00	6,560,729 5/6/03
BITLINE OXIDATION BY REMOVING ONO OXIDE PRIOR TO BITLINE IMPLANT	Spansion LLC	09/651704 8/31/00	6,562,683 5/13/03
SALICIDED GATE FOR VIRTUAL GROUND ARRAYS	Spansion LLC	09/968465 10/1/01	6,566,194 5/20/03

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SHALLOW TRENCH ISOLATION SPACER FOR WEFF IMPROVEMENT	Spansion LLC	10/032630 12/27/01	6,566,230 5/20/03
METHOD FOR SIMULTANEOUS DEPOSITION AND SPUTTERING OF TEOS AND DEVICE THEREBY FORMED	Spansion LLC	09/689144 10/11/00	6,566,252 5/20/03
DIE SEAL FOR SEMICONDUCTOR DEVICE MOISTURE PROTECTION	Spansion LLC	09/998,624 11/30/2001	6,566,736 5/20/2003
PHYSICAL MEMORY LAYOUT WITH VARIOUS SIZED MEMORY SECTORS	Spansion LLC	09/644359 8/23/00	6,567,289 5/20/03
CHARGE INJECTION	Spansion LLC	10/050483 1/16/02	6,567,303 5/20/03
A NONVOLATILE SEMICONDUCTOR MEMORY DEVICE HAVING A CHARGE STORING INSULATION FILM AND DATA HOLDING METHOD THEREFOR	Spansion Inc.	09/689,714 10/13/2000	6,567,312 5/20/2003
2BIT/CELL ARCHITECTURE FOR FLOATING GATE FLASH MEMORY PRODUCT AND ASSOCIATED METHOD	Spansion LLC	10/180673 6/26/02	6,570,211 5/27/03
PROGRAMMING WITH FLOATING SOURCE FOR LOW POWER, LOW LEAKAGE AND HIGH DENSITY FLASH MEMORY DEVICES	Spansion LLC	10/126330 4/19/02	6,570,787 5/27/03
MULTIPLE PURPOSE BUS FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE	Spansion LLC	09/421,758 10/19/1999	6,571,307 5/27/2003
PROCESS FOR MAKING A DUAL BIT MEMORY DEVICE WITH ISOLATED POLYSILICON FLOATING GATES	Spansion LLC	09/810,155 3/16/2001	6,573,140 6/3/2003
METHOD OF FORMING ZERO MARKS	Spansion LLC	09/884204 6/19/01	6,573,151 6/3/03

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METHOD AND DEVICE FOR READING DUAL BIT MEMORY CELLS USING MULTIPLE REFERENCE CELLS WITH TWO SIDE READ	Spansion Inc.	10/052,484 1/18/2002	6,574,139 6/3/2003
SEMICONDUCTOR MEMORY AND ITS USAGE	Spansion Inc.	10/097,924 3/15/2002	6,574,149 6/3/2003
NOVEL METHOD TO DISTINGUISH AN STI OUTER EDGE CURRENT COMPONENT WITH AN STI NORMAL CURRENT COMPONENT	Spansion LLC	10/126363 4/19/02	6,576,487 6/10/03
INTEGRATED CIRCUIT HAVING OPTIMIZED GATE COUPLING CAPACITANCE	Spansion LLC	09/387710 8/30/99	6,576,949 6/10/03
SOURCE BUS FORMATION FOR A FLASH MEMORY USING SILICIDE	Spansion LLC	09/634991 8/8/00	6,579,778 6/17/03
ELIMINATION OF N+ CONTACT IMPLANT FROM FLASH TECHNOLOGIES BY REPLACEMENT WITH STANDARD DOUBLEDIFFUSED AND N+ IMPLANTS	Spansion LLC	09/619231 7/19/00	6,579,781 6/17/03
METHOD OF REDUCING PROGRAM DISTURBS IN NAND TYPE FLASH MEMORY DEVICES	Spansion LLC	09/372406 8/10/99	6,580,639 6/17/03
INNOVATIVE NARROW GATE FORMATION FOR FLOATING GATE FLASH TECHNOLOGY	Spansion LLC	10/178106 6/24/02	6,583,009 6/24/03
SIDEWALL NROM AND METHOD OF MANUFACTURE THEREOF FOR NONVOLATILE MEMORY CELLS	Spansion LLC	09/688,936 10/16/2000	6,583,479 6/24/2003
DATA PREREADING AND ERROR CORRECTION CIRCUIT FOR A MEMORY DEVICE	Spansion LLC	09/314574 5/18/99	6,584,594 6/24/03

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METHOD OF MICROARCHITECTURAL IMPLEMENTATION OF INTERFACE BETWEEN BIST STATE MACHINE AND TESTER INTERFACE TO ENABLE BIST CYCLING	Spansion LLC	09/654965 9/5/00	6,587,982 7/1/03
OXIDE/NITRIDE OR OXIDE/NITRIDE/OXIDE THICKNESS MEASUREMENT USING SCATTEROMETRY	Spansion LLC	09/904089 7/12/01	6,589,804 7/8/03
CHARGE GAIN/CHARGE LOSS JUNCTION LEAKAGE PREVENTION FOR FLASH TECHNOLOGY BY USING DOUBLE ISOLATION/CAPPING LAYER BETWEEN LIGHTLY DOPED DRAIN AND GATE	Spansion LLC	10/180772 6/25/02	6,589,841 7/8/03
MEMORY DEVICE HAVING IMPROVED PROGRAMMABILITY	Spansion LLC	10/103077 3/30/02	6,590,260 7/8/03
HIGHER PROGRAM VT AND FASTER PROGRAMMING RATES BASED ON IMPROVED ERASE METHODS	Spansion LLC	10/173262 6/17/02	6,590,811 7/8/03
SILICON NITRIDE ETCH PROCESS WITH CRITICAL GAIN	Spansion LLC	08/690848 8/1/96	6,593,245 7/15/03
A TEST STRUCTURE APPARATUS FOR MEASURING STANDBY CURRENT IN FLASH MEMORY DEVICES	Spansion LLC	10/112976 3/28/02	6,593,590 7/15/03
STAGGERED BITLINE STRAPPING OF A NONVOLATILE MEMORY CELL	Spansion LLC	09/718771 11/22/00	6,593,606 7/15/03
SYSTEM FOR READING A DOUBLEBIT MEMORY CELL	Spansion Inc.	10/143,449 5/10/2002	6,594,181 7/15/2003
METHOD OF FORMING LOW RESISTANCE COMMON SOURCE LINE FOR FLASH MEMORY DEVICES	Spansion LLC	10/152747 5/21/02	6,596,586 7/22/03

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METHODS TO FORM REDUCED DIMENSION BITLINE ISOLATION IN THE MANUFACTURE OF NONVOLATILE MEMORY DEVICES	Spansion LLC	09/739733 12/18/00	6,596,591 7/22/03
METHOD AND SYSTEM FOR PROVIDING A POLYSILICON STRINGER MONITOR	Spansion LLC	10/155,500 5/23/2002	6,602,776 8/5/2003
METHOD OF FABRICATING NITRIDATED TUNNEL OXIDE BARRIERS FOR FLASH MEMORY DEVICES HAVING STI AND LOCOS ISOLATION	Spansion LLC	10/295738 11/15/02	6,605,511 8/12/03
METHOD FOR MINIMIZING NITRIDE RESIDUE ON A SILICON WAFER	Spansion LLC	10/150282 5/15/02	6,605,517 8/12/03
METHODS AND SYSTEMS FOR FLASH MEMORY TUNNEL OXIDE RELIABILITY TESTING	Spansion LLC	10/121140 4/11/02	6,606,273 8/12/03
HARD MASK REMOVAL PROCESS INCLUDING ISOLATION DIELECTRIC REFILL	Spansion LLC	10/165837 6/6/02	6,607,925 8/19/03
SELFALIGNED POLYSILICON POLISH	Spansion LLC	10/150204 5/15/02	6,610,577 8/26/03
FLASH MEMORY ARRAY AND A METHOD AND SYSTEM OF FABRICATION THEREOF	Spansion LLC	09/563179 5/2/00	6,610,580 8/26/03
ASCENDING STAIRCASE READ TECHNIQUE FOR A MULTILEVEL CELL NAND FLASH MEMORY DEVICE	Spansion LLC	09/794480 2/26/01	6,614,683 9/2/03
POWERSAVING MODES FOR MEMORIES	Spansion LLC	10/061,620 2/1/2002	6,611,473 8/26/2003
METHOD AND SYSTEM FOR QUALIFYING AN ONO LAYER IN A SEMICONDUCTOR DEVICE	Spansion LLC	09/875056 6/5/01	6,617,179 9/9/03
NONVOLATILE MEMORY CIRCUIT FOR RECORDING MULTIPLE BIT INFORMATION	Spansion Inc.	10/069,124 3/1/2002	6,614,686 9/2/2003

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USE OF HIGHK DIELECTRIC MATERIAL FOR ONO AND TUNNEL OXIDE TO IMPROVE FLOATING GATE FLASH MEMORY COUPLING	Spansion LLC	10/176594 6/21/02	6,617,639 9/9/03
MEMORY WORDLINE HARD MASK	Spansion LLC	10/109,235 3/27/2002	6,617,215 9/9/2003
METHOD OF PROGRAMMING A NONVOLATILE MEMORY CELL USING A BAKING PROCESS	Spansion LLC	09/880366 6/13/01	6,618,290 9/9/03
NITRIDING PRETREATMENT OF ONO NITRIDE FOR OXIDE DEPOSITION	Spansion LLC	10/006529 12/5/01	6,620,705 9/16/03
MEMORY WITH DISPOSABLE ARC FOR WORDLINE FORMATION	Spansion LLC	10/100487 3/14/02	6,620,717 9/16/03
SYSTEM FOR PROGRAMMING A FLASH MEMORY DEVICE	Spansion Inc.	10/136,033 4/29/2002	6,621,742 9/16/2003
BURST ARCHITECTURE FOR A FLASH MEMORY	Spansion LLC	09/829,518 4/9/2001	6,621,761 9/16/2003
CHAINED ARRAY OF SEQUENTIAL ACCESS MEMORIES ENABLING CONTINUOUS READ	Spansion LLC	09/525078 3/14/00	6,622,201 9/16/03
MULTISET BLOCK ERASE	Spansion LLC	09/724,675 11/28/2000	6,622,230 9/16/2003
METHOD OF MICROARCHITECTURAL IMPLEMENTATION ON BIST FRONTED STATE MACHINE UTILIZING 'DEATH LOGIC' STATE TRANSITION FOR AREA MINIMIZATION	Spansion LLC	09/655335 9/5/00	6,622,274 9/16/03
METHOD FOR FABRICATING A CONDUCTIVE STRUCTURE FOR A SEMICONDUCTOR DEVICE	Spansion LLC	09/805287 3/13/01	6,627,526 9/30/03
MEMORY DEVICE AND METHOD OF MAKING	Spansion LLC	10/189651 7/3/02	6,627,945 9/30/03

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A VOIDFREE INTERLAYER DIELECTRIC (ILD0) FOR 0.18MICRON FLASH MEMORY SEMICONDUCTOR DEVICE	Spansion LLC	10/244129 9/13/02	6,627,973 9/30/03
MEMORY CIRCUIT FOR SUPPRESSING BIT LINE CURRENT LEAKAGE	Spansion LLC	10/306080 11/26/02	6,628,545 9/30/03
BILAYER FLOATING GATE FOR IMPROVED WORK FUNCTION BETWEEN FLOATING GATE AND A HIGHK DIELECTRIC LAYER	Spansion LLC	10/274063 10/17/02	6,630,383 10/7/03
METHOD OF FABRICATING DOUBLE DENSED CORE GATES IN SONOS FLASH MEMORY	Spansion LLC	09/971483 10/5/01	6,630,384 10/7/03
ONCHIP REPAIR OF DEFECTIVE ADDRESS OF CORE FLASH MEMORY CELLS	Spansion LLC	10/200544 7/22/02	6,631,086 10/7/03
BANK SELECTOR CIRCUIT FOR A SIMULTANEOUS OPERATION FLASH MEMORY DEVICE WITH A FLEXIBLE BANK PARTITION ARCHITECTURE	Spansion LLC	09/892,431 6/26/2001	6,633,949 10/14/2003
METHOD AND SYSTEM FOR REDUCING CHARGE GAIN AND CHARGE LOSS IN INTERLAYER DIELECTRIC FORMATION	Spansion LLC	09/533617 3/22/00	6,635,943 10/21/03
METHOD AND SYSTEM FOR PROCESSING A SEMICONDUCTOR DEVICE	Spansion LLC	09/483176 1/13/00	6,638,358 10/28/03
FULLY ISOLATED DIELECTRIC MEMORY CELL STRUCTURE FOR A DUAL BIT NITRIDE STORAGE DEVICE AND PROCESS FOR MAKING SAME	Spansion LLC	10/027253 12/20/01	6,639,271 10/28/03
OVERERASE CORRECTION METHOD	Spansion LLC	10/099499 3/13/02	6,639,844 10/28/03
NONVOLATILE SEMICONDUCTOR MEMORY DEVICE PROGRAMMING SECOND DYNAMIC	Spansion Inc.	10/356,495 2/3/2003	6,639,849 10/28/2003

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METHOD FOR INCREASING CORE GAIN IN FLASH MEMORY DEVICE USING STRAINED SILICON	Spansion LLC	10/159323 5/31/02	6,642,106 11/4/03
RELACS SHRINK METHOD APPLIED FOR SINGLE PRINT RESIST MASK FOR LDD OR BURIED BITLINE IMPLANTS USING CHEMICALLY AMPLIFIED DUV TYPE PHOTORESIST	Spansion LLC	10/126,326 4/19/2002	6,642,148 11/4/2003
USE OF HIGHK DIELECTRIC MATERIAL IN MODIFIED ONO STRUCTURE FOR SEMICONDUCTOR DEVICES	Spansion LLC	10/097912 3/13/02	6,642,573 11/4/03
SEMICONDUCTOR MEMORY CAPABLE OF BEING DRIVEN AT LOW VOLTAGE AND ITS MANUFACTURE METHOD	Spansion Inc.	09/973,743 10/11/2001	6,642,586 11/4/2003
METHOD FOR IMPROVING READ MARGIN IN A FLASH MEMORY DEVICE	Spansion LLC	10/349293 1/21/03	6,643,177 11/4/03
METHOD FOR REPAIRING OVERERASURE OF FAST BITS IN FLOATING GATE MEMORY DEVICES	Spansion LLC	10/215140 8/7/02	6,643,185 11/4/03
SALICIDED GATE FOR VIRTUAL GROUND ARRAYS	Spansion LLC	09/968456 10/1/01	6,645,801 11/11/03
EXTRACTION OF DRAIN JUNCTION OVERLAP WITH THE GATE AND THE CHANNEL LENGTH FOR ULTRASMALL CMOS DEVICES WITH ULTRATHIN GATE OXIDES	Spansion LLC	10/178144 6/24/02	6,646,462 11/11/03
FLASH MEMORY ARRAY ARCHITECTURE HAVING STAGGERED METAL LINES	Spansion LLC	10/096313 3/12/02	6,646,914 11/11/03
SOURCE SIDE BORON IMPLANT AND DRAIN SIDE MDD IMPLANT FOR DEEP SUB 0.18 MICRON FLASH	Spansion LLC	09/699711 10/30/00	6,653,189 11/25/03
FLASH MEMORY WITH CONTROLLED WORDLINE WIDTH	Spansion LLC	10/023436 12/15/01	6,653,190 11/25/03

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FASL LLC	Spansion LLC	10/151,576 5/16/2002	6,653,191 11/25/2003
FLASH MEMORY ARRAY ARCHITECTURE AND METHOD OF PROGRAMMING, ERASING AND READING THEREOF	Spansion LLC	10/013993 12/11/01	6,654,283 11/25/03
METHOD OF MATCHING CORE CELL AND REFERENCE CELL SOURCE RESISTANCES	Spansion LLC	10/083789 2/27/02	6,654,285 11/25/03
SIMULTANEOUS EXECUTION COMMAND MODES IN A FLASH MEMORY DEVICE	Spansion LLC	09/662791 9/15/00	6,654,848 11/25/03
SPIN ON POLYMERS FOR ORGANIC MEMORY DEVICES	Spansion LLC	10/385375 3/10/03	6,656,763 12/2/03
HIGH DENSITY FLOATING GATE FLASH MEMORY AND FABRICATION PROCESSES THEREFOR	Spansion LLC	10/244229 9/16/02	6,660,588 12/9/03
OTP SECTOR DOUBLE PROTECTION FOR A SIMULTANEOUS OPERATION FLASH MEMORY	Spansion LLC	09/420,535 10/19/1999	6,662,262 12/9/2003
NON SELFALIGNED SHALLOW TRENCH ISOLATION PROCESS WITH DISPOSABLE SPACE TO DEFINE SUBLITHOGRAPHIC POLY SPACE	Spansion LLC	09/973131 10/9/01	6,664,191 12/16/03
ONCHIP ERASE PULSE COUNTER FOR EFFICIENT ERASE VERIFY BIST (BUILTINSELFTEST) MODE	Spansion LLC	10/200330 7/22/02	6,665,214 12/16/03
MULTIPLE BLOCK SEQUENTIAL MEMORY MANAGEMENT	Spansion LLC	09/912834 7/25/01	6,665,777 12/16/03
ALIGNMENT SYSTEM FOR PLANAR CHARGE TRAPPING DIELECTRIC MEMORY CELL LITHOGRAPHY	Spansion LLC	10/394,565 3/21/2003	6,667,212 12/23/2003
NOVEL NAND TYPE CORE CELL STRUCTURE FOR A HIGH DENSITY FLASH MEMORY DEVICE HAVING A UNIQUE SELECT GATE TRANSISTOR CONFIGURATION	Spansion LLC	08/993368 12/18/97	6,667,511 12/23/03

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LOW DIELECTRIC METAL SILICIDE LINED INTERCONNECTION SYSTEM	Spansion LLC	09/252186 2/18/99	6,667,552 12/23/03
METHOD FOR FABRICATING DEVICES IN CORE AND PERIPHERY SEMICONDUCTOR REGIONS USING DUAL SPACERS	Spansion LLC	10/361455 2/10/03	6,670,227 12/30/03
SEMICONDUCTOR MEMORY WITH DEUTERATED MATERIALS	Spansion LLC	10/128,771 4/22/2002	6,670,241 12/30/2003
MULTIPLEBIT NONVOLATILE MEMORY UTILIZING NONCONDUCTIVE CHARGE TRAPPING GATE	Spansion Inc.	10/030,117 1/23/2002	6,670,669 12/30/2003
ULTRAVIOLETLIGHT IRRADIATION APPARATUS	Spansion LLC	10/103557 3/22/02	6,670,616 12/30/03
SHALLOW TRENCH ISOLATION FILL PROCESS	Spansion LLC	10/174550 6/18/02	6,670,691 12/30/03
PIGGYBACK PROGRAMMING WITH STAIRCASE VERIFY FOR MULTILEVEL CELL FLASH MEMORY DESIGNS	Spansion LLC	09/779884 2/8/01	6,671,207 12/30/03
USE OF HIGHK DIELECTRIC MATERIALS IN MODIFIED ONO STRUCTURE FOR SEMICONDUCTOR DEVICES	Spansion LLC	10/036757 12/31/01	6,674,138 1/6/04
DEMAND USABLE ADAPTER MEMORY ACCESS	Spansion LLC	09/912954 7/25/01	6,675,277 1/6/04
DUAL BIT ISOLATION SCHEME FOR FLASH MEMORY DEVICES HAVING POLYSILICON FLOATING GATES	Spansion LLC	09/833307 4/1/101	6,680,507 1/20/04
NITRIDE BARRIER LAYER FOR PROTECTION OF ONO STRUCTURE FROM TOP OXIDE LOSS IN FABRICATION OF SONOS FLASH MEMORY	Spansion LLC	10/158044 5/30/02	6,680,509 1/20/04
INTEGRATED CIRCUIT HAVING INCREASED GATE COUPLING CAPACITANCE	Spansion LLC	09/504087 2/15/00	6,682,978 1/27/04
RELIABILITY MONITOR FOR A MEMORY ARRAY	Spansion LLC	09/733252 12/7/00	6,684,353 1/27/04

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SELECTIVE FORMATION OF TOP MEMORY ELECTRODE BY ELECTROLESS FORMATION OF CONDUCTIVE MATERIALS	Spansion LLC	10/314837 12/9/02	6,686,263 2/3/04
REPLACING A FIRST LINER LAYER WITH A THICKER OXIDE LAYER WHEN FORMING A SEMICONDUCTOR DEVICE	Spansion LLC	10/126841 4/19/02	6,689,666 2/10/04
ALGORITHM DYNAMIC REFERENCE PROGRAMMING	Spansion LLC	10/119391 4/8/02	6,690,602 2/10/04
FLASH MEMORY CELL WITH MINIMIZED FLOATING GATE TO DRAIN/SOURCE OVERLAP FOR MINIMIZING CHARGE LEAKAGE	Spansion LLC	09/713390 11/15/00	6,693,009 2/17/04
REPLACING LAYERS OF AN INTERGATE DIELECTRIC LAYER WITH HIGHK MATERIAL FOR IMPROVED SCALABILITY	Spansion LLC	10/145952 5/15/02	6,693,321 2/17/04
METHOD OF PROTECTING A STACKED GATE STRUCTURE DURING FABRICATION	Spansion LLC	10/217807 8/12/02	6,696,331 2/24/04
REDUCTION OF SECTOR CONNECTING LINE CAPACITANCE USING STAGGERED METAL LINES	Spansion LLC	10/013902 12/11/01	6,700,201 3/2/04
REFRESH SCHEME FOR DYNAMIC PAGE PROGRAMMING	Spansion LLC	10/119273 4/8/02	6,700,815 3/2/04
LASER THERMAL ANNEALING OF SILICON NITRIDE FOR INCREASED DENSITY AND ETCH SELECTIVITY	Spansion LLC	10/096741 3/14/02	6,706,576 3/16/04
HARD MASK PROCESS FOR MEMORY DEVICE WITHOUT BITLINE SHORTS	Spansion LLC	10/100,485 3/14/2002	6,706,595 3/16/2004
DUMMY WORDLINE FOR ERASE AND BITLINE LEAKAGE	Spansion LLC	10/230,729 8/29/2002	6,707,078 3/16/2004
INTERLACED MULTILEVEL MEMORY	Spansion LLC	09/516478 3/1/00	6,707,713 3/16/04
GENERATION OF MARGINING VOLTAGE ONCHIP DURING TESTING CAM PORTION OF FLASH MEMORY DEVICE	Spansion LLC	10/200539 7/22/02	6,707,718 3/16/04

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FABRICATION OF SHALLOW TRENCH ISOLATION STRUCTURES WITH ROUNDED CORNER AND SELFALIGNED GATE	Spansion LLC	10/292121 11/12/02	6,709,924 3/23/04
PROCESS FOR TREATING ONO DIELECTRIC FILM OF A FLOATING GATE MEMORY CELL	Spansion LLC	09/927134 8/10/01	6,709,927 3/23/04
DUAL BIT MEMORY DEVICE WITH ISOLATED POLYSILICON FLOATING GATES	Spansion LLC	09/809,969 3/16/2001	6,713,809 3/30/2004
MASK FOR AND METHOD OF FORMING A CHARACTER ON A SUBSTRATE	Spansion LLC	09/639798 8/17/00	6,713,842 3/30/04
METHODS AND SYSTEMS FOR A SHARED MEMORY UNIT WITH EXTENDABLE FUNCTIONS	Spansion LLC	09/912898 7/25/01	6,715,059 3/30/04
VIRTUAL GROUND SILICIDE BIT LINE PROCESS FOR FLOATING GATE FLASH MEMORY	Spansion LLC	10/238412 9/10/02	6,716,698 4/6/04
METHOD OF FORMING FLASH MEMORY HAVING PREINTERPOLY DIELECTRIC TREATMENT LAYER	Spansion LLC	10/291293 11/8/02	6,716,702 4/6/04
USING A FIRST LINER LAYER AS A SPACER IN A SEMICONDUCTOR DEVICE	Spansion LLC	10/126207 4/19/02	6,716,710 4/6/04
EFFICIENT METHOD TO DETECT PROCESS INDUCED DEFECTS IN THE GATE STACK OF FLASH MEMORY DEVICES	Spansion LLC	10/313676 12/5/02	6,717,850 4/6/04
MEMORY MANUFACTURING PROCESS USING DISPOSABLE ARC FOR WORDLINE FORMATION	Spansion LLC	10/126,280 4/19/2002	6,720,133 4/13/2004
METHOD FOR MANUFACTURING MEMORY WITH HIGH CONDUCTIVITY BITLINE AND SHALLOW TRENCH ISOLATION INTEGRATION	Spansion LLC	10/022292 12/15/01	6,723,605 4/20/04
PERFORMANCE IN FLASH MEMORY DEVICES	Spansion LLC	10/358866 2/5/03	6,723,638 4/20/04

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METHOD AND SYSTEM FOR DECREASING THE SPACES BETWEEN WORDLINES	Spansion LLC	09/777457 2/6/01	6,727,195 4/27/04
PATH GATE DRIVER CIRCUIT	Spansion LLC	10/243,433 9/12/2002	6,728,160 4/27/2004
DATA RECYCLING IN MEMORY	Spansion LLC	09/513698 2/25/00	6,728,913 4/27/04
SALICIDED GATE FOR VIRTUAL GROUND ARRAYS	Spansion LLC	10/217,821 8/12/2002	6,730,564 5/4/2004
METHOD OF DETERMINING GATE OXIDE THICKNESS OF AN OPERATIONAL MOSFET	Spansion LLC	10/017832 12/12/01	6,731,130 5/4/04
PASSWORD AND DYNAMIC PROTECTION OF FLASH MEMORY DATA	Spansion LLC	10/091767 3/7/02	6,731,536 5/4/04
CIRCUIT FOR ACCURATE MEMORY READ OPERATIONS	Spansion LLC	10/313444 12/5/02	6,731,542 5/4/04
INTEGRATION OF EMBEDDED AND TEST MODE TIMER	Spansion LLC	09/664819 9/19/00	6,732,308 5/4/04
METHOD OF DETECTING SHALLOW TRENCH ISOLATION CORNER THINNING BY ELECTRICAL STRESS	Spansion LLC	10/113152 3/28/02	6,734,028 5/11/04
SEMICONDUCTOR ISOLATION MATERIAL DEPOSITION SYSTEM AND METHOD	Spansion LLC	10/159078 5/31/02	6,734,080 5/11/04
METHOD OF IMPROVING DYNAMIC REFERENCE TRACKING FOR FLASH MEMORY UNIT	Spansion LLC	10/357879 2/4/03	6,735,114 5/11/04
HIGH DENSITY DUAL BIT FLASH MEMORY CELL WITH NON PLANAR STRUCTURE	Spansion LLC	10/164895 6/7/02	6,735,123 5/11/04
FLASH MEMORY DEVICE HAVING FOURBIT CELLS	Spansion LLC	10/315632 12/10/02	6,735,124 5/11/04
METHOD OF DRIVING A SEMICONDUCTOR MEMORY	Spansion Inc.	10/160,050 6/4/2002	6,735,127 5/11/2004
STRUCTURE AND METHOD FOR REDUCING CHARGE LOSS IN A MEMORY CELL	Spansion LLC	10/313454 12/5/02	6,737,701 5/18/04

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MEMORY ARRAY WITH BURIED BIT LINES	Spansion LLC	10/095512 3/12/02	6,737,703 5/18/04
PROCESS FOR REDUCING HYDROGEN CONTAMINATION IN DIELECTRIC MATERIALS IN MEMORY DEVICES	Spansion LLC	10/429,447 5/5/2003	6,740,605 5/25/2004
PLANAR TRANSISTOR STRUCTURE USING ISOLATION IMPLANTS FOR IMPROVED VSS RESISTANCE AND FOR PROCESS SIMPLIFICATION	Spansion LLC	10/032646 12/27/01	6,740,926 5/25/04
METHOD FOR FABRICATING NITRIDE MEMORY CELLS USING A FLOATING GATE FABRICATION PROCESS	Spansion LLC	10/306529 11/27/02	6,743,677 6/1/04
MEMORY ARRAY HAVING SHALLOW BIT LINE WITH SILICIDE CONTACT PORTION AND METHOD OF FORMATION	Spansion LLC	10/382731 3/5/03	6,744,105 6/1/04
METHOD AND SYSTEM TO MINIMIZE PAGE PROGRAMMING TIME FOR FLASH MEMORY DEVICES	Spansion LLC	10/243,792 9/12/2002	6,744,666 6/1/2004
FLASH MEMORY ARRAY WITH DUAL FUNCTION CONTROL LINES AND ASYMMETRICAL SOURCE AND DRAIN JUNCTIONS	Spansion LLC	10/233906 9/3/02	6,744,668 6/1/04
CIRCUIT FOR FAST AND ACCURATE MEMORY READ OPERATIONS	Spansion LLC	10/387617 3/13/03	6,744,674 6/1/04
PROGRAM ALGORITHM INCLUDING SOFT ERASE FOR SONOS MEMORY DEVICE	Spansion LLC	10/305756 11/26/02	6,744,675 6/1/04
METHOD OF FORMING COPPER SULFIDE FOR MEMORY CELL	Spansion LLC	10/314060 12/5/02	6,746,971 6/8/04
MEMORY CIRCUIT ARRANGEMENT FOR PROGRAMMING A MEMORY CELL	Spansion LLC	10/348732 1/21/03	6,747,900 6/8/04
PRECISION HIGHK INTERGATE DIELECTRIC LAYER	Spansion LLC	10/117818 4/8/02	6,750,066 6/15/04

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
NROM CELL WITH NLESS CHANNEL	Spansion LLC	10/086,112 2/27/2002	6,750,103 6/15/2004
NONVOLATILE MEMORY CELL WITH A NITRIDATED OXIDE LAYER	Spansion LLC	10/199793 7/19/02	6,750,157 6/15/04
SEMICONDUCTOR MEMORY AND METHOD OF MANUFACTURE THEREOF	Spansion Inc.	10/085,023 3/1/2002	6,750,520 6/15/2004
SYSTEM AND METHOD FOR CHARGE RESTORATION IN A NONVOLATILE MEMORY DEVICE	Spansion LLC	10/338333 1/7/03	6,751,146 6/15/04
MEMORY CELL FORMATION WITH PROCESS FOR PATTERNING CONDUCTING POLYMER FILMS	Spansion LLC	10/285183 10/31/02	6,753,247 6/22/04
MEMORY DEVICE AND METHOD OF MAKING	Spansion LLC	10/223920 8/20/02	6,753,570 6/22/04
TRENCH SIDE WALL CHARGE TRAPPING DIELECTRIC FLASH MEMORY DEVICE	Spansion LLC	10/430,582 5/6/2003	6,754,105 6/22/2004
REFERENCE CELL WITH VARIOUS LOAD CIRCUITS COMPENSATING FOR SOURCE SIDE LOADING EFFECTS IN A NONVOLATILE MEMORY	Spansion LLC	10/245146 9/16/02	6,754,106 6/22/04
METHOD OF PROGRAMMING INSERIES MEMORY CELLS	Spansion LLC	10/282847 10/29/02	6,754,109 6/22/04
METHOD OF DETERMINING LOCATION OF GATE OXIDE BREAKDOWN OF MOSFET BY MEASURING CURRENTS	Spansion LLC	10/113017 3/28/02	6,756,806 6/29/04
METHOD OF DETERMINING THE ACTIVE REGION WIDTH BETWEEN SHALLOW TRENCH ISOLATION STRUCTURES USING A GATE CURRENT MEASUREMENT TECHNIQUE FOR FABRICATING A FLASH MEMORY SEMICONDUCTOR DEVICE AND DEVICE THEREBY FORMED	Spansion LLC	10/224737 8/20/02	6,759,295 7/6/04

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STACKED POLYSILICON LAYER FOR BORON PENETRATION INHIBITION	Spansion LLC	10/118363 4/8/02	6,762,454 7/13/04
TRENCHED GATE NONVOLATILE SEMICONDUCTOR METHOD WITH THE SOURCE/DRAIN REGIONS SPACED FROM THE TRENCH BY SIDEWALL DOPINGS	Spansion LLC	09/629780 7/31/00	6,764,904 7/20/04
METHOD FOR REDUCING SHALLOW TRENCH ISOLATION EDGE THINNING ON TUNNEL OXIDES USING PARTIAL NITRIDE STRIP AND SMALL BIRD'S BEAK FORMATION FOR HIGH PERFORMANCE FLASH MEMORY DEVICES	Spansion LLC	10/126840 4/19/02	6,764,920 7/20/04
STRUCTURE AND METHOD FOR PREVENTING UV RADIATION DAMAGE AND INCREASING DATA RETENTION IN MEMORY CELLS	Spansion LLC	10/460279 6/12/03	6,765,254 7/20/04
METHOD FOR MANUFACTURING NONVOLATILE SEMICONDUCTOR MEMORY AND NONVOLATILE SEMICONDUCTOR MEMORY MANUFACTURED THEREBY	Spansion Inc.	10/237,805 9/10/2002	6,765,271 7/20/2004
METHOD AND SYSTEM FOR DETECTING DEFECTIVE MATERIAL SURROUNDING FLASH MEMORY CELLS	Spansion LLC	10/384936 3/10/03	6,765,827 7/20/04
NONVOLATILE SEMICONDUCTOR STORAGE DEVICE AND METHOD OF READING OUT DATA	Spansion Inc.	10/356,496 2/3/2003	6,765,828 7/20/2004
STRUCTURE AND METHOD FOR SUPPRESSING OXIDE ENCROACHMENT IN A FLOATING GATE MEMORY CELL	Spansion LLC	10/364569 2/10/03	6,767,791 7/27/04
MEMORY DEVICE	Spansion LLC	10/413829 4/15/03	6,768,157 7/27/04

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
NOVEL NONVOLATILE MEMORY CELL AND METHOD OF PROGRAMMING FOR IMPROVED DATA RETENTION	Spansion LLC	10/352658 1/28/03	6,768,160 7/27/04
METHOD OF PROGRAMMING AND READING A DUAL CELL MEMORY DEVICE	Spansion LLC	10/422276 4/24/03	6,768,673 7/27/04
CASCODE AMPLIFIER CIRCUIT FOR PRODUCING A FAST, STABLE AND ACCURATE BIT LINE VOLTAGE	Spansion LLC	10/302672 11/22/02	6,768,677 7/27/04
SELECTION CIRCUIT FOR ACCURATE MEMORY READ OPERATIONS	Spansion LLC	10/361378 2/10/03	6,768,679 7/27/04
LOW COLUMN LEAKAGE FLASH MEMORY ARRAY	Spansion LLC	10/095739 3/12/02	6,768,683 7/27/04
METHOD FOR SEMICONDUCTOR WAFER PLANARIZATION BY CMP STOP LAYER FORMATION	Spansion LLC	10/190397 7/2/02	6,770,523 8/3/04
IMPLANTATION FOR THE FORMATION OF CUX LAYER IN AN ORGANIC MEMORY DEVICE	Spansion LLC	10/314054 12/5/02	6,770,905 8/3/04
DIODE FABRICATION FOR ESD/EOS PROTECTION	Spansion LLC	10/050394 1/16/02	6,770,938 8/3/04
IMPLEMENTING REFERENCE CURRENT MEASUREMENT MODE WITHIN REFERENCE ARRAY PROGRAMMING MODE OR REFERENCE ARRAY ERASE MODE IN A SEMICONDUCTOR	Spansion LLC	10/254381 9/25/02	6,771,093 8/3/04
PRECHARGING SCHEME FOR READING A MEMORY CELL	Spansion LLC	10/226912 8/22/02	6,771,543 8/3/04
METHOD FOR READING A NONVOLATILE MEMORY CELL ADJACENT TO AN INACTIVE REGION OF A NONVOLATILE MEMORY CELL ARRAY	Spansion LLC	10/353558 1/29/03	6,771,545 8/3/04
METHODS OF FORMING PASSIVE LAYERS IN ORGANIC MEMORY CELLS	Spansion LLC	10/313494 12/5/02	6,773,954 8/10/04
MEMORY WORDLINE SPACER	Spansion LLC	10/243108 9/13/02	6,773,988 8/10/04

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METHOD FOR REDUCING SHORT CHANNEL EFFECTS IN MEMORY CELLS AND RELATED STRUCTURE	Spansion LLC	10/429150 5/3/03	6,773,990 8/10/04
UVBLOCKING LAYER FOR REDUCING UVINDUCED CHARGING OF SONOS DUALBIT FLASH MEMORY DEVICES IN BEOL PROCESSING	Spansion LLC	10/358589 2/5/03	6,774,432 8/10/04
METHOD OF PROGRAMMING A DUAL CELL MEMORY DEVICE	Spansion LLC	10/422489 4/24/03	6,775,187 8/10/04
TEST STRUCTURE TO MEASURE INTERLAYER DIELECTRIC EFFECTS AND BREAKDOWN AND DETECT METAL DEFECTS IN FLASH MEMORIES	Spansion LLC	10/174734 6/18/02	6,777,957 8/17/04
MEMORY CIRCUIT FOR PROVIDING WORD LINE REDUNDANCY IN A MEMORY SECTOR	Spansion LLC	10/635974 8/7/03	6,778,437 8/17/04
METHOD OF DUAL CELL MEMORY DEVICE OPERATION FOR IMPROVED ENDOFLIFE READ MARGIN	Spansion LLC	10/422092 4/24/03	6,778,442 8/17/04
METHOD OF FORMING CORE AND PERIPHERY GATES INCLUDING TWO CRITICAL MASKING STEPS TO FORM A HARD MASK IN A CORE REGION THAT INCLUDES A CRITICAL DIMENSION LESS THAN ACHIEVABLE AT A RESOLUTION LIMIT OF LITHOGRAPHY	Spansion LLC	10/382744 3/5/03	6,780,708 8/24/04
BUFFER DRIVER CIRCUIT FOR PRODUCING A FAST, STABLE, AND ACCURATE REFERENCE VOLTAGE	Spansion LLC	10/282459 10/29/02	6,781,417 8/24/04
SYSTEM FOR SETTING MEMORY VOLTAGE THRESHOLD	Spansion Inc.	10/096,338 3/11/2002	6,781,884 8/24/2004
METHOD OF PROGRAMMING A MEMORY CELL	Spansion LLC	10/379885 3/5/03	6,781,885 8/24/04

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RESOURCE LOCKING AND THREAD SYNCHRONIZATION IN A MULTIPROCESSOR ENVIRONMENT	Spansion LLC	09/912870 7/25/01	6,782,440 8/24/04
PROCESS TO IMPROVE THE VSS LINE FORMATION FOR HIGH DENSITY FLASH MEMORY AND RELATED STRUCTURE ASSOCIATED THEREWITH	Spansion LLC	10/179723 6/25/02	6,784,061 8/31/04
METHOD OF DETECTING SHALLOW TRENCH ISOLATION CORNER THINNING BY ELECTRICAL TRAPPING	Spansion LLC	10/113259 3/28/02	6,784,682 8/31/04
INTERNAL SELFTEST CIRCUIT FOR A MEMORY ARRAY	Spansion LLC	09/732616 12/7/00	6,785,856 8/31/04
POLYMER MEMORY DEVICE FORMED IN VIA OPENING	Spansion LLC	10/614397 7/7/03	6,787,458 9/7/04
NITRIDATED TUNNEL OXIDE BARRIERS FOR FLASH MEMORY TECHOLOGY CIRCUITRY	Spansion LLC	09/492931 1/27/00	6,787,840 9/7/04
NONVOLATILE SEMICONDUCTOR STORAGE DEVICE AND DATA ERASING METHOD	Spansion Inc.	10/454,630 6/5/2003	6,788,580 9/7/2004
PRECHARGE METHOD FOR READING A NONVOLATILE MEMORY CELL	Spansion LLC	10/307749 12/2/02	6,788,583 9/7/04
METHODS OF CONTROLLING VSS IMPLANTS ON MEMORY DEVICES, AND SYSTEM FOR PERFORMING SAME	Spansion LLC	10/358587 2/5/03	6,790,752 9/14/04
NONVOLATILE MEMORY READ CIRCUIT WITH END OF LIFE SIMULATION	Spansion LLC	10/431,320 5/6/2003	6,791,880 9/14/2004
CHARGETRAPPING MEMORY ARRAYS RESISTANT TO DAMAGE FROM CONTACT HOLE FORMATION	Spansion LLC	10/382,726 3/5/2003	6,794,764 9/21/2004
SYSTEM FOR PROGRAMMING A NONVOLATILE MEMORY CELL	Spansion LLC	10/307667 12/2/02	6,795,342 9/21/04
METHOD FOR READING A NONVOLATILE MEMORY CELL	Spansion LLC	10/283590 10/30/02	6,795,357 9/21/04

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
METHODS FOR FABRICATING AND PLANARIZING DUAL POLY SCALABLE SONOS FLASH MEMORY	Spansion LLC	10/244369 9/16/02	6,797,565 9/28/04
FLASH MEMORY DEVICES WITH OXYNITRIDE DIELECTRIC AS THE CHARGE STORAGE MEDIA	Spansion LLC	10/342032 1/14/03	6,797,650 9/28/04
DUALPURPOSE ANTIREFLECTIVE COATING AND SPACER FOR FLASH MEMORY AND OTHER DUAL GATE TECHNOLOGIES AND METHOD OF FORMING	Spansion LLC	09/607675 6/30/00	6,798,002 9/28/04
MOCVD FORMATION OF CU2S	Spansion LLC	10/305889 11/26/02	6,798,068 9/28/04
FAST, ACCURATE AND LOW POWER SUPPLY VOLTAGE BOOSTER USING A/D CONVERTER	Spansion LLC	10/406415 4/3/03	6,798,275 9/28/04
SYSTEM AND METHOD FOR MULTIBIT FLASH READS USING DUAL DYNAMIC REFERENCES	Spansion LLC	10/136,173 5/1/2002	6,799,256 9/28/2004
LINER FOR SEMICONDUCTOR MEMORIES AND MANUFACTURING METHOD THEREFOR	Spansion LLC	10/109,234 3/27/2002	6,803,265 10/12/2004
SILICON CONTAINING MATERIAL FOR PATTERNING POLYMERIC MEMORY ELEMENT	Spansion LLC	10/614484 7/7/03	6,803,267 10/12/04
USE OF HIGHK DIELECTRIC MATERIAL IN MODIFIED ONO STRUCTURE FOR SEMICONDUCTOR DEVICES	Spansion LLC	10/646080 8/22/03	6,803,272 10/12/04
ONO FABRICATION PROCESS FOR REDUCING OXYGEN VACANCY CONTENT IN BOTTOM OXIDE LAYER IN FLASH MEMORY DEVICES	Spansion LLC	10/308,518 12/3/2002	6,803,275 10/12/2004
METHOD AND SYSTEM FOR SCALING NONVOLATILE MEMORY CELLS	Spansion LLC	10/150255 5/15/02	6,806,155 10/19/04
ISOLATION TRENCH FILL PROCESS	Spansion LLC	10/120116 4/9/02	6,806,165 10/19/04

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MEMORY DEVICE	Spansion LLC	10/304863 11/27/02	6,806,526 10/19/04
METHOD AND SYSTEM FOR TESTING TUNNEL OXIDE ON A MEMORYRELATED STRUCTURE	Spansion LLC	10/339536 1/8/03	6,808,945 10/26/04
METHOD FOR FORMING ISOLATION IN FLASH MEMORY WAFER	Spansion LLC	09/019409 2/5/98	6,808,988 10/26/04
METHOD AND SYSTEM FOR TAILORING CORE AND PERIPHERY CELLS IN A NONVOLATILE MEMORY	Spansion LLC & FASL LLC	10/150240 5/15/02	6,808,992 10/26/04
METHOD FOR PROTECTING GATE EDGES FROM CHARGE GAIN/LOSS IN SEMICONDUCTOR DEVICE	Spansion LLC	09/376659 8/18/99	6,808,996 10/26/04
INNOVATIVE METHOD OF HARD MASK REMOVAL	Spansion LLC	10/045,354 11/7/2001	6,809,033 10/26/2004
REFLOWABLEDOPED HDP FILM	Spansion LLC	10/217403 8/14/02	6,809,402 10/26/04
METHOD AND SYSTEM FOR DETERMINING FLOW RATES FOR CONTACT FORMATION	Spansion LLC	10/165383 6/6/02	6,811,932 11/2/04
HIGH DENSITY FLOATING GATE FLASH MEMORY AND FABRICATION PROCESSES THEREFOR	Spansion LLC	10/660420 9/10/03	6,812,514 11/2/04
METHOD AND APPARATUS FOR IMPROVED PERFORMANCE OF FLASH MEMORY CELL DEVICES	Spansion LLC	09/492243 1/27/00	6,812,521 11/2/04
SYSTEM FOR USING A DYNAMIC REFERENCE IN A DOUBLEBIT CELL MEMORY	Spansion Inc.	10/197,116 7/16/2002	6,813,189 11/2/2004
I/O BASED COLUMN REDUNDANCY FOR VIRTUAL GROUND WITH 2BIT CELL FLASH MEMORY	Spansion LLC	09/676,623 10/2/2000	6,813,735 11/2/2004
METHOD OF DETERMINING CHARGE LOSS ACTIVATION ENERGY OF A MEMORY ARRAY	Spansion LLC	10/306667 11/26/02	6,813,752 11/2/04

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
MEMORY DEVICE	Spansion LLC	10/238880 9/11/02	6,815,286 11/9/04
FLASH MEMORY HAVING IMPROVED CORE FIELD ISOLATION IN SELECT GATE REGIONS	Spansion LLC	10/260061 9/27/02	6,815,292 11/9/04
SYSTEM FOR CONTROL OF PRECHARGE LEVELS IN A MEMORY DEVICE	Spansion Inc.	10/136,034 4/29/2002	6,816,423 11/9/2004
METHOD OF DETERMINING THE ACTIVE REGION WIDTH BETWEEN SHALLOW TRENCH ISOLATION STRUCTURES USING A CV MEASUREMENT TECHNIQUE FOR FABRICATING A FLASH MEMORY SEMICONDUCTOR DEVICE AND A DEVICE THEREBY FORMED	Spansion LLC	10/224028 8/19/02	6,818,462 11/16/04
METHOD FOR ERASING A MEMORY SECTOR IN VIRTUAL GROUND ARCHITECTURE WITH REDUCED LEAKAGE CURRENT	Spansion LLC & FASL, LLC	10/762071 1/20/04	6,819,591 11/16/04
APPARATUS AND METHOD FOR A SENSE AMPLIFIER CIRCUIT THAT SAMPLES AND HOLDS A REFERENCE VOLTAGE	Spansion LLC	10/389149 3/13/03	6,819,612 11/16/04
MEMORY DEVICE HAVING RESISTIVE ELEMENT COUPLED TO REFERENCE CELL FOR IMPROVED RELIABILITY	Spansion LLC	10/285909 10/31/02	6,819,615 11/16/04
METHOD OF DETECTING AND DISTINGUISHING STACK GATE EDGE DEFECTS AT THE SOURCE OR DRAIN JUNCTION	Spansion LLC	10/126193 4/19/02	6,822,259 11/23/04
METHOD OF CONTROLLING PROGRAM THRESHOLD VOLTAGE DISTRIBUTION OF A DUAL CELL MEMORY DEVICE	Spansion LLC	10/422090 4/24/03	6,822,909 11/23/04
NONVOLATILE MEMORY SYSTEM HAVING A PROGRAMMABLY SELECTABLE BOOT CODE SECTION SIZE	Spansion LLC	08/974971 11/20/97	6,823,435 11/23/04

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PHOTOSENSITIVE POLYMERIC MEMORY ELEMENTS	Spansion LLC	10/405272 4/2/03	6,825,060 11/30/04
METHOD FOR REDUCING SHALLOW TRENCH ISOLATION EDGE THINNING ON THIN GATE OXIDES TO IMPROVE PERIPHERAL TRANSISTOR RELIABILITY AND PERFORMANCE FOR HIGH PERFORMANCE FLASH MEMORY DEVICES	Spansion LLC	10/126814 4/19/02	6,825,083 11/30/04
STRUCTURE FOR INCREASING DRIVE CURRENT IN A MEMORY ARRAY AND RELATED METHOD	Spansion LLC	10/759809 1/16/04	6,825,526 11/30/04
MONOS DEVICE HAVING BURIED METAL SILICIDE BIT LINE	Spansion LLC	10/022,798 12/20/2001	6,828,199 12/7/2004
DISCONTINUOUS NITRIDE STRUCTURE FOR NONVOLATILE TRANSISTORS	Spansion LLC	10/315458 12/9/02	6,828,607 12/7/04
FLOATING GATE MEMORY DEVICE WITH HOMOGENEOUS OXYNITRIDE TUNNELING DIELECTRIC	Spansion LLC	10/232487 8/30/02	6,828,623 12/7/04
METHOD FOR REDUCING DRAIN INDUCED BARRIER LOWERING IN A MEMORY DEVICE	Spansion LLC	10/265001 10/4/02	6,833,297 12/21/04
STRUCTURE AND METHOD FOR PREVENTING PROCESSINDUCED UV RADIATION DAMAGE IN A MEMORY CELL	Spansion LLC	10/460282 6/12/03	6,833,581 12/21/04
MEMORY DEVICE AND METHODS OF USING NEGATIVE GATE STRESS TO CORRECT OVERERASED MEMORY CELLS	Spansion LLC	10/863673 6/8/04	6,834,012 12/21/04
PARTIALLY DECOUPLED CORE AND PERIPHERY GATE MODULE PROCESS	Spansion LLC	10/619797 7/14/03	6,835,662 12/28/04
SYSTEM AND METHOD OF FORMING A PASSIVE LAYER BY A CMP PROCESS	Spansion LLC	10/284769 10/31/02	6,836,398 12/28/04
PARTIAL PAGE PROGRAMMING OF MULTI LEVEL FLASH	Spansion LLC	10/074495 2/11/02	6,836,432 12/28/04

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
MEMORY DEVICE WITH ACTIVE PASSIVE LAYERS	Spansion LLC	10/413841 4/15/03	6,838,720 1/4/05
CLOCKED BASED METHOD AND DEVICES FOR MEASURING VOLTAGEVARIABLE CAPACITANCES AND OTHER ONCHIP PARAMETERS	Spansion LLC	09/825027 4/2/01	6,838,869 1/4/05
NONVOLATILE SEMICONDUCTOR MEMORY DEVICE	Spansion Inc.	10/455,310 6/6/2003	6,839,279 1/4/
NEUTRON DETECTING DEVICE	Spansion LLC	10/728510 12/5/03	6,841,841 1/11/05
CONTROL OF MEMORY ARRAYS UTILIZING ZENER DIODELIKE DEVICES	Spansion LLC	10/287363 11/4/02	6,847,047 1/25/05
SELF ASSEMBLY OF CONDUCTING POLYMER FOR FORMATION OF POLYMER MEMORY CELL	Spansion LLC	10/677042 10/1/03	6,852,586 2/8/05
TWOSTEP SOURCE SIDE IMPLANT FOR IMPROVING SOURCE RESISTANCE AND SHORT CHANNEL EFFECT IN DEEP SUB0.18MUM FLASH MEMORY TECHNOLOGY	Spansion LLC	10/053256 1/18/02	6,852,594 2/8/05
SEMICONDUCTOR MEMORY ENABLING CORRECT SUBSTITUTION OF REDUNDANT CELL ARRAY	Spansion Inc.	10/658,428 9/10/2003	6,853,596 2/8/2005
METHOD OF FABRICATING A PLANAR STRUCTURE CHARGE TRAPPING MEMORY CELL ARRAY WITH RECTANGULAR GATES AND REDUCED BIT LINE RESISTANCE	Spansion LLC	10/463643 6/17/03	6,855,608 2/15/05
SEMICONDUCTOR MEMORY AND METHOD OF DRIVING THE SAME	Spansion Inc.	10/207,056 7/30/2002	6,856,552 2/15/2005
METHOD OF ALTERNATING GROUNDED/FLOATING POLY LINES TO MONITOR SHORTS	Spansion LLC	10/288871 11/5/02	6,858,450 2/22/05
MEMORY DEVICE WITH ACTIVE AND PASSIVE LAYERS	Spansion LLC	10/413818 4/15/03	6,858,481 2/22/05

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OXIDIZING PRETREATMENT OF ONO LAYER FOR FLASH MEMORY	Spansion LLC	10/010280 12/5/01	6,858,496 2/22/05
GROUND STRUCTURE FOR PAGE READ AND PAGE WRITE FOR FLASH MEMORY	Spansion LLC	10/264,387 10/4/2002	6,859,393 2/22/2005
TEST STRUCTURE FOR MEASURING EFFECT OF TRENCH ISOLATION ON OXIDE IN A MEMORY DEVICE	Spansion LLC	10/190420 7/3/02	6,859,748 2/22/05
FULLY ISOLATED DIELECTRIC MEMORY CELL STRUCTURE FOR A DUAL BIT NITRIDE STORAGE DEVICE AND PROCESS FOR MAKING SAME	Spansion LLC	10/631199 7/31/03	6,861,307 3/1/05
STRUCTURE AND METHOD FOR A TWOBIT MEMORY CELL	Spansion LLC	10/429140 5/3/03	6,861,696 3/1/05
MEMORY DEVICE HAVING A THIN TOP DIELECTRIC AND METHOD OF ERASING SAME	Spansion LLC	10/459102 6/11/03	6,862,221 3/1/05
METHOD AND SYSTEM FOR DETECTING TUNNEL OXIDE ENCROACHMENT ON A MEMORY DEVICE	Spansion LLC	10/217965 8/12/02	6,864,106 3/8/05
MEMORY DEVICE	Spansion LLC	10/414353 4/15/03	6,864,522 3/8/05
MEMORY CIRCUIT WITH REDUNDANT CONFIGURATION	Spansion Inc.	10/652,035 9/2/2003	6,865,133 3/8/2005
ORGANIC SPINON ANTIREFLECTIVE COATING OVER INORGANIC ANTIREFLECTIVE COATING	Spansion LLC	10/262221 9/30/02	6,867,063 3/15/05
METHOD OF MAKING A MEMORY CELL WITH POLISHED INSULATOR LAYER	Spansion LLC	09/430366 10/28/99	6,867,097 3/15/05
NITROGEN OXIDATION TO REDUCE ENCROACHMENT	Spansion LLC	10/284866 10/30/02	6,867,119 3/15/05
MEMORY DEVICE WITH REDUCED OPERATING VOLTAGE HAVING DIELECTRIC STACK	Spansion LLC	10/430604 5/6/03	6,868,014 3/15/05

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
METHOD AND STRUCTURE FOR PROTECTING NROM DEVICES FROM INDUCED CHARGE DAMAGE DURING DEVICE FABRICATION	Spansion LLC	10/701780 11/5/03	6,869,844 3/22/05
STACKED ORGANIC MEMORY DEVICES AND METHODS OF OPERATING AND FABRICATING	Spansion LLC	10/287612 11/4/02	6,870,183 3/22/05
NARROW BITLINE USING SAFIER FOR MIRRORBIT	Spansion LLC	10/755430 1/12/04	6,872,609 3/29/05
IMPLANT DAMAGE REMOVAL BY LASER THERMAL ANNEALING	Spansion LLC	10/378885 3/5/03	6,872,643 3/29/05
SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME	Spansion LLC	10/662810 9/16/03	6,873,022 3/29/05
METHOD AND SYSTEM FOR IMPROVING SHORT CHANNEL EFFECT ON A FLOATING GATE DEVICE	Spansion LLC	10/431322 5/6/03	6,878,589 4/12/05
PHOTOSENSITIVE POLYMERIC MEMORY ELEMENTS	Spansion LLC	10/951370 9/28/04	6,878,961 4/12/05
METHOD OF FABRICATING A FLASH MEMORY SEMICONDUCTOR DEVICE BY DETERMINING THE ACTIVE REGION WIDTH BETWEEN SHALLOW TRENCH ISOLATION STRUCTURES USING AN OVERDRIVE CURRENT MEASUREMENT TECHNIQUE AND A DEVICE THEREBY FABRICATED	Spansion LLC	10/225052 8/20/02	6,884,638 4/26/05
METHOD OF MANUFACTURING A SEMICONDUCTOR MEMORY WITH DEUTERATED MATERIALS	Spansion LLC	10/672,093 9/26/2003	6,884,681 4/26/2005
CASCODE AMPLIFIER CIRCUIT FOR GENERATING AND MAINTAINING A FAST, STABLE AND ACCURATE BIT LINE VOLTAGE	Spansion LLC	10/844116 5/12/04	6,885,250 4/26/05

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
MEMORY DEVICE HAVING A P+ GATE AND THIN BOTTOM OXIDE AND METHOD OF ERASING SAME	Spansion LLC	10/341881 1/14/03	6,885,590 4/26/05
NGATE/NSUBSTRATE OR PGATE/PSUBSTRATE CAPACITOR TO CHARACTERIZE POLYSILICON GATE DEPLETION EVALUATION	Spansion LLC	09/917440 7/27/01	6,888,157 5/3/05
COMPENSATED OSCILLATOR CIRCUIT FOR CHARGE PUMPS	Spansion LLC	10/358498 2/4/03	6,888,763 5/3/05
SYSTEM AND METHOD FOR ERASE VOLTAGE CONTROL DURING MULTIPLE SECTOR ERASE OF A FLASH MEMORY DEVICE	Spansion LLC	10/210378 7/31/02	6,891,752 5/10/05
LOAD/STORE MICROPACKET HANDLING SYSTEM	Spansion LLC	09/915109 7/25/01	6,892,298 5/10/05
CUS FORMATION BY ANODIC SULFIDE PASSIVATION OF COPPER SURFACE	Spansion LLC	10/885944 7/7/04	6,893,895 5/17/05
STRUCTURE AND METHOD FOR PREVENTING UV RADIATION DAMAGE IN A MEMORY CELL AND IMPROVING CONTACT CD CONTROL	Spansion LLC	10/460278 6/12/03	6,894,342 5/17/05
FAST BANDGAP REFERENCE CIRCUIT FOR USE IN A LOW POWER SUPPLY A/D BOOSTER	Spansion LLC	10/379744 3/5/03	6,894,473 5/17/05
FLASH MEMORY CELL PROGRAMMING METHOD AND SYSTEM	Spansion LLC	10/342585 1/14/03	6,894,925 5/17/05
DUAL CELL MEMORY DEVICE HAVING A TOP DIELECTRIC STACK	Spansion LLC	10/716230 11/18/03	6,894,932 5/17/05
METHOD OF PROTECTING A MEMORY ARRAY FROM CHARGE DAMAGE DURING FABRICATION	Spansion LLC	10/305750 11/26/02	6,897,110 5/24/05

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TEST STRUCTURE FOR DETERMINING ELECTROMIGRATION AND INTERLAYER DIELECTRIC FAILURE	Spansion LLC	10/636162 8/7/03	6,897,476 5/24/05
FLASH MEMORY CELL HAVING REDUCED LEAKAGE CURRENT	Spansion LLC	10/618191 7/10/03	6,897,518 5/24/05
A MULTIBIT SILICON NITRIDE CHARGETRAPPING NONVOLATILE MEMORY CELL	Spansion LLC	10/247641 9/18/02	6,897,533 5/24/05
EFFICIENT AND ACCURATE SENSING CIRCUIT AND TECHNIQUE FOR LOW VOLTAGE FLASH MEMORY DEVICES	Spansion LLC	10/678446 10/3/03	6,898,124 5/24/05
ESD IMPLANT FOLLOWING SPACER DEPOSITION	Spansion LLC	09/891885 6/26/01	6,900,085 5/31/05
PATTERNING FOR ELONGATED VSS CONTACT ON FLASH MEMORY	Spansion LLC	10/654739 9/3/03	6,900,124 5/31/05
MULTICELL ORGANIC MEMORY ELEMENT AND METHODS OF OPERATING AND FABRICATING	Spansion LLC	10/284946 10/31/02	6,900,488 5/31/05
ERASE METHOD FOR A DUAL BIT MEMORY CELL	Spansion LLC	10/119366 4/8/02	6,901,010 5/31/05
NON VOLATILE CHARGE TRAPPING DIELECTRIC MEMORY CELL STRUCTURE WITH GATE HOLE INJECTION ERASE	Spansion LLC	10/684890 10/14/03	6,903,407 6/7/05
TREATMENT OF DIELECTRIC MATERIAL TO ENHANCE ETCH RATE	Spansion LLC	10/331938 12/30/02	6,905,971 6/14/05
METHOD AND SYSTEM FOR ERASING A NITRIDE MEMORY DEVICE	Spansion LLC	10/306252 11/27/02	6,906,959 6/14/05
METHOD FOR FORMING A DIELECTRIC SPACER IN A NONVOLATILE MEMORY DEVICE	Spansion LLC	10/696234 10/28/03	6,908,816 6/21/05
MEMORY CELL ARRAY WITH STAGGERED LOCAL INTERCONNECT STRUCTURE	Spansion LLC	10/685044 10/14/03	6,911,704 6/28/05

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NONVOLATILE SEMICONDUCTOR MEMORY DEVICE	Spansion Inc.	10/387,064 3/11/2003	6,912,160 6/28/2005
MEMORY DEVICE HAVING HIGH WORK FUNCTION GATE AND METHOD OF ERASING SAME	Spansion LLC	10/658,506 9/9/2003	6,912,163 6/28/2005
NONVOLATILE SEMICONDUCTOR MEMORY THAT IS BASED ON A VIRTUAL GROUND METHOD	Spansion Inc.	10/392,912 3/21/2003	6,914,824 7/5/2005
SEMICONDUTOR DEVICE HAVING CONDUCTIVE STRUCTURES FORMED NEAR A GATE ELECTRODE	Spansion LLC	10/454517 6/5/03	6,917,068 7/12/05
METHOD OF FABRICATING A FLOATING GATE	Spansion LLC	10/655936 9/4/03	6,919,247 7/19/05
NARROW WIDE SPACER	Spansion LLC	10/821312 4/8/04	6,927,129 8/9/05
SEMICONDUCTOR MEMORY CAPABLE OF BEING DRIVEN AT LOW VOLTAGE AND ITS MANUFACTURE METHOD	Spansion Inc.	10/649,994 8/28/2003	6,927,133 8/9/2005
BITLINE HARD MASK SPACER FLOW FOR MEMORY CELL SCALING	Spansion LLC	10/770673 2/2/04	6,927,145 8/9/05
TIGHTLY SPACED GATE FORMATION THROUGH DAMASCENE PROCESS	Spansion LLC	10/716209 11/18/03	6,933,219 8/23/05
RECESSED TUNNEL OXIDE PROFILE FOR IMPROVED RELIABILITY IN NAND DEVICES	Spansion LLC	09/904042 7/11/01	6,933,554 8/23/05
FLASH MEMORY DEVICE	Spansion LLC	10/726508 12/4/03	6,933,558 8/23/05
RAMP SOURCE HOTHOLE PROGRAMMING FOR TRAP BASED NONVOLATILE MEMORY DEVICES	Spansion LLC	10/863933 6/9/04	6,934,190 8/23/05
NONVOLATILE MEMORY HAVING A TRAP LAYER	Spansion Inc.	10/631,812 8/1/2003	6,934,194 8/23/2005

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
MEMORY DEVICE HAVING REVERSE LDD	Spansion LLC	10/387,774 3/12/2003	6,936,515 8/30/2005
ORGANIC MEMORY CELL FORMATION ON AG SUBSTRATE	Spansion LLC	10/676612 10/1/03	6,936,545 8/23/05
PROGRAMMING OF A FLASH MEMORY CELL	Spansion LLC	10/617971 7/10/03	6,937,518 8/30/05
METHOD FOR FABRICATING A FLASH MEMORY DEVICE	Spansion LLC	10/616804 7/9/03	6,939,766 9/6/05
METHOD OF FABRICATING SEMICONDUCTOR DEVICE HAVING TRIPLE LDD STRUCTURE AND LOWER GATE RESISTANCE FORMED WITH A SINGLE IMPLANT PROCESS	Spansion LLC	10/618514 7/11/03	6,939,770 9/6/05
NONVOLATILE SEMICONDUCTOR MEMORY DEVICE AND METHOD OF FABRICATING THEREOF	Spansion Inc.	10/437,896 5/15/2003	6,940,120 9/6/2005
CONTROL OF MEMORY ARRAYS UTILIZING ZENER DIODELIKE DEVICES	Spansion LLC	10/882538 6/30/04	6,943,370 9/13/05
A FLASH MEMORY CELL WITH DRAIN AND SOURCE FORMED BY DIFFUSION OF A DOPANT FROM A SILICIDE	Spansion LLC	10/661720 9/11/03	6,943,401 9/13/05
METHOD TO OBTAIN TEMPERATURE INDEPENDENT PROGRAM THRESHOLD VOLTAGE DISTRIBUTION USING TEMPERATURE DEPENDENT VOLTAGE REFERENCE	Spansion LLC	10/431,065 5/6/2003	6,944,057 9/13/2005
METHOD OF FORMATION OF SEMICONDUCTOR RESISTANT TO HOT CARRIER INJECTION STRESS	Spansion LLC	10/359,872 2/7/2003	6,949,433 9/27/2005
PROCESS FOR FABRICATION OF SPACER LAYER WITH REDUCED HYDROGEN CONTENT IN SEMICONDUCTOR DEVICE	Spansion LLC	10/731,494 12/9/2003	6,949,481 9/27/2005

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
NONVOLATILE SEMICONDUCTOR MEMORY DEVICE STORING TWOBIT INFORMATION	Spansion Inc.	10/717,622 11/21/2003	6,950,343 9/27/2005
READING FLASH MEMORY	Spansion LLC	10/721643 11/24/03	6,950,344 9/27/05
REDUCED SILICON GOUGING AND COMMON SOURCE LINE RESISTANCE IN SEMICONDUCTOR DEVICES	Spansion LLC	10/358756 2/5/03	6,953,752 10/11/05
MEMORY ELEMENT FORMATION WITH PHOTOSENSITIVE POLYMER DIELECTRIC	Spansion LLC	10/700021 11/3/03	6,955,939 10/18/05
PROCESS FOR FABRICATION OF NITRIDE LAYER WITH REDUCED HYDROGEN CONTENT IN ONO STRUCTURE IN SEMICONDUCTOR DEVICE	Spansion LLC	10/731,659 12/9/2003	6,955,965 10/18/2005
METHOD OF PROGRAMMING DUAL CELL MEMORY DEVICE TO STORE MULTIPLE DATA STATES PER CELL	Spansion LLC	10/413800 4/15/03	6,956,768 10/18/05
SIMULTANEOUS EXECUTION COMMAND MODES IN A FLASH MEMORY DEVICE	Spansion LLC	10/603136 6/23/03	6,957,297 10/18/05
A METHOD OF FABRICATING A DUALLEVEL STACKED FLASH MEMORY CELL WITH A MOSFET STORAGE TRANSISTOR	Spansion LLC	10/634042 8/4/03	6,958,271 10/25/05
POCKET IMPLANT FOR COMPLEMENTARY BIT DISTURB IMPROVEMENT AND CHARGING IMPROVEMENT OF SONOS MEMORY CELL	Spansion LLC	10/755740 1/12/04	6,958,272 10/25/05
FLASH MEMORY DEVICE AND METHOD OF FABRICATION THEREOF INCLUDING A BOTTOM OXIDE LAYER WITH TWO REGIONS WITH DIFFERENT CONCENTRATIONS OF NITROGEN	Spansion LLC	10/679,774 10/6/2003	6,958,511 10/25/2005

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
NON VOLATILE MEMORY DEVICE	Spansion LLC	10/770010 2/3/04	6,958,512 10/25/05
ERASING AND PROGRAMMING AN ORGANIC MEMORY DEVICE AND METHOD OF FABRICATING	Spansion LLC	10/436786 5/13/03	6,960,783 11/1/05
METHOD AND DEVICE FOR PROGRAMMING CELLS IN A MEMORY ARRAY IN A NARROW DISTRIBUTION	Spansion LLC	10/738,301 12/16/2003	6,961,267 11/1/2005
OPTICAL DISK HAVING SYNCHRONIZATION REGION FORMED BETWEEN PRERECORDED AREA AND RECORDABLE AREA	Spansion LLC	10/221682 9/13/02	6,961,301 11/1/05
HARD MASK SPACER FOR SUBLITHOGRAPHIC BITLINE	Spansion LLC	10/729732 12/5/03	6,962,849 11/8/05
NONVOLATILE MEMORY DEVICE	Spansion LLC	10/459576 6/12/03	6,963,104 11/8/05
MEMORY ARRAY WITH MEMORY CELLS HAVING REDUCED SHORT CHANNEL EFFECTS	Spansion LLC & FASL LLC	10/839626 5/4/04	6,963,106 11/8/05
RECESSED CHANNEL	Spansion LLC	10/683631 10/10/03	6,963,108 11/8/05
CIRCUIT AND TECHNIQUE FOR ACCURATELY SENSING LOW VOLTAGE FLASH MEMORY DEVICES	Spansion LLC	10/679179 10/10/03	6,963,506 11/8/05
RECESS CHANNEL FLASH ARCHITECTURE FOR REDUCED SHORT CHANNEL EFFECT	Spansion LLC	10/683649 10/10/03	6,965,143 11/15/05
SEMICONDUCTOR MEMORY DEVICE AND SEMICONDUCTOR MEMORY DEVICE CONTROL METHOD	Spansion Inc.	11/029,454 1/6/2005	6,965,530 11/15/2005
SYSTEM AND METHOD FOR ERASE TEST OF INTEGRATED CIRCUIT DEVICE HAVING NONHOMOGENEOUSLY SIZED SECTORS	Spansion LLC	09/836065 4/16/01	6,966,016 11/15/05

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MEMORY DEVICE AND METHOD USING POSITIVE GATE STRESS TO RECOVER OVERERASED CELL	Spansion LLC	10/677790 10/2/03	6,967,873 11/22/05
FLASH NVROM DEVICES WITH UV CHARGE IMMUNITY	Spansion LLC	09/727714 11/28/00	6,969,654 11/29/05
METHOD OF MANUFACTURING A MEMORY INTEGRATED CIRCUIT DEVICE	Spansion Inc.	10/650,072 8/28/2003	6,969,663 11/29/2005
ONO FABRICATION PROCESS FOR REDUCING OXYGEN VACANCY CONTENT IN BOTTOM OXIDE LAYER IN FLASH MEMORY DEVICES	Spansion LLC	10/889,424 7/12/2004	6,969,886 11/29/2005
SEMICONDUCTOR DEVICE LOW TEMPERATURE TEST APPARATUS USING ELECTRONIC COOLING ELEMENT	Spansion Inc.	10/404,081 4/2/2003	6,970,007 11/29/2005
CAM (CONTENT ADDRESSABLE MEMORY) CELLS AS PART OF CORE ARRAY IN FLASH MEMORY DEVICE	Spansion LLC	10/650049 8/26/03	6,970,368 11/29/05
SEMICONDUCTOR MEMORY	Spansion Inc.	10/747,692 12/30/2003	6,970,381 11/29/2005
METHOD AND SYSTEM FOR TESTING ARTICLES OF MANUFACTURE	Spansion LLC	10/703860 11/7/03	6,970,806 11/29/05
MEMORY DEVICE AND METHOD	Spansion LLC	10/677073 10/1/03	6,973,003 12/6/05
STRUCTURE AND METHOD FOR PROTECTING MEMORY CELLS FROM UV RADIATION DAMAGE AND UV RADIATIONINDUCED CHARGING DURING BACKEND PROCESSING	Spansion LLC & FASL LLC	10/841933 5/6/04	6,974,989 12/13/05
METHOD AND SYSTEM FOR FORMING DUAL GATE STRUCTURES IN A NONVOLATILE MEMORY USING A PROTECTIVE LAYER	Spansion LLC & FASL LLC	10/032757 12/27/01	6,974,995 12/13/05

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
TEST STRUCTURE FOR CHARACTERIZING JUNCTION LEAKAGE CURRENT	Spansion LLC	10/919,119 8/16/2004	6,977,195 12/20/2005
PLANAR POLYMER MEMORY DEVICE	Spansion LLC	10/452877 6/2/03	6,977,389 12/20/05
FLASH MEMORY DEVICE AND A METHOD OF FABRICATION THEREOF	Spansion LLC	09/941370 8/28/01	6,979,619 12/27/05
STACKED ORGANIC MEMORY DEVICES AND METHODS OF OPERATING AND FABRICATING	Spansion LLC	10/848679 5/19/04	6,979,837 12/27/05
MEMORY DEVICE AND METHOD	Spansion LLC	10/677031 10/1/03	6,980,473 12/27/05
POST CMP PRECURSOR TREATMENT	Spansion LLC	10/726829 12/3/03	6,982,188 1/3/06
FLOATING GATE SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE	Spansion LLC	10/883,924 7/1/2004	6,984,563 1/10/2006
MEMORY DEVICE HAVING SILICIDED BITLINES AND METHOD OF FORMING THE SAME	Spansion LLC	10/635781 8/6/03	6,987,048 1/17/06
SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURING METHOD THEREOF	Spansion Inc.	10/768,188 2/2/2004	6,987,297 1/17/2006
METHOD OF IMPROVING ERASE VOLTAGE DISTRIBUTION FOR A FLASH MEMORY ARRAY HAVING DUMMY WORDLINES	Spansion LLC	10/885268 7/6/04	6,987,696 1/17/06
METHODS FOR FORMING NITROGENRICH REGIONS IN NONVOLATILE SEMICONDUCTOR MEMORY DEVICES	Spansion LLC	10/718707 11/24/03	6,989,319 1/24/06
BITLINE IMPLANT UTILIZING DUAL POLY	Spansion LLC	10/843289 5/11/04	6,989,320 1/24/06
FLASH MEMORY CELL WITH UV PROTECTIVE LAYER	Spansion LLC	10/770260 2/2/04	6,989,563 1/24/06

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
METHOD FOR ERROR DETECTION/CORRECTION OF MULTILEVEL CELL MEMORY AND MULTILEVEL CELL MEMORY HAVING ERROR DETECTION/CORRECTION FUNCTION	Spansion Inc.	10/146,074 5/16/2002	6,990,623 1/24/2006
METHOD FOR PRODUCING A LOW DEFECT HOMOGENEOUS OXYNITRIDE	Spansion LLC	10/306382 11/27/02	6,991,987 1/31/06
MEMORY CELL STRUCTURE HAVING NITRIDE LAYER WITH REDUCED CHARGE LOSS AND METHOD FOR FABRICATING SAME	Spansion LLC	10/655179 9/4/03	6,992,370 1/31/06
SEMICONDUCTOR MANUFACTURING RESOLUTION ENHANCEMENT SYSTEM AND METHOD FOR SIMULTANEOUSLY PATTERNING DIFFERENT FEATURE TYPES	Spansion LLC	10/283685 10/29/02	6,994,939 2/7/06
MEMORY DEVICE HAVING A P+ GATE AND THIN BOTTOM OXIDE AND METHOD OF ERASING SAME	Spansion LLC	10/878091 6/28/04	6,995,423 2/7/06
SEMICONDUCTOR DEVICE WITH CORE AND PERIPHERY REGIONS	Spansion LLC	10/869774 6/16/04	6,995,437 2/7/06
MINIMIZATION OF FGFG COUPLING IN FLASH MEMORY	Spansion LLC	10/700414 11/4/03	6,996,004 2/7/06
SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE	Spansion LLC	10/795924 3/8/04	6,998,677 2/14/06
FULLY ISOLATED DIELECTRIC MEMORY CELL STRUCTURE FOR A DUAL BIT NITRIDE STORAGE DEVICE AND PROCESS FOR MAKING SAME	Spansion LLC	10/997345 11/24/04	7,001,807 2/21/06
LASER THERMAL ANNEALING METHODS FOR FLASH MEMORY DEVICES	Spansion LLC	10/438942 5/16/03	7,001,814 2/21/06

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
SWITCHEDCAPACITOR CONTROLLER TO CONTROL THE RISE TIMES OF ONCHIP GENERATED HIGH VOLTAGES	Spansion LLC	10/015033 12/11/01	7,002,381 2/21/06
MEMORY DEVICE WITH AN ALTERNATING VSS INTERCONNECTION	Spansion LLC	10/823972 4/13/04	7,009,271 3/7/06
METHOD OF DETERMINING VOLTAGE COMPENSATION FOR FLASH MEMORY DEVICES	Spansion LLC	10/860,450 6/3/2004	7,009,887 3/7/2006
ADDRESS SEQUENCER WITHIN BIST (BUILTINSELFTEST) SYSTEM	Spansion LLC	10/200518 7/22/02	7,010,736 3/7/06
HIGH VOLTAGE TRANSISTOR SCALING TILT ION IMPLANT METHOD	Spansion LLC	10/756573 1/12/04	7,011,998 3/14/06
DUAL SPACER PROCESS FOR NONVOLATILE MEMORY DEVICES	Spansion LLC	09/728554 12/1/00	7,012,008 3/14/06
DIELECTRIC PATTERN FORMATION FOR ORGANIC ELECTRONIC DEVICES	Spansion LLC	10/726868 12/3/03	7,012,013 3/14/06
NONVOLATILE MEMORY DEVICE	Spansion LLC	10/211317 8/5/02	7,012,298 3/14/06
NONVOLATILE SEMICONDUCTOR MEMORY DEVICE SUPPLYING PROPER PROGRAM POTENTIAL	Spansion Inc.	10/631,856 8/1/2003	7,012,838 3/14/2006
METHOD FOR REDUCING ANTIREFLECTIVE COATING LAYER REMOVAL DURING REMOVAL OF PHOTORESIST	Spansion LLC	10/079775 2/19/02	7,015,134 3/21/06
METHOD AND SYSTEM FOR REDUCING CONTACT DEFECTS USING NON CONVENTIONAL CONTACT FORMATION METHOD FOR SEMICONDUCTOR CELLS	Spansion LLC	10/316569 12/10/02	7,015,135 3/21/06
SIDEWALL FORMATION FOR HIGH DENSITY POLYMER MEMORY ELEMENT ARRAY	Spansion LLC	10/699903 11/3/03	7,015,504 3/21/06
DISPOSABLE HARD MASK FOR MEMORY BITLINE SCALING	Spansion LLC	10/770245 2/2/04	7,018,868 3/28/06

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
UVBLOCKING LAYER FOR REDUCING UVINDUCED CHARGING OF SONOS DUALBIT FLASH MEMORY DEVICES IN BEOL PROCESSING	Spansion LLC	10/818112 4/5/04	7,018,896 3/28/06
PATTERNING FOR ELONGATED VSS CONTACT FLASH MEMORY	Spansion LLC	10/968713 10/19/04	7,018,922 3/28/06
ELECTROSTATIC DISCHARGE PERFORMANCE OF A SILICON STRUCTURE AND EFFICIENT USE OF AREA WITH ELECTROSTATIC DISCHARGE PROTECTIVE DEVICE UNDER THE PAD APPROACH AND ADJUSTMENT OF VIA CONFIGURATION THERETO TO CONTROL DRAIN JUNCTION RESISTANCE	Spansion LLC	10/758,173 1/14/2004	7,019,366 3/28/2006
RAMPED SOFT PROGRAMMING FOR CONTROL OF ERASE VOLTAGE DISTRIBUTIONS IN FLASH MEMORY DEVICES	Spansion LLC	10/981833 11/4/04	7,020,021 3/28/06
METHOD OF REFERENCE CELL DESIGN FOR OPTIMIZED MEMORY CIRCUIT YIELD	Spansion LLC	10/887782 7/9/04	7,020,022 3/28/06
UNDOPED OXIDE LINER/BPSG FOR IMPROVED DATA RETENTION	Spansion LLC	10/617450 7/11/03	7,023,046 4/4/06
SUBSTRATE BIAS FOR PROGRAMMING NONVOLATILE MEMORY	Spansion LLC	10/755979 1/12/04	7,023,740 4/4/06
SEMICONDUCTOR COMPONENT AND METHOD OF MANUFACTURE	Spansion LLC	10/795,890 3/8/2004	7,026,211 4/11/2006
METHOD FOR FABRICATING A MEMORY DEVICE	Spansion LLC	10/662011 9/11/03	7,026,230 4/11/06
MEMORY DEVICE	Spansion LLC	10/776850 2/11/04	7,026,702 4/11/06
NONVOLATILE SEMICONDUCTOR MEMORY AND METHOD OF MANUFACTURING THE SAME	Spansion Inc.	10/387,427 3/14/2003	7,026,687 4/11/2006

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
FLEXIBLE CASCODE AMPLIFIER CIRCUIT WITH HIGH GAIN FOR FLASH MEMORY CELLS	Spansion LLC	10/759855 1/16/04	7,026,843 4/11/06
DIAGNOSTIC MODE FOR TESTING FUNCTIONALITY OF BIST (BUILTINSELFTEST) BACKEND STATE MACHINE	Spansion LLC	10/200526 7/22/02	7,028,240 4/11/06
METHOD AND APPARATUS FOR ELIMINATING WORD LINE BENDING BY SOURCE SIDE IMPLANTATION	Spansion LLC	10/839561 5/4/04	7,029,975 4/18/06
DIFFERENTIALLY MISALIGNED CONTACTS IN FLASH ARRAYS TO CALIBRATE FAILURE MODES	Spansion LLC	10/320910 12/17/02	7,032,193 4/18/06
ONO FABRICATION PROCESS FOR INCREASING OXYGEN CONTENT AT BOTTOM OXIDESUBSTRATE INTERFACE IN FLASH MEMORY DEVICES	Spansion LLC	10/358,586 2/5/2003	7,033,957 4/25/2006
DIODE ARRAY ARCHITECTURE FOR ADDRESSING NANOSCALE RESISTIVE MEMORY ARRAYS	Spansion LLC	10/990706 11/17/04	7,035,141 4/25/06
SEMICONDUCTOR MEMORY DEVICE AND METHOD OF FABRICATING THE SAME	Spansion LLC	10/714909 11/18/03	7,037,780 5/2/06
READ APPROACH FOR MULTILEVEL VIRTUAL GROUND MEMORY	Spansion LLC & FASL LLC	10/946809 9/22/04	7,038,948 5/2/06
MULTI BIT PROGRAM ALGORITHM	Spansion LLC	10/982296 11/5/04	7,038,950 5/2/06
METHOD OF PROGRAMMING A FLASH MEMORY DEVICE USING MULTILEVEL CHARGE STORAGE	Spansion LLC & FASL, LLC	10/896651 7/22/04	7,042,766 5/9/06
FLASH MEMORY UNIT AND METHOD OF PROGRAMMING A FLASH MEMORY DEVICE	Spansion LLC	10/909693 8/2/04	7,042,767 5/9/06
CURRENTVOLTAGE CONVERTER CIRCUIT AND ITS CONTROL METHOD	Spansion LLC	11/061119 2/18/05	7,046,043 5/16/06
LATERAL DOPED CHANNEL	Spansion LLC	10/305724 11/26/02	7,049,188 5/23/06

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
METHOD FOR FORMING WORDLINES HAVING IRREGULAR SPACING IN A MEMORY ARRAY	Spansion LLC & Globalfoundries Inc.	11/003574 12/3/04	7,052,961 5/30/06
METHOD FOR SEMICONDUCTOR WAFER PLANARIZATION BY ISOLATION MATERIAL GROWTH	Spansion LLC	10/190002 7/3/02	7,052,969 5/30/06
MEMORY DEVICE WITH BARRIER LAYER	Spansion LLC	11/194471 8/2/05	7,053,445 5/30/06
MEMORY WORDLINE SPACER	Spansion LLC	10/864142 6/8/04	7,053,446 5/30/06
METHOD AND APPARATUS FOR PRECHARGING NEGATIVE PUMP MOS REGULATION CAPACITORS	Spansion LLC	10/050342 1/16/02	7,057,949 6/6/06
PECVD SILICONRICH OXIDE LAYER FOR REDUCED UV CHARGING	Spansion LLC	10/617451 7/11/03	7,060,554 6/13/06
MEMORY DEVICE AND METHOD OF SIMULTANEOUS FABRICATION OF CORE AND PERIPHERY OF SAME	Spansion LLC	10/635089 8/6/03	7,060,564 6/13/06
NONVOLATILE SEMICONDUCTOR MEMORY DEVICE INCLUDING A PLURALITY OF BLOCKS AND A SENSING CIRCUIT PROVIDED IN EACH OF THE BLOCKS FOR COMPARING DATA WITH A REFERENCE SIGNAL HAVING A LOAD IMPOSED THEREON	Spansion Inc.	10/633,535 8/5/2003	7,061,809 6/13/2006
SEMICONDUCTOR MEMORY STORAGE DEVICE AND ITS REDUNDANT METHOD	Spansion LLC	11/061365 2/18/05	7,061,816 6/13/06
METHODS OF DETERMINING CHARACTERISTICS OF DOPED REGIONS ON DEVICE WAFERS, AND SYSTEM FOR ACCOMPLISHING SAME	Spansion LLC & Globalfoundries Inc.	10/900832 7/28/04	7,063,991 6/20/06
ION PATH POLYMERS FOR IONMOTION MEMORY	Spansion LLC	10/968705 10/19/04	7,067,349 6/27/06
RECESSED CHANNEL WITH SEPARATED ONO MEMORY DEVICE	Spansion LLC	10/812,703 3/30/2004	7,067,377 6/27/2006

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
STRUCTURE AND METHOD TO REDUCE DRAIN INDUCED BARRIER LOWERING	Spansion LLC	10/636336 8/6/03	7,067,381 6/27/06
FLASH MEMORY DEVICE AND METHOD OF FORMING THE SAME WITH IMPROVED GATE BREAKDOWN AND ENDURANCE	Spansion LLC	10/819162 4/7/04	7,067,388 6/27/06
SYSTEM THAT FACILITATES READING MULTILEVEL DATA IN NONVOLATILE MEMORY	Spansion LLC & FASL LLC	10/951410 9/28/04	7,068,204 6/27/06
SEMICONDUCTOR MEMORY STORAGE DEVICE AND A REDUNDANCY CONTROL METHOD THEREFOR	Spansion LLC	11/061307 2/18/05	7,068,555 6/27/06
STRUCTURE AND METHOD FOR REDUCING STANDING WAVES IN A PHOTORESIST	Spansion LLC	10/350472 1/23/03	7,070,911 7/4/06
ONE STACK WITH STEAM OXIDE FOR CHARGE RETENTION	Spansion L.L.C.	11/008263 12/10/04	7,071,538 7/4/06
ARCHITECTURE FOR GENERATING ADAPTIVE ARBITRARY WAVEFORMS	Spansion LLC	10/885,284 7/6/2004	7,072,781 7/4/2006
METHOD AND SYSTEM FOR APPLYING TESTING VOLTAGE SIGNAL	Spansion LLC	10/384856 3/10/03	7,073,104 7/4/06
MEMORY WITH IMPROVED CHARGETRAPPING DIELECTRIC LAYER	Spansion LLC	10/307,189 11/29/2002	7,074,677 7/11/2006
METHOD AND SYSTEM FOR DEFINING A REDUNDANCY WINDOW AROUND A PARTICULAR COLUMN IN A MEMORY ARRAY	Spansion LLC	10/305700 11/26/02	7,076,703 7/11/06
MEMORY DEVICE HAVING IMPROVED PERIPHERY AND CORE ISOLATION	Spansion LLC	10/407999 4/3/03	7,078,314 7/18/06
MEMORY STRUCTURE HAVING TUNABLE INTERLAYER DIELECTRIC AND METHOD FOR FABRICATING SAME	Spansion LLC	10/618156 7/11/03	7,078,749 7/18/06

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
METHOD FOR PROGRAMMING DUAL BIT MEMORY DEVICES TO REDUCE COMPLEMENTARY BIT DISTURBANCE	Spansion LLC	10/896,299 7/20/2004	7,079,423 7/18/2006
METHODS AND SYSTEMS FOR REDUCING ERASE TIMES IN FLASH MEMORY DEVICES	Spansion L.L.C.	10/945914 9/22/04	7,079,424 7/18/06
VOLTAGE DETECTION CIRCUIT, SEMICONDUCTOR DEVICE, METHOD FOR CONTROLLING VOLTAGE DETECTION CIRCUIT	Spansion LLC & Fujitsu Limited	11/057143 2/15/05	7,081,776 7/25/06
FLASH MEMORY HAVING SPARE SECTOR WITH SHORTENED ACCESS TIME	Spansion LLC & Fujitsu Limited	11/170183 6/30/05	7,082,066 7/25/06
CONTROL METHOD OF SEMICONDUCTOR MEMORY DEVICE AND SEMICONDUCTOR MEMORY DEVICE	Spansion LLC & Fujitsu Limited	10/635431 8/7/03	7,082,077 7/25/06
SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME	Spansion Inc.	10/986,652 11/12/2004	7,084,037 8/1/2006
USE OF TACAPPED METAL LINE TO IMPROVE FORMATION OF MEMORY ELEMENT FILMS	Spansion LLC & Globalfoundries Inc.	11/033653 1/12/05	7,084,062 8/1/06
A SEMICONDUCTOR DEVICE HAVING TRIPLE LDD STRUCTURE AND LOWER GATE RESISTANCE FORMED WITH A SINGLE IMPLANT PROCESS	Spansion LLC	11/120690 5/2/05	7,084,458 8/1/06
UVBLOCKING ETCH STOP LAYER FOR REDUCING UVINDUCED CHARGING OF CHARGE STORAGE LAYER IN MEMORY DEVICES IN BEOL PROCESSING	Spansion LLC	10/861437 6/3/04	7,091,088 8/15/06
METHOD FOR PULSE ERASE IN DUAL BIT MEMORY DEVICES	Spansion LLC	10/899,684 7/26/2004	7,092,297 8/15/2006
MEMORY CONTROLLER FOR MULTILEVEL CELL MEMORY	Spansion LLC & Fujitsu Limited	10/097499 3/15/02	7,096,406 8/22/06

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
ALIGNMENT MARKS WITH SALICIDED SPACERS BETWEEN BITLINES FOR ALIGNMENT SIGNAL IMPROVEMENT	Spansion LLC	10/869,286 6/16/2004	7,098,546 8/29/2006
SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE	Spansion LLC	10/643967 8/20/03	7,098,147 8/29/06
CURRENT SENSING CIRCUIT WITH A CURRENTCOMPENSATED DRAIN VOLTAGE REGULATION	Spansion LLC	11/087944 3/23/05	7,099,204 8/29/06
MEMORY ELEMENTS USING ORGANIC ACTIVE LAYER	Spansion LLC & Globalfoundries Inc.	11/021681 12/23/04	7,102,156 9/5/06
SEMICONDUCTOR MEMORY APPARATUS	Spansion Inc.	10/304,762 11/27/2002	7,102,928 9/5/2006
SYSTEM AND METHOD FOR MULTIBIT FLASH READS USING DUAL DYNAMIC REFERENCES	Spansion LLC	10/933588 9/3/04	7,103,706 9/5/06
MEMORY CELL CONTAINING COPOLYMER CONTAINING DIARYLACETYLENE PORTION	Spansion LLC	11/033941 1/12/05	7,105,374 9/12/06
SEMICONDUCTOR MEMORY DEVICE AND METHOD OF READING DATA FROM SEMICONDUCTOR MEMORY DEVICE	Spansion LLC & Fujitsu Limited	11/066484 2/28/05	7,106,651 9/12/06
INTEGRATED CIRCUIT TEST SOCKET	Spansion LLC	11/180943 7/12/05	7,108,535 9/19/06
METHOD FOR PROVIDING SHORT CHANNEL EFFECT CONTROL USING A SILICIDE VSS LINE	Spansion LLC	10/835341 4/28/04	7,109,555 9/19/06
QUAD BIT USING HOTHOLE ERASE FOR CBD CONTROL	Spansion LLC	11/091982 3/29/05	7,113,431 9/26/06
NONVOLATILE SEMICONDUCTOR MEMORY, SEMICONDUCTOR DEVICE AND CHARGE PUMP CIRCUIT	Spansion LLC	11/126701 5/11/05	7,113,442 9/26/06

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
SO2 TREATMENT OF OXIDIZED CUO FOR COPPER SULFIDE FORMATION OF MEMORY ELEMENT GROWTH	Spansion LLC	10/957247 10/1/04	7,115,440 10/3/06
INTEGRATED ONO PROCESSING FOR SEMICONDUCTOR DEVICES USING INSITU STEAM GENERATION (ISSG) PROCESS	Spansion LLC	10/754948 1/8/04	7,115,469 10/3/06
LOW POWER CHARGE PUMP	Spansion LLC	10/636337 8/6/03	7,116,154 10/3/06
PROTECTION OF CHARGE TRAPPING DIELECTRIC FLASH MEMORY DEVICES FROM UVINDUCED CHARGING IN BEOL PROCESSING	Spansion LLC	10/368696 2/19/03	7,118,967 10/10/06
METHOD AND APPARATUS FOR SETTING OPERATIONAL INFORMATION OF A NONVOLATILE MEMORY	Spansion LLC	11/259873 10/26/05	7,120,050 10/10/06
FLASH MEMORY CELL AND METHODS FOR PROGRAMMING AND ERASING	Spansion LLC	10/841850 5/7/04	7,120,063 10/10/06
METHOD FOR ACHIEVING INCREASED CONTROL OVER INTERCONNECT LINE THICKNESS ACROSS A WAFER AND BETWEEN WAFERS	Spansion LLC	11/003208 12/2/04	7,122,465 10/17/06
METHOD TO IMPROVE YIELD AND SIMPLIFY OPERATION OF POLYMER MEMORY CELLS	Spansion LLC	10/919,872 8/17/2004	7,122,853 10/17/2006
SILICIDED BURIED BITLINE PROCESS FOR A NONVOLATILE MEMORY CELL	Spansion LLC	09/885426 6/19/01	7,125,763 10/24/06
DECODER FOR MEMORY DEVICE	Spansion LLC	11/076252 3/8/05	7,126,862 10/24/06
METHOD AND STRUCTURE OF MEMORY ELEMENT PLUG WITH CONDUCTIVE TA REMOVED FROM SIDEWALL AT REGION OF MEMORY ELEMENT FILM	Spansion LLC	10/939773 9/13/04	7,129,133 10/31/06
MULTILEVEL ONO FLASH PROGRAM ALGORITHM FOR THRESHOLD WIDTH CONTROL	Spansion LLC	11/034642 1/13/05	7,130,210 10/31/06

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURING METHOD THEREOF	Spansion Inc.	11/247,328 10/12/2005	7,132,332 11/7/2006
METHOD OF MAKING A SEMICONDUCTOR STRUCTURE	Spansion LLC & Advanced Micro Devices, Inc.	10/939775 9/13/04	7,135,396 11/14/06
METHOD OF MAKING A MEMORY CELL	Spansion LLC	10/979516 11/2/04	7,141,482 11/28/06
BURIED WORD LINE MEMORY INTEGRATED CIRCUIT SYSTEM	Spansion LLC	11/045694 1/27/05	7,141,838 11/28/06
SELECTIVE POLYMER GROWTH FOR MEMORY CELL FABRICATION	Spansion, LLC	11/000740 12/1/04	7,141,844 11/28/06
SYSTEM AND METHOD FOR YDECODING IN A FLASH MEMORY DEVICE	Spansion LLC	10/243315 9/12/02	7,142,454 11/28/06
POSITIVE GATE STRESS DURING ERASE TO IMPROVE RETENTION IN MULTILEVEL, NONVOLATILE FLASH MEMORY	Spansion LLC	10/839562 5/4/04	7,142,455 11/28/06
ELECTRICALLY ADDRESSABLE MEMORY SWITCH	Spansion LLC & Globalfoundries Inc.	10/873069 6/21/04	7,145,793 12/5/06
TEMPERATURE COMPENSATION OF THIN FILM DIODE VOLTAGE THRESHOLD IN MEMORY SENSING CIRCUIT	Spansion LLC	11/086884 3/22/05	7,145,824 12/5/06
METHOD OF FORMING COPPER SULFIDE LAYER OVER SUBSTRATE	Spansion LLC	10/939897 9/13/04	7,148,144 12/12/06
METHOD AND DEVICE FOR REDUCING INTERFACE AREA OF A MEMORY DEVICE	Spansion LLC & FASL LLC	10/859369 6/1/04	7,151,027 12/19/06
MEMORY CELL WITH PLASMAGROWN OXIDE SPACER FOR REDUCED DIBL AND VSS RESISTANCE AND INCREASED RELIABILITY	Spansion LLC	10/981174 11/4/04	7,151,028 12/19/06
DIELECTRIC MEMORY CELL STRUCTURE WITH COUNTER DOPED CHANNEL REGION	Spansion LLC	10/342549 1/15/03	7,151,292 12/19/06
SONOS MEMORY WITH INVERSION BITLINES	Spansion, LLC	10/928582 8/27/04	7,151,293 12/19/06

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
MEMORY DEVICE INCLUDING BARRIER LAYER FOR IMPROVED SWITCHING SPEED AND DATA RETENTION	Spansion LLC	11/052689 2/7/05	7,154,769 12/26/06
SEMICONDUCTOR MEMORY STORAGE DEVICE AND ITS CONTROL METHOD	Spansion LLC	11/064054 2/22/05	7,154,807 12/26/06
USING THIN UNDOPED TEOS WITH BPTEOS ILD OR BPTEOS ILD ALONE TO IMPROVE CHARGE LOSS AND CONTACT RESISTANCE IN MULTI BIT MEMORY DEVICES	Spansion LLC & FASL LLC	10/917562 8/13/04	7,157,335 1/2/07
SWITCHABLE MEMORY DIODE A NEW MEMORY DEVICE	Spansion LLC	10/883350 7/1/04	7,157,732 1/2/07
MOLECULAR MEMORY DEVICE	Spansion LLC & Advanced Micro Devices, Inc.	10/899873 7/27/04	7,157,750 1/2/07
SEMICONDUCTOR DEVICE AND METHOD FOR WRITING DATA INTO THE SEMICONDUCTOR DEVICE	Spansion LLC	11/090716 3/25/05	7,158,417 1/2/07
FLEXIBLE LATENCY IN FLASH MEMORY	Spansion LLC	11/135231 5/23/05	7,158,442 1/2/07
NONVOLATILE SEMICONDUCTOR MEMORY THAT PREVENTS UNAUTHORIZED READING	Spansion LLC & Fujitsu Limited	10/298512 11/19/02	7,159,124 1/2/07
METHODS AND APPARATUS FOR WORDLINE PROTECTION IN FLASH MEMORY DEVICES	Spansion LLC	10/839614 5/5/04	7,160,773 1/9/07
MULTICHIP MODULE AND METHOD OF MANUFACTURE	Spansion LLC	11/116571 4/27/05	7,163,839 1/16/07
METHOD OF FORMATION OF GATE STACK SPACER AND CHARGE STORAGE MATERIALS HAVING REDUCED HYDROGEN CONTENT IN CHARGE TRAPPING DIELECTRIC FLASH MEMORY DEVICE	Spansion LLC & FASL LLC	10/430471 5/6/03	7,163,860 1/16/07
SEMICONDUCTOR MEMORY DEVICES AND METHODS FOR FABRICATING THE SAME	Spansion LLC	11/243752 10/4/05	7,163,862 1/16/07

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
SYSTEM AND METHOD FOR ERASING A MEMORY CELL	Spansion L.L.C.	11/062641 2/23/05	7,167,398 1/23/07
MEMORY CELL WITH REDUCED DIBL AND VSS RESISTANCE	Spansion LLC	10/915771 8/11/04	7,170,130 1/30/07
METHODS AND SYSTEMS FOR REDUCING THE THRESHOLD VOLTAGE DISTRIBUTION FOLLOWING A MEMORY CELL ERASE	Spansion LLC	11/193391 8/1/05	7,170,796 1/30/07
LDC IMPLANT FOR MIRRORBIT TO IMPROVE VT ROLLOFF AND FORM SHARPER JUNCTION	Spansion LLC	10/862636 6/7/04	7,176,113 2/13/07
NONVOLATILE SEMICONDUCTOR MEMORY DEVICE WITH A PLURALITY OF SECTORS	Spansion LLC & Fujitsu Limited	11/085496 3/22/05	7,180,785 2/20/07
REVERSIBLE FIELDPROGRAMMABLE ELECTRIC INTERCONNECTS	Spansion LLC & Coatue Corporation	11/026105 12/30/04	7,183,141 2/27/07
SEMICONDUCTOR DEVICE, SEMICONDUCTOR DEVICE TESTING METHOD, AND PROGRAMMING METHOD	Spansion LLC	11/215253 8/30/05	7,184,338 2/27/07
METHOD FOR STORING IN NONVOLATILE MEMORY AND STORAGE UNIT	Spansion LLC & Fujitsu Limited	10/727481 12/5/03	7,185,140 2/27/07
METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE	Spansion LLC & Fujitsu Microelectronics Limited	10/705881 11/13/03	7,189,659 3/13/07
SEMICONDUCTOR STORAGE DEVICE AND METHOD OF SELECTING BIT LINE OF THE SEMICONDUCTOR STORAGE DEVICE	Spansion LLC & Fujitsu Limited	11/155510 6/20/05	7,190,630 3/13/07
ALUMINUM OXIDE AS LINER OR COVER LAYER TO SPACERS IN MEMORY DEVICE	Spansion LLC & Globalfoundries Inc.	11/087793 3/23/05	7,196,008 3/27/07
FLASH MEMORY DEVICE	Spansion LLC	10/614177 7/8/03	7,196,372 3/27/07

PATENT
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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
CHARGE SHARING TECHNIQUE DURING FLASH MEMORY PROGRAMMING	Spansion LLC	11/229530 9/20/05	7,196,938 3/27/07
BMCHOSTED REALTIME CLOCK AND NONVOLATILE RAM REPLACEMENT	Spansion LLC	10/406130 4/3/03	7,197,657 3/27/07
POLYMER MEMORY DEVICE WITH VARIABLE PERIOD OF RETENTION TIME	Spansion, LLC	10/919572 8/17/04	7,199,394 4/3/07
SYSTEMS AND METHODS FOR A MEMORY AND/OR SELECTION ELEMENT FORMED WITHIN A RECESS IN A METAL LINE	Spansion, LLC	10/985172 11/10/04	7,199,416 4/3/07
METHOD OF FORMING A MEMORY DEVICE HAVING IMPROVED ERASE SPEED	Spansion LLC & Globalfoundries Inc.	11/165330 6/24/05	7,202,128 4/10/07
SEMICONDUCTOR MEMORY DEVICE	Spansion LLC & Advanced Micro Devices, Inc. & Fujitsu Limited	11/066567 2/28/05	7,202,540 4/10/07
METHODS AND SYSTEMS FOR HIGH WRITE PERFORMANCE IN MULTIBIT FLASH MEMORY DEVICES	Spansion LLC	11/037477 1/18/05	7,206,224 4/17/07
SEMICONDUCTOR DEVICE AND SOURCE VOLTAGE CONTROL METHOD	Spansion LLC	11/165008 6/23/05	7,206,232 4/17/07
SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD	Spansion LLC	11/126558 5/11/05	7,206,241 4/17/07
NONVOLATILE MEMORY SYSTEM HAVING A PROGRAMMABLY SELECTABLE BOOT CODE SECTION SIZE	Spansion LLC	10/968414 10/19/04	7,206,914 4/17/07
SEMICONDUCTOR DEVICE WITH HIGH CONDUCTIVITY REGION USING SHALLOW TRENCH	Spansion LLC	10/151595 5/16/02	7,208,382 4/24/07
MEMORY ELEMENT WITH NITROGENCONTAINING ACTIVE LAYER	Spansion LLC	11/021959 12/23/04	7,208,757 4/24/07
METHOD AND STRUCTURE FOR CONTROLLING FLOATING BODY EFFECTS	Spansion LLC	10/756585 1/12/04	7,211,473 5/1/07

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
NONVOLATILE MEMORY AND WRITE METHOD OF THE SAME	Spansion LLC & Fujitsu Limited	11/062662 2/23/05	7,212,443 5/1/07
FLASH MEMORY CELL AND METHODS FOR PROGRAMMING AND ERASING	Spansion LLC	11/511763 8/29/06	7,215,577 5/8/07
A METHOD OF FORMING HIGHLY CONDUCTIVE SEMICONDUCTOR STRUCTURES VIA PLASMA ETCH	Spansion LLC	09/805273 3/13/01	7,217,652 5/15/07
METHOD FOR MANUFACTURING A SEMICONDUCTOR COMPONENT THAT INHIBITS FORMATION OF WORMHOLES	Spansion LLC & Globalfoundries Inc.	11/109964 4/19/05	7,217,660 5/15/07
METHOD AND APPARATUS FOR COUPLING TO A SOURCE LINE IN A MEMORY DEVICE	Spansion LLC	10/658937 9/9/03	7,217,964 5/15/07
PROTECTION OF ACTIVE LAYERS OF MEMORY CELLS DURING PROCESSING OF OTHER ELEMENTS	Spansion LLC	10/987262 11/12/04	7,220,642 5/22/07
SYSTEM AND METHOD FOR GATE FORMATION IN A SEMICONDUCTOR DEVICE	Spansion LLC	11/147207 6/8/05	7,220,643 5/22/07
SELF ALIGNED MEMORY ELEMENT AND WORDLINE	Spansion LLC	10/314591 12/9/02	7,220,985 5/22/07
SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD	Spansion LLC	11/126738 5/11/05	7,221,587 5/22/07
SEMICONDUCTOR DEVICE AND METHOD FOR WRITING DATA INTO SEMICONDUCTOR DEVICE	Spansion LLC	11/193872	7,221,594 5/22/07
SEMICONDUCTOR DEVICE AND METHOD OF GENERATING SENSE SIGNAL	Spansion LLC	11/194007 7/29/05	7,221,595 5/22/07
POLYMER MEMORY CELL OPERATION	Spansion LLC	10/978621 11/1/04	7,221,599 5/22/07
SEMICONDUCTOR MEMORY DEVICE AND CONTROL METHOD HAVING DATA PROTECTION FEATURE	Spansion LLC	11/126869 5/11/05	7,224,602 5/29/07
METHOD AND SYSTEM FOR IMPROVING THE TOPOGRAPHY OF A MEMORY ARRAY	Spansion LLC & FASL LLC	10/861575 6/4/04	7,226,839 6/5/07

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
POWER INTERCONNECT STRUCTURE FOR BALANCED BITLINE CAPACITANCE IN A MEMORY ARRAY	Spansion LLC	11/173930 7/1/05	7,227,768 6/5/07
SEMICONDUCTOR DEVICE AND WRITING METHOD	Spansion LLC	11/194023 7/29/05	7,227,778 6/5/07
SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREOF	Spansion LLC	11/289997 11/30/05	7,227,780 6/5/07
RADICAL OXIDATION FOR BITLINE OXIDE OF SONOS	Spansion LLC & Globalfoundries Inc.	11/113507 4/25/05	7,232,724 6/19/07
A METHOD FOR MANUFACTURING A DOUBLE BITLINE IMPLANT	Spansion LLC	10/431321 5/6/03	7,232,729 6/19/07
METHODS INVOLVING SPINON POLYMERS THAT REVERSIBLY BIND CHARGE CARRIERS	Spansion LLC	11/034154 1/12/05	7,232,750 6/19/07
UTILIZATION OF A TACONTAINING CAP OVER COPPER TO FACILITATE CONCURRENT FORMATION OF COPPER VIAS AND MEMORY ELEMENT STRUCTURES	Spansion LLC & Advanced Micro Devices, Inc.	10/988239 11/12/04	7,232,765 6/19/07
SEMICONDUCTOR DEVICE WITH ELECTRICALLY BIASED DIE EDGE SEAL	Spansion LLC & Advanced Micro Devices, Inc.	10/976876 11/1/04	7,235,867 6/26/07
METHOD AND APPARATUS FOR SCHEDULING WORK IN A FABRICATION FACILITY	Spansion LLC	11/185388 7/20/05	7,236,843 6/26/07
FORMATION METHOD OF AN ARRAY SOURCE LINE IN NAND FLASH MEMORY	Spansion LLC	11/113508 4/25/05	7,238,569 6/26/07
NONVOLATILE MEMORY DEVICE WITH INCREASED RELIABILITY	Spansion LLC & Globalfoundries Inc.	11/063560 2/24/05	7,238,571 7/3/07
METHOD AND APPARATUS FOR APPLYING BIAS TO A STORAGE DEVICE	Spansion LLC	11/317082 12/21/05	7,239,548 7/3/07
METHOD AND APPARATUS FOR REFERENCE CELL ADJUSTING IN A STORAGE DEVICE	Spansion LLC	11/344677 1/31/06	7,239,553 7/3/07

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
SYNCHRONOUS STORAGE DEVICE AND CONTROL METHOD THEREFOR	Spansion LLC	11/317084 12/21/05	7,239,574 7/3/07
MEMORY DEVICE AND METHOD OF CONTROLLING THE SAME	Spansion LLC	11/342013 1/27/06	7,239,576 7/3/07
BOND PAD STRUCTURE FOR COPPER METALLIZATION HAVING INCREASED RELIABILITY AND METHOD FOR FABRICATING SAME	Spansion LLC	10/887585 7/8/04	7,242,102 7/10/07
METHOD FOR MANUFACTURING A SEMICONDUCTOR COMPONENT	Spansion LLC	11/264194 10/31/05	7,244,660 7/17/07
ERASE ALGORITHM FOR MULTILEVEL BIT FLASH MEMORY	Spansion LLC & FASL LLC	10/864947 6/10/04	7,251,158 7/31/07
SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING SAID SEMICONDUCTOR DEVICE	Spansion LLC	11/290001 11/30/05	7,251,161 7/31/07
SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURING METHOD THEREOF	Spansion LLC	11/065305 2/25/05	7,253,046 8/7/07
ACTIVE PROGRAMMING AND OPERATION OF A MEMORY DEVICE	Spansion LLC	10/776870 2/11/04	7,254,053 8/7/07
TESTING FOR OPERATING LIFE OF A MEMORY DEVICE WITH ADDRESS CYCLING USING A GRAY CODE SEQUENCE	Spansion LLC	10/791417 3/2/04	7,254,692 8/7/07
INTERFACE LAYER BETWEEN DUAL POLYCRYSTALLINE SILICON LAYERS	Spansion LLC & Advanced Micro Devices, Inc.	11/135492 5/24/05	7,256,141 8/14/07
MEMORY DEVICE AND METHODS OF USING AND MAKING THE DEVICE	Spansion LLC	10/818261 4/2/04	7,259,039 8/21/07
PAGE BUFFER ARCHITECTURE FOR PROGRAMMING, ERASING AND READING NANOSCALE RESISTIVE MEMORY DEVICES	Spansion LLC	11/139227 5/17/05	7,259,983 8/21/07
VOLTAGE SUPPLY CIRCUIT FOR MEMORY ARRAY PROGRAMMING	Spansion LLC	11/250913 10/14/05	7,260,014 8/21/07

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
MEMORY ARRAY	Spansion LLC	11/262651 10/31/05	7,260,019 8/21/07
SYSTEM AND METHOD FOR REDUCING PROCESSINDUCED CHARGING	Spansion LLC	11/146126 6/7/05	7,262,095 8/28/07
USE OF SUPERCRITICAL FLUID TO DRY WAFER AND CLEAN LENS IN IMMERSION LITHOGRAPHY	Spansion LLC & Globalfoundries Inc.	11/173257 7/1/05	7,262,422 8/28/07
SEMICONDUCTOR MEMORY DEVICE USING READ DATA BUS FOR WRITING DATA DURING HIGHSPEED WRITING	Spansion LLC	11/228777 9/16/05	7,263,007 8/28/07
AVOIDING FIELD OXIDE GOUGING IN SHALLOW TRENCH ISOLATION (STI) REGIONS	Spansion LLC & FASL LLC	10/799413 3/12/04	7,265,014 9/4/07
NONVOLATILE MEMORY DEVICE AND ERASING METHOD THEREFOR	Spansion LLC	11/215889 8/30/05	7,266,019 9/4/07
MEMORY DEVICE FOR CONTROLLING NONVOLATILE AND VOLATILE MEMORIES	Spansion LLC & Fujitsu Limited	10/077778 2/20/02	7,266,664 9/4/07
METHOD OF PROGRAMMING A MEMORY DEVICE	Spansion LLC	11/146690 6/7/05	7,269,050 9/11/07
PROGRAMMING A MEMORY DEVICE	Spansion LLC	11/174560 7/6/05	7,269,067 9/11/07
METHOD, SYSTEM, AND CIRCUIT FOR PERFORMING A MEMORY RELATED OPERATION	Spansion LLC	11/001940 12/1/04	7,272,060 9/18/07
VARIABLE DENSITY AND VARIABLE PERSISTENT ORGANIC MEMORY DEVICES, METHODS, AND FABRICATION	Spansion LLC	11/034071 1/12/05	7,273,766 9/25/07
RELIABLE AND SCALABLE VIRTUAL GROUND MEMORY ARRAY FORMED WITH REDUCED THERMAL CYCLE	Spansion LLC	11/242773 10/4/05	7,273,775 9/25/07
NONVOLATILE MEMORY AND METHOD OF CONTROLLING THE SAME	Spansion LLC	11/342947 1/30/06	7,274,592 9/25/07
STORAGE DEVICE AND CONTROL METHOD THEREFOR	Spansion LLC	11/443770 5/30/06	7,274,602 9/25/07

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
FLASH MEMORY DEVICE	Spansion LLC	10/838215 5/504	7,279,735 10/9/07
NONVOLATILE SEMICONDUCTOR MEMORY DEVICE THAT ERASES STORED DATA AFTER A PREDETERMINED TIME PERIOD WITHOUT THE USE OF A TIMER CIRCUIT	Spansion Inc.	11/087,735 3/24/2005	7,280,404 10/9/2007
NONVOLATILE MEMORY DEVICE, AND CONTROL METHOD THEREFOR	Spansion LLC	11/215850 8/30/05	7,280,414 10/9/07
MEMORY SYSTEM AND TEST METHOD THEREFOR	Spansion LLC	11/173735 7/1/05	7,281,180 10/9/07
METHOD FOR MINIMIZING FALSE DETECTION OF STATES IN FLASH MEMORY DEVICES	Spansion LLC & FASL LLC	10/838962 5/4/04	7,283,398 10/16/07
METHODS AND SYSTEMS FOR HIGH WRITE PERFORMANCE IN MULTIBIT FLASH MEMORY DEVICES	Spansion LLC	11/653655 1/16/07	7,283,402 10/16/07
AUTOMATED TESTS FOR BUILTIN SELF TEST	Spansion LLC	11/041608 1/24/05	7,284,167 10/16/07
POLYMER SPACERS FOR CREATING SUBLITHOGRAPHIC SPACES	Spansion LLC & Globalfoundries Inc.	11/127175 5/12/05	7,285,499 10/23/07
BACKTOBACK NPN/PNP PROTECTION DIODES	Spansion LLC	11/194449 8/2/05	7,285,827 10/23/07
CARRIER FOR STACKED TYPE SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME	Spansion LLC	11/126739 5/11/05	7,285,848 10/23/07
EXPOSURE SYSTEM, SEMICONDUCTOR DEVICE, AND METHOD FOR FABRICATING THE SEMICONDUCTOR DEVICE	Spansion LLC	11/215246 8/30/05	7,286,219 10/23/07
AUTOMATIC RESOURCE ASSIGNMENT IN STACKED MODULE DEVICES	Spansion LLC & Advanced Micro Devices, Inc.	11/158509 6/22/05	7,286,384 10/23/07
RESISTIVE MEMORY DEVICE WITH IMPROVED DATA RETENTION	Spansion LLC	11/165005 6/23/05	7,286,388 10/23/07

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SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING SAID SEMICONDUCTOR DEVICE	Spansion LLC	11/290002 11/30/05	7,286,398 10/23/07
SEMICONDUCTOR DEVICE AND METHOD FOR CONTROLLING THE SAME	Spansion LLC	11/261743 10/28/05	7,286,407 10/23/07
METAL/OXIDE ETCH AFTER POLISH TO PREVENT BRIDGING BETWEEN ADJACENT FEATURES OF A SEMICONDUCTOR STRUCTURE	Spansion LLC & Advanced Micro Devices, Inc.	11/000870 12/1/04	7,288,487 10/30/07
USE OF TACAPPED METAL LINE TO IMPROVE FORMATION OF MEMORY ELEMENT FILMS	Spansion LLC & Globalfoundries Inc.	11/251291 10/14/05	7,288,782 10/30/07
FLASH MEMORY WITH BURIED BIT LINES	Spansion LLC	10/738322 12/16/03	7,288,809 10/30/07
METHOD OF PROGRAMMING A RESISTIVE MEMORY DEVICE	Spansion LLC	11/166572 6/24/05	7,289,351 10/30/07
SYSTEMS AND METHODS FOR ADJUSTING PROGRAMMING THRESHOLDS OF POLYMER MEMORY CELLS	Spansion, LLC	10/919846 8/17/04	7,289,353 10/30/07
METHOD FOR CONTROLLING POLY 1 THICKNESS AND UNIFORMITY IN A MEMORY ARRAY FABRICATION PROCESS	Spansion LLC & Advanced Micro Devices, Inc.	11/035188 1/13/05	7,294,573 11/13/07
MEMORY DEVICE WITH A SELFASSEMBLED POLYMER FILM AND METHOD OF MAKING THE SAME	Spansion LLC	10/958,044 10/4/2004	7,295,461 11/13/2007
FLASH MEMORY PROGRAMMING USING AN INDICATION BIT TO INTERPRET STATE	Spansion LLC	11/229664 9/20/05	7,295,475 11/13/07
SEMICONDUCTOR MEMORY WITH DATA RETENTION LINER	Spansion LLC	11/195201 8/1/05	7,297,592 11/20/07
INTERLAYER DIELECTRIC FOR CHARGE LOSS IMPROVEMENT	Spansion LLC & Advanced Micro Devices	11/147208 6/8/05	7,300,886 11/27/07

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
STRUCTURE AND METHOD FOR LOW VSS RESISTANCE AND REDUCED DIBL IN A FLOATING GATE MEMORY CELL	Spansion LLC	10/762445 1/22/04	7,301,193 11/27/07
SELFALIGNED STI SONOS	Spansion LLC	11/113509 4/25/05	7,303,964 12/4/07
MEMORY CELL AND METHOD OF MAKING THE MEMORY CELL	Spansion LLC & Advanced Micro Devices, Inc.	11/063138 2/22/05	7,306,988 12/11/07
NONCRITICAL COMPLEMENTARY MASKING METHOD FOR POLY1 DEFINITION IN FLASH MEMORY DEVICE FABRICATION	Spansion LLC	11/099339 4/4/05	7,307,002 12/11/07
VOID FREE INTERLAYER DIELECTRIC	Spansion LLC & Advanced Micro Devices, Inc.	11/201378 8/11/05	7,307,027 12/11/07
MEMORY DEVICES WITH ACTIVE AND PASSIVE DOPED SOLGEL LAYERS	Spansion LLC	11/228842 9/16/05	7,307,280 12/11/07
MEMORY DEVICE WITH IMPROVED DATA RETENTION	Spansion LLC	11/089707 3/25/05	7,307,321 12/11/07
THREE DIMENSIONAL POLYMER MEMORY CELL SYSTEMS	Spansion LLC & FASL, LLC	10/899344 7/26/04	7,307,338 12/11/07
FLASH MEMORY DEVICE HAVING IMPROVED PROGRAM RATE	Spansion LLC	11/212850 8/29/05	7,307,878 12/11/07
NONVOLATILE MEMORY DEVICE, AND ITS MANUFACTURING METHOD	Spansion LLC	11/291048 11/29/05	7,307,879 12/11/07
SEMICONDUCTOR DEVICE AND METHOD FOR CONTROLLING THE SAME	Spansion LLC	11/228976 9/16/05	7,307,893 12/11/07
SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME	Spansion LLC	11/127712 5/12/05	7,307,894 12/11/07
MEMORY DEVICE HAVING A NANOCRYSTAL CHARGE STORAGE REGION AND METHOD	Spansion LLC & Advanced Micro Devices, Inc.	11/065388 2/24/05	7,309,650 12/18/07
SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME	Spansion LLC	11/152547 6/14/05	7,309,893 12/18/07

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
SPLIT GATE MULTIBIT MEMORY CELL	Spansion LLC	11/101783 4/7/05	7,312,495 12/25/07
SENSE AMPLIFIERS WITH HIGH VOLTAGE SWING	Spansion LLC	11/024257 12/28/04	7,312,641 12/25/07
RAMP GATE ERASE FOR DUAL BIT FLASH MEMORY	Spansion LLC	11/497597 8/2/06	7,319,615 1/15/08
METHOD FOR ISOLATING A FAILURE SITE IN A WORDLINE IN A MEMORY ARRAY	Spansion LLC	10/981026 11/4/04	7,319,623 1/15/08
SYSTEM AND METHOD FOR GATE FORMATION IN A SEMICONDUCTOR DEVICE	Spansion LLC	11/062629 2/23/05	7,320,914 1/22/08
SEMICONDUCTOR DEVICE AND METHOD FOR CONTROLLING OPERATION THEREOF	Spansion LLC	11/316800 12/22/05	7,321,511 1/22/08
SEMICONDUCTOR DEVICE AND METHOD OF GENERATING A REFERENCE VOLTAGE THEREFOR	Spansion LLC	11/392398 3/28/06	7,321,513 1/22/08
MEMORY DEVICE AND CONTROL METHOD THEREFOR	Spansion LLC	11/378444 3/16/06	7,321,515 1/22/08
ETCHBACK PROCESS FOR CAPPING A POLYMER MEMORY DEVICE	Spansion LLC	11/102004 4/8/05	7,323,418 1/29/08
METHOD AND APPARATUS FOR COUPLING TO A COMMON LINE IN AN ARRAY	Spansion LLC	10/658882 9/9/03	7,323,726 1/29/08
SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR	Spansion LLC	11/361724 2/24/06	7,323,744 1/29/08
MEMORY WITH A COREBASED VIRTUAL GROUND AND DYNAMIC REFERENCE SENSING SCHEME	Spansion LLC	10/600065 6/20/03	7,324,374 1/29/08
FAST WIDE OUTPUT RANGE CMOS VOLTAGE REFERENCE	Spansion LLC	11/135925 5/24/05	7,327,186 2/5/08
METHOD FOR MANUFACTURING A MEMORY DEVICE HAVING A NANOCRYSTAL CHARGE STORAGE REGION	Spansion LLC & Globalfoundries Inc.	11/116538 4/27/05	7,335,594 2/26/08

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
METHOD FOR DETERMINING WORDLINE CRITICAL DIMENSION IN A MEMORY ARRAY AND RELATED STRUCTURE	Spansion LLC	11/416551 5/3/06	7,339,222 3/4/08
DUALLEVEL STACKED FLASH MEMORY CELL WITH A MOSFET STORAGE TRANSISTOR	Spansion LLC	11/154070 6/16/05	7,339,226 3/4/08
DISPOSABLE HARD MASK FOR FORMING BIT LINES	Spansion LLC & Advanced Micro Devices, Inc.	11/100563 4/7/05	7,341,956 3/11/08
PROGRAM AND PROGRAM VERIFY OPERATIONS FOR FLASH MEMORY	Spansion LLC	11/332263 1/17/06	7,342,830 3/11/08
METHOD FOR PATTERNING ELECTRICALLY CONDUCTING POLY(PHENYL ACETYLENE) AND POLY(DIPHENYL ACETYLENE)	Spansion LLC	11/069181 3/1/05	7,344,912 3/18/08
SPIN ON MEMORY CELL ACTIVE LAYER DOPED WITH METAL IONS	Spansion LLC	11/099847 4/6/05	7,344,913 3/18/08
METHOD AND APPARATUS FOR HIGH VOLTAGE OPERATION FOR A HIGH PERFORMANCE SEMICONDUCTOR MEMORY DEVICE	Spansion LLC	11/423638 6/12/06	7,345,916 3/18/08
NONVOLATILE SEMICONDUCTOR DEVICE AND METHOD FOR AUTOMATICALLY RECOVERING ERASE FAILURE IN THE DEVICE	Spansion LLC	11/110220 4/20/05	7,352,620 4/1/08
VOLTAGE REGULATOR WITH LESS OVERSHOOT AND FASTER SETTLING TIME	Spansion LLC	11/212614 8/29/05	7,352,626 4/1/08
METHOD AND APPARATUS FOR TESTING A MEMORY DEVICE	Spansion LLC	11/362318 2/23/06	7,352,638 4/1/08
METHOD FOR FORMING MEMORY ARRAY BITLINES COMPRISING EPITAXIALLY GROWN SILICON AND RELATED STRUCTURE	Spansion LLC & Globalfoundries Inc.	11/112607 4/22/05	7,354,826 4/8/08

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
METHOD OF PROGRAMMING, ERASING AND READING MEMORY CELLS IN A RESISTIVE MEMORY ARRAY	Spansion LLC	11/633791 12/5/06	7,355,886 4/8/08
METHOD AND APPARATUS FOR DRAIN PUMP OPERATION	Spansion LLC	11/423645 6/12/06	7,355,904 4/8/08
METHOD FOR DECREASING SHEET RESISTIVITY VARIATIONS OF AN INTERCONNECT METAL LAYER	Spansion LLC & Advanced Micro Devices, Inc.	11/388390 3/24/06	7,358,191 4/15/08
VOLTAGE DETECTION CIRCUIT, SEMICONDUCTOR DEVICE, METHOD FOR CONTROLLING VOLTAGE DETECTION CIRCUIT	Spansion LLC	11/482129 7/7/06	7,358,778 4/15/08
PREAMORPHIZATION TO MINIMIZE VOID FORMATION	Spansion LLC	11/173244 7/1/05	7,361,586 4/22/08
SEMICONDUCTOR CONTACT AND NITRIDE SPACER FORMATION SYSTEM AND METHOD	Spansion LLC	10/934923 9/2/04	7,361,587 4/22/08
SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE SAME	Spansion LLC	11/394491 3/31/06	7,362,620 4/22/08
MEMORY CELL HAVING ENHANCED HIGHK DIELECTRIC	Spansion L.L.C. & Advanced Micro Devices, Inc.	11/008233 12/10/04	7,365,389 4/29/08
DUAL BIT FLASH MEMORY DEVICES AND METHODS FOR FABRICATING THE SAME	Spansion LLC	11/538404 10/3/06	7,368,347 5/6/08
CONTROLLING A NONVOLATILE STORAGE DEVICE	Spansion LLC	11/639128 12/13/06	7,372,743 5/13/08
METHOD OF MAKING AN ORGANIC MEMORY CELL	Spansion LLC	10/978845 11/1/04	7,374,654 5/20/08
SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD THEREFOR	Spansion LLC	11/443640 5/30/06	7,376,033 5/20/08
METHOD FOR MANUFACTURING A MEMORY DEVICE HAVING A NANOCRYSTAL CHARGE STORAGE REGION	Spansion LLC & Globalfoundries Inc.	11/116551 4/27/05	7,378,310 5/27/08

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
MEMORY ELEMENT USING ACTIVE LAYER OF BLENDED MATERIALS	Spansion LLC	11/052688 2/7/05	7,378,682 5/27/08
AUTOMATED LOADING/UNLOADING OF DEVICES FOR BURNIN TESTING	Spansion LLC	11/424934 6/19/06	7,378,836 5/27/08
METHOD OF PROGRAMMING, READING AND ERASING MEMORYDIODE IN A MEMORYDIODE ARRAY	Spansion LLC	11/021958 12/23/04	7,379,317 5/27/08
OXYGEN ELIMINATION FOR DEVICE PROCESSING	Spansion LLC	11/371023 3/9/06	7,381,620 6/3/08
METHOD AND APPARATUS FOR SECTOR ERASE OPERATION IN A FLASH MEMORY ARRAY	Spansion LLC	11/538408 10/3/06	7,382,650 6/3/08
METHOD OF FABRICATING METALINSULATORMETAL (MIM) DEVICE WITH STABLE DATA RETENTION	Spansion LLC	11/633942 12/5/06	7,384,800 6/10/08
SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE SAME	Spansion LLC	11/494872 7/27/06	7,385,844 6/10/08
REPETITIVE ERASE VERIFY TECHNIQUE FOR FLASH MEMORY DEVICES	Spansion LLC	11/615710 12/22/06	7,385,851 6/10/08
SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME	Spansion LLC	11/977034 10/23/07	7,387,936 6/17/08
MEMORY DEVICE WITH A SELECTION ELEMENT AND A CONTROL LINE IN A SUBSTANTIALLY SIMILAR LAYER	Spansion, LLC	11/001519 12/1/04	7,391,064 6/24/08
RECESSED CHANNEL WITH SEPARATED ONO MEMORY DEVICE	Spansion LLC	11/361,277 2/24/2006	7,394,125 7/1/2008
METHODS FOR ERASING AND PROGRAMMING MEMORY DEVICES	Spansion LLC	11/399130 4/5/06	7,394,702 7/1/08

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
CURRENT SENSING ARCHITECTURE FOR HIGH BITLINE VOLTAGE, RAIL TO RAIL OUTPUT SWING AND VCC NOISE CANCELLATION	Spansion LLC	11/023914 12/28/04	7,397,696 7/8/08
HIGHVOLTAGE TRANSISTOR HAVING A USHAPED GATE AND METHOD FOR FORMING SAME	Spansion LLC	11/003528 12/3/04	7,400,013 7/15/08
SYSTEM AND METHOD FOR PROTECTING SEMICONDUCTOR DEVICES	Spansion L.L.C.	10/976816 11/1/04	7,402,868 7/22/08
MULTI MEDIA CARD WITH HIGH STORAGE CAPACITY	Spansion LLC	11/400902 4/10/06	7,404,026 7/22/08
SEMICONDUCTOR COMPONENT HAVING A CONTACT STRUCTURE AND METHOD OF MANUFACTURE	Spansion LLC & FASL LLC & Advanced Micro Devices, Inc.	10/928665 8/27/04	7,407,882 8/5/08
SEMICONDUCTOR MEMORY DEVICE AND MANUFACTURING METHOD THEREOF	Spansion LLC	11/878296 7/23/07	7,410,857 8/12/08
MEMORY CELL HAVING COMBINATION RAISED SOURCE AND DRAIN AND METHOD OF FABRICATING SAME	Spansion L.L.C. & Advanced Micro Devices, Inc.	11/112884 4/22/05	7,414,277 8/19/08
FLASH MEMORY WITH HIGHK DIELECTRIC MATERIAL BETWEEN SUBSTRATE AND GATE	Spansion LLC	10/658936 9/9/03	7,414,281 8/19/08
CARRIER FOR STACKED TYPE SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING STACKED TYPE SEMICONDUCTOR DEVICES	Spansion LLC	11/341984 1/27/06	7,414,305 8/19/08
METHOD AND APPARATUS FOR MANUFACTURING SEMICONDUCTOR DEVICE	Spansion LLC	11/244166 10/6/05	7,415,318 8/19/08
METHOD AND APPARATUS FOR INITIALIZATION CONTROL IN A NONVOLATILE MEMORY DEVICE	Spansion LLC	11/194111 7/28/05	7,415,568 8/19/08
PAGE.SUB.EXE ERASE ALGORITHM FOR FLASH MEMORY	Spansion LLC & FASL LLC	10/946812 9/22/04	7,415,646 8/19/08

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
METHODS FOR FABRICATING FLASH MEMORY DEVICES	Spansion LLC	11/418352 5/3/06	7,416,940 8/26/08
APPARATUS AND METHOD FOR A MEMORY ARRAY WITH SHALLOW TRENCH ISOLATION REGIONS BETWEEN BIT LINES FOR INCREASED PROCESS MARGINS	Spansion LLC & FASL LLC	10/896292 7/20/04	7,423,312 9/9/08
RANDOM CACHE READ USING A DOUBLE MEMORY	Spansion LLC	11/332241 1/17/06	7,423,915 9/9/08
MEMORY DEVICE AND METHODS FOR ITS FABRICATION	Spansion LLC	11/409361 4/20/06	7,432,156 10/7/08
BIT LINE IMPLANT	Spansion LLC & Globalfoundries Inc.	11/254769 10/21/05	7,432,178 10/7/08
METHOD AND APPARATUS FOR ADDRESS ALLOTTING AND VERIFICATION IN A SEMICONDUCTOR DEVICE	Spansion LLC	11/341029 1/27/06	7,433,219 10/7/08
MULTIBIT FLASH MEMORY DEVICE HAVING IMPROVED PROGRAM RATE	Spansion LLC	11/229519 9/20/05	7,433,228 10/7/08
NONVOLATILE MEMORY DEVICE, AND CONTROL METHOD OF NONVOLATILE MEMORY DEVICE	Spansion LLC	11/479387 6/30/06	7,436,715 10/14/08
SHALLOW TRENCH ISOLATION APPROACH FOR IMPROVED STI CORNER ROUNDING	Spansion LLC	10/277395 10/22/02	7,439,141 10/21/08
METHOD OF DETERMINING VOLTAGE COMPENSATION FOR FLASH MEMORY DEVICES	Spansion LLC	11/340916 1/27/06	7,440,333 10/21/08
CONTROL OF MEMORY DEVICES POSSESSING VARIABLE RESISTANCE CHARACTERISTICS	Spansion LLC	10/983919 11/8/04	7,443,710 10/28/08
MEMORY ERASE MANAGEMENT SYSTEM	Spansion LLC	11/470958 9/7/06	7,443,712 10/28/08
HIGH PERFORMANCE FLASH MEMORY DEVICE CAPABLE OF HIGH DENSITY DATA STORAGE	Spansion LLC	11/229527 9/20/05	7,443,732 10/28/08

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
MEMORY ARRAY TESTER INFORMATION PROCESSING SYSTEM	Spansion LLC	11/253521 10/18/05	7,443,746 10/28/08
SONOS MEMORY CELL HAVING HIGHK DIELECTRIC	Spansion LLC & Globalfoundries Inc.	11/196434 8/4/05	7,446,369 11/4/08
MEMORY DEVICE WITH ACTIVE LAYER OF DENDRIMERIC MATERIAL	Spansion LLC	11/642477 12/20/06	7,449,742 11/11/08
UTILIZATION OF MEMORYDIODE WHICH MAY HAVE EACH OF A PLURALITY OF DIFFERENT MEMORY STATES	Spansion LLC	11/021944 12/23/04	7,450,416 11/11/08
SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREFOR	Spansion LLC	11/636111 12/7/06	7,450,419 11/11/08
SEMICONDUCTOR DEVICE AND ITS CONTROL METHOD	Spansion LLC	11/127713 5/12/05	7,450,434 11/11/08
VOLTAGE CONTROL CIRCUIT AND SEMICONDUCTOR DEVICE	Spansion LLC	11/166575 6/24/05	7,450,460 11/11/08
SEMICONDUCTOR MEMORY DEVICE AND METHOD OF FABRICATING THE SAME	Spansion LLC	11/368678 3/7/06	7,453,116 11/18/08
FLASH MEMORY DEVICE HAVING IMPROVED PROGRAM RATE	Spansion LLC	11/931992 10/31/07	7,453,724 11/18/08
DRAIN VOLTAGE REGULATOR	Spansion LLC	11/639936 12/15/06	7,460,415 12/2/08
NONVOLATILE MEMORY DEVICE FOR STORING MULTIBIT DATA	Spansion LLC	11/386686 3/23/06	7,462,529 12/9/08
METHODS FOR FABRICATING SEMICONDUCTOR DEVICES AND CONTACTS TO SEMICONDUCTOR DEVICES	Spansion LLC	11/227657 9/14/05	7,462,903 12/9/08
METHOD OF INCREASING ERASE SPEED IN MEMORY ARRAYS	Spansion LLC	11/268025 11/7/05	7,462,907 12/9/08
NEGATIVE WORDLINE BIAS FOR REDUCTION OF LEAKAGE CURRENT DURING FLASH MEMORY OPERATION	Spansion LLC	11/615280 12/22/06	7,463,525 12/9/08
ISOLATION REGION BIRD'S BEAK SUPPRESSION	Spansion LLC & Globalfoundries Inc.	11/258209 10/26/05	7,465,644 12/16/08

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
STACKED ORGANIC MEMORY DEVICES AND METHODS OF OPERATING AND FABRICATING	Spansion LLC	11/251999 10/17/05	7,465,956 12/16/08
SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREFOR	Spansion LLC	11/360091 2/22/06	7,466,605 12/16/08
THIN FILM GERMANIUM DIODE WITH LOW REVERSE BREAKDOWN	Spansion LLC & Globalfoundries Inc.	11/290787 11/30/05	7,468,296 12/23/08
TEST STRUCTURES FOR DEVELOPMENT OF METALINSULATORMETAL (MIM) DEVICES	Spansion LLC	11/633930 12/5/06	7,468,525 12/23/08
SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE SAME	Spansion LLC	11/637260 12/11/06	7,468,909 12/23/08
METHODS FOR FABRICATING SEMICONDUCTOR DEVICES AND CONTACTS TO SEMICONDUCTOR DEVICES	Spansion LLC	11/355474 2/15/06	7,470,614 12/30/08
USE OF PERIODIC REFRESH IN MEDIUM RETENTION MEMORY ARRAYS	Spansion LLC	11/613832 12/20/06	7,474,579 1/6/09
AGGRESSIVE CLEANING PROCESS FOR SEMICONDUCTOR DEVICE CONTACT FORMATION	Spansion LLC & Advanced Micro Devices, Inc.	11/128391 5/13/05	7,476,604 1/13/09
SEMICONDUCTOR DEVICE AND METHOD OF FABRICATION	Spansion LLC	11/237591 9/27/05	7,479,427 1/20/09
FORMING METALSEMICONDUCTOR FILMS HAVING DIFFERENT THICKNESSES WITHIN DIFFERENT REGIONS OF AN ELECTRONIC DEVICE	Spansion LLC	11/949637 12/3/07	7,482,217 1/27/09
SEMICONDUCTOR MEMORY DEVICE	Spansion LLC & Advanced Micro Devices, Inc.	11/656438 1/23/07	7,482,226 1/27/09
FLASH MEMORY AND METHOD FOR CONTROLLING THE MEMORY	Spansion LLC & Fujitsu Limited	11/083016 3/18/05	7,487,286 2/3/09

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
METHOD AND SYSTEM FOR FORMING STRAIGHT WORD LINES IN A FLASH MEMORY ARRAY	Spansion LLC	11/155707 5/16/05	7,488,657 2/10/09
CARRIER STRUCTURE FOR STACKEDTYPE SEMICONDUCTOR DEVICE, METHOD OF PRODUCING THE SAME, AND METHOD OF FABRICATING STACKEDTYPE SEMICONDUCTOR DEVICE	Spansion LLC	11/214630 8/30/05	7,489,029 2/10/09
REDUCTION OF LEAKAGE CURRENT AND PROGRAM DISTURBS IN FLASH MEMORY DEVICES	Spansion LLC	11/398414 4/5/06	7,489,560 2/10/09
METHOD AND APPARATUS FOR SETTING INPUT TERMINALS FOR RECEIVING CONTROL INFORMATION IN A SEMICONDUCTOR MEMORY DEVICE	Spansion LLC	11/192562 7/29/05	7,490,192 2/10/09
HIGH K STACK FOR NONVOLATILE MEMORY	Spansion LLC	11/086310 3/23/05	7,492,001 2/17/09
RESISTIVE MEMORY CELL ARRAY WITH COMMON PLATE	Spansion LLC	11/412589 4/27/06	7,495,951 2/24/09
ENHANCED ETCHING OF A HIGH DIELECTRIC CONSTANT LAYER	Spansion LLC & Advanced Micro Devices, Inc.	11/371024 3/9/06	7,498,222 3/3/09
SENSE AMPLIFIERS WITH HIGH VOLTAGE SWING	Spansion LLC	11/985427 11/15/07	7,498,849 3/3/09
USING ORGANIC SEMICONDUCTOR MEMORY IN CONJUNCTION WITH A MEMS ACTUATOR FOR AN ULTRA HIGH DENSITY MEMORY	Spansion LLC	10/817186 4/2/04	7,499,309 3/3/09
SONOS MEMORY WITH INVERSION BITLINES	Spansion LLC	11/595639 11/10/06	7,501,677 3/10/09
SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD	Spansion LLC	11/789888 4/25/07	7,502,271 3/10/09
TRANSFER OF NONASSOCIATED INFORMATION ON FLASH MEMORY DEVICES	Spansion LLC	11/741996 4/30/07	7,505,298 3/17/09

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
METHOD AND ARCHITECTURE FOR FAST FLASH MEMORY PROGRAMMING	Spansion LLC	11/504254 8/14/06	7,505,328 3/17/09
METHOD OF FORMING NARROWLY SPACED FLASH MEMORY CONTACT OPENINGS AND LITHOGRAPHY MASKS	Spansion LLC	10/916167 8/11/04	7,507,661 3/24/09
USING SHARED MEMORY WITH AN EXECUTEINPLACE PROCESSOR AND A COPROCESSOR	Spansion LLC	11/557439 11/7/06	7,512,743 3/31/09
METHOD AND APPARATUS FOR HIGH VOLTAGE OPERATION FOR A HIGH PERFORMANCE SEMICONDUCTOR MEMORY DEVICE	Spansion LLC	11/950,811 12/5/2007	7,613,044 11/3/2009
SEMICONDUCTOR DEVICE AND METHOD FOR BOOSTING WORD LINE	Spansion LLC	11/502957 8/11/06	7,525,853 4/28/09
COMPENSATION METHOD TO ACHIEVE UNIFORM PROGRAMMING SPEED OF FLASH MEMORY DEVICES	Spansion LLC	11/767622 6/25/07	7,532,518 5/12/09
SEMICONDUCTOR DEVICES WITH COPPER INTERCONNECTS AND COMPOSITE SILICON NITRIDE CAPPING LAYERS	Spansion LLC & Advanced Micro Devices, Inc.	11/356311 2/17/06	7,534,732 5/19/09
READING MULTICELL MEMORY DEVICES UTILIZING COMPLEMENTARY BIT INFORMATION	Spansion LLC	11/834420 8/6/07	7,535,767 5/19/09
TWOBIT MEMORY CELL HAVING CONDUCTIVE CHARGE STORAGE SEGMENTS AND METHOD FOR FABRICATING SAME	Spansion LLC	11/416703 5/3/06	7,538,383 5/26/09
SWITCHABLE MEMORY DIODE A NEW MEMORY DEVICE	Spansion LLC	11/616045 12/26/06	7,550,761 6/23/09
USING IMPLANTED POLY1 TO IMPROVE CHARGING PROTECTION IN DUALPOLY PROCESS	Spansion LLC	11/724726 3/16/07	7,553,727 6/30/09

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
DIE OFFSET DIE TO DIE BONDING	Spansion LLC	11/820278 6/18/07	7,554,204 6/30/09
SCAN SENSING METHOD THAT IMPROVES SENSING MARGINS	Spansion LLC	11/957366 12/14/07	7,558,101 7/7/09
REGULATION OF BOOSTSTRAP NODE RAMP RATE USING CAPACITANCE TO COUNTER PARASITIC ELEMENTS IN CHANNEL	Spansion LLC	11/837976 8/13/07	7,558,116 7/7/09
EFFICIENT AND SYSTEMATIC MEASUREMENT FLOW ON DRAIN VOLTAGE FOR DIFFERENT TRIMMING IN FLASH SILICON CHARACTERIZATION	Spansion LLC	11/837949 8/13/07	7,558,123 7/7/09
CONTROLLER, DATA MEMORY SYSTEM, DATA REWRITING METHOD, AND COMPUTER PROGRAM PRODUCT	Spansion LLC	11/187650 7/22/05	7,558,904 7/7/,09
VIRTUAL MEMORY CARD CONTROLLER	Spansion LLC	11/549551 10/13/06	7,558,907 7/7/09
SELECT TRANSISTOR USING BURIED BIT LINE FROM CORE	Spansion LLC	11/465701 8/18/06	7,561,457 7/14/09
METHODS AND SYSTEMS FOR RECOVERING DATA IN A NONVOLATILE MEMORY ARRAY	Spansion LLC & Globalfoundries Inc.	11/724774 3/16/07	7,561,465 7/14/09
CYCLING IMPROVEMENT USING HIGHER ERASE BIAS	Spansion LLC	11/724711 3/16/07	7,561,471 7/14/09
REFERENCEFREE SAMPLED SENSING	Spansion LLC	11/955802 12/13/07	7,561,484 7/14/09
MEMORY DEVICE AND METHODS FOR ITS FABRICATION	Spansion LLC	12/199692 8/27/08	7,564,091 7/21/09
METHOD OF PROGRAMMING MEMORY DEVICE	Spansion LLC	11/633845 12/5/06	7,564,708 7/21/09
NONVOLATILE STORAGE AND ERASE CONTROL	Spansion LLC	11/879989 7/18/07	7,564,720 7/21/09
SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE	Spansion LLC	11/644031 12/22/06	7,565,477 7/21/09

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
PROCESS FOR MAKING A RESISTIVE MEMORY CELL WITH SEPARATELY PATTERNED ELECTRODES	Spansion LLC	11/763510 6/15/07	7,566,628 7/28/09
SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD	Spansion LLC	11/654703 1/17/07	7,566,978 7/28/09
AUTOMATED LOADING/UNLOADING OF DEVICES FOR BURNIN TESTING	Spansion LLC	12/055141 3/25/08	7,567,076 7/28/09
NONVOLATILE MEMORY ARRAY ARCHITECTURE	Spansion LLC	11/929724 10/30/07	7,567,457 7/28/09
SEMICONDUCTOR FORMATION METHOD THAT UTILIZES MULTIPLE ETCH STOP LAYERS	Spansion LLC	10/934828 9/2/04	7,572,727 8/11/09
SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME	Spansion LLC	11/362317 2/23/06	7,573,091 8/11/09
BACKTOBACK NPN/PNP PROTECTION DIODES	Spansion LLC	11/855704 9/14/07	7,573,103 8/11/09
SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME	Spansion LLC	11/514391 8/30/06	7,573,743 8/11/09
SEMICONDUCTOR DEVICE AND METHOD OF CONTROLLING THE SAME	Spansion LLC	11/644161 12/22/06	7,574,576 8/11/09
VARIABLE BREAKDOWN CHARACTERISTIC DIODE	Spansion LLC	11/087000 3/22/05	7,579,631 8/25/09
SEMICONDUCTOR MEMORY DEVICE COMPRISING ONE OR MORE INJECTING BILAYER ELECTRODES	Spansion LLC	11/227603 9/15/05	7,582,893 9/1/09
SEMICONDUCTOR DEVICE AND FABRICATION METHOD THEREFOR	Spansion LLC	11/513693 8/30/06	7,589,371 9/15/09
SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREFOR	Spansion LLC	11/478554 6/28/06	7,596,032 9/29/09
FLASH MEMORY DEVICE HAVING INCREASED OVERERASE CORRECTION EFFICIENCY AND ROBUSTNESS AGAINST DEVICE VARIATIONS	Spansion L.L.C.	10/976760 11/1/04	7,599,228 10/6/09

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
HETEROSTRUCTURE VARIABLE SILICON RICH NITRIDE FOR MULTIPLE LEVEL MEMORY FLASH MEMORY DEVICE	Spansion LLC	11/957787 12/17/07	7,602,067 10/13/09
READING ELECTRONIC MEMORY UTILIZING RELATIONSHIPS BETWEEN CELL STATE DISTRIBUTIONS	Spansion LLC	11/957309 12/14/07	7,602,639 10/13/09
SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME	Spansion LLC	11/636155 12/7/06	7,605,457 10/20/09
VOLTAGE DETECTOR CIRCUIT	Spansion LLC	11/975097 10/16/07	7,605,616 10/20/09
MEMORY WITH A COREBASED VIRTUAL GROUND AND DYNAMIC REFERENCE SENSING SCHEME	Spansion LLC	12/017693 1/22/08	7,606,068 10/20/09
SEMICONDUCTOR DEVICE AND CONTROL METHOD OF THE SAME	Spansion LLC	11/501449 8/8/06	7,606,085 10/20/09
POLYMER DIELECTRICS FOR MEMORY ELEMENT ARRAY INTERCONNECT	Spansion LLC	10/817467 4/2/04	7,608,855 10/27/09
DECODING SYSTEM CAPABLE OF REDUCING SECTOR SELECT AREA OVERHEAD FOR FLASH MEMORY	Spansion LLC	11/935049 11/5/07	7,613,042 11/3/09
METHOD AND APPARATUS FOR HIGH VOLTAGE OPERATION FOR A HIGH PERFORMANCE SEMICONDUCTOR MEMORY DEVICE	Spansion LLC	11/950811 12/5/07	7,613,044 11/3/09
ALGORITHM FOR CHARGE LOSS REDUCTION AND VT DISTRIBUTION IMPROVEMENT	Spansion LLC	11/959122 12/18/07	7,619,932 11/17/09
METHOD AND APPARATUS FOR ADAPTIVE MEMORY CELL OVERERASE COMPENSATION	Spansion LLC	11/613379 12/20/06	7,619,934 11/17/09
APPARATUS AND METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE	Spansion LLC	11/441760 5/26/06	7,622,067 11/24/09

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
MEMORY DEVICE HAVING IMPLANTED OXIDE TO BLOCK ELECTRON DRIFT, AND METHOD OF MANUFACTURING THE SAME	Spansion LLC	11/615563 12/22/06	7,622,373 11/24/09
SELECTIVE CONTACT FORMATION USING MASKING AND RESIST PATTERNING TECHNIQUES	Spansion LLC & Globalfoundries Inc.	11/411353 4/25/06	7,622,389 11/24/09
DETERMINING SCHEDULING PRIORITY USING QUEUE TIME OPTIMIZATION	Spansion LLC & Globalfoundries Inc.	11/356267 2/16/06	7,623,936 11/24/09
SEMICONDUCTOR DEVICE WITH REDUCED TRANSISTOR BREAKDOWN VOLTAGE FOR PREVENTING SUBSTRATE JUNCTION CURRENTS	Spansion LLC	11/414082 4/27/06	7,626,227 12/1/09
COMPUTING DEVICE INCLUDING A STACKED SEMICONDUCTOR DEVICE	Spansion LLC	11/514390 8/30/06	7,626,253 12/1/09
MULTIPHASE WORDLINE ERASING FOR FLASH MEMORY	Spansion, LLC	11/745327 5/7/07	7,626,869 12/1/09
FLASH MEMORY DEVICE WITH EXTERNAL HIGH VOLTAGE SUPPLY	Spansion LLC	11/613383 12/20/06	7,626,882 12/1/09
SEMICONDUCTOR DEVICE AND CONTROL METHOD THEREFOR	Spansion LLC	11/543399 10/4/06	7,630,245 12/8/09
CONTROLLED RAMP RATES FOR METAL BITLINES DURING WRITE OPERATIONS FROM HIGH VOLTAGE DRIVER FOR MEMORY APPLICATIONS	Spansion LLC	11/872989 10/16/07	7,630,250 12/8/09
FLASH MEMORY PROGRAMMING AND VERIFICATION WITH REDUCED LEAKAGE CURRENT	Spansion LLC	11/398415 4/5/06	7,630,253 12/8/09
METHODS FOR CONTROLLING THE PROFILE OF A TRENCH OF A SEMICONDUCTOR STRUCTURE	Spansion LLC	11/538403 10/3/06	7,632,689 12/15/09
SYSTEM AND METHOD FOR PROCESSING AN ORGANIC MEMORY CELL	Spansion LLC & Advanced Micro Devices, Inc.	11/256558 10/21/05	7,632,706 12/15/09

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Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
SEMICONDUCTOR DEVICE HAVING A PAD METAL LAYER AND A LOWER METAL LAYER THAT ARE ELECTRICALLY COUPLED, WHEREAS APERTURES ARE FORMED IN THE LOWER METAL LAYER BELOW A CENTER AREA OF THE PAD METAL LAYER	Spansion LLC & FASL LLC	10/823970 4/13/04	7,632,749 12/15/09
MEMORY DEVICES WITH ACTIVE AND PASSIVE LAYERS HAVING MULTIPLE SELFASSEMBLED SUBLAYERS	Spansion LLC	11/228975 9/16/05	7,633,129 12/15/09
FLEXIBLE WORD LINE BOOSTING ACROSS VCC SUPPLY	Spansion LLC	11/951263 12/5/07	7,633,815 12/15/09
CHARGE PUMP TO SUPPLY VOLTAGE BANDS	Spansion LLC	12/012389 2/1/08	7,633,824 12/15/09
METHODS FOR FABRICATING A MEMORY DEVICE INCLUDING A DUAL BIT MEMORY CELL	Spansion LLC	11/614050 12/20/06	7,635,627 12/22/09
FAST RAILTORAIL VOLTAGE COMPARATOR AND METHOD FOR RAILTORAIL VOLTAGE COMPARISON	Spansion LLC	11/336464 1/20/06	7,635,994 12/22/09
HIGH SPEED CASCODE CIRCUIT WITH LOW POWER CONSUMPTION	Spansion LLC	11/986509 11/20/07	7,639,543 12/29/09
METHOD FOR IMPROVING PERFORMANCE IN A MOBILE DEVICE	Spansion LLC	11/414845 5/1/06	7,639,768 12/29/09
CARRIER FOR STACKED TYPE SEMICONDUCTOR DEVICE AND METHOD OF FABRICATING THE SAME	Spansion LLC	11/894828 8/22/07	7,642,637 1/5/10
ADDRESS/DATA MULTIPLEXED DEVICE	Spansion LLC	11/986385 11/20/07	7,643,371 1/5/10
SYSTEM AND METHOD FOR MAINTAINING RAM COMMAND TIMING ACROSS PHASESHIFTED TIME DOMAINS	Spansion LLC	11/642412 12/19/06	7,644,226 1/5/10
SELF ALIGNED MEMORY ELEMENT AND WORDLINE	Spansion LLC	11/750724 5/18/07	7,645,632 1/12/10

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SEMICONDUCTOR DEVICE AND PROGRAMMING METHOD THEREFOR	Spansion LLC	11/414647 4/27/06	7,645,693 1/12/10
ARRAYED NEUTRON DETECTOR WITH MULTI SHIELDING ALLOWING FOR DISCRIMINATION BETWEEN RADIATION TYPES	Spansion LLC	11/966672 12/28/07	7,645,993 1/12/10
METHOD OF SELECTING OPERATING CHARACTERISTICS OF A RESISTIVE MEMORY DEVICE	Spansion LLC	11/590378 10/31/06	7,646,624 1/12/10
SEMICONDUCTOR DEVICE, FABRICATING METHOD THEREOF, AND PHOTOMASK	Spansion LLC	11/291318 11/30/05	7,651,826 1/26/10
MULTILEVEL OPERATION IN DUAL ELEMENT CELLS USING A SUPPLEMENTAL PROGRAMMING LEVEL	Spansion LLC	11/771961 6/29/07	7,652,919 1/26/10
FAST SINGLE PHASE PROGRAM ALGORITHM FOR QUADBIT	Spansion LLC	11/874,076 10/17/2007	7,656,705 2/2/2010
SPARK GENERATOR METHOD AND IGNITION SYSTEM USING THE SAME	Spansion LLC & VMX Technologies Inc.	11/212580 08/29/2005	7,121,270 10/17/2006
METHOD AND APPARATUS FOR MANUFACTURING SEMICONDUCTOR DEVICE	Spansion LLC	10/682299 10/10/2003	6,979,577 12/27/2005
FLASH EEPROM ARRAY WITH PAGED ERASE ARCHITECTURE	Spansion LLC	07/426601 10/23/1989	5,126,808 06/30/1992
ASYNCHRONOUS/SYNCHRONOUS PIPELINE DUAL MODE MEMORY ACCESS CIRCUIT AND METHOD	Spansion LLC	07/407403 09/13/1989	5,107,465 04/21/1992
FLASH EEPROM ARRAY WITH NEGATIVE GATE VOLTAGE ERASE OPERATION	Spansion LLC	07/426332 10/23/1989	5,077,691 12/31/1991
METHOD OF FORMING AND REMOVING POLYSILICON LIGHTLY DOPED DRAIN SPACERS	Spansion LLC	07/355634 05/23/1989	5,013,675 05/07/1991

Patent	Owner	Application No. Filing Date	Publication No. / Patent No. Issue Date
SEMICONDUCTOR MEMORY DEVICE AND METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE	Spansion, LLC	10/643967	7,098,147 8/29/2006
METHOD AND DEVICE FOR PROGRAMMING CELLS IN A MEMORY ARRAY IN A NARROW DISTRIBUTION	Spansion LLC	10/738301 12/16/2003	6,961,267 11/1/2005
MEMORY DEVICE WITH A SELF-ASSEMBLED POLYMER FILM AND METHOD OF MAKING THE SAME	Spansion LLC	10/139745 5/7/2002	6,855,977 2/15/2005
METHOD FOR BALL GRID ARRAY (BGA) SOLDER ATTACH FOR SURFACE MOUNT	Spansion LLC	12/12660005/23/ 2008	20090289101
SINGULATED BARE DIE TESTING	Spansion LLC	11/835545 08/08/2007	20080233663
FLASH MEMORY DEVICES AND METHODS FOR FABRICATING THE SAME	Spansion LLC & Advanced Micro Devices, Inc.	11/615425 12/22/2006	20080153236
INTEGRATED CIRCUIT SYSTEM WITH MEMORY SYSTEM	Spansion LLC & Advanced Micro Devices, Inc.	11735229 04/13/2007	20080153224
MEMORY SYSTEM WITH POLY METAL GATE	Spansion LLC & Globalfoundries Inc.	11/735241 04/13/2007	20080149990
INTEGRATED CIRCUIT SYSTEM WITH IMPLANT OXIDE	Spansion LLC & Globalfoundries Inc.	11/611860 12/16/2006	20080142874
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