PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	Grant of Security Interest in Patent Rights - Second Priority

CONVEYING PARTY DATA

Name	Execution Date
UTAC Hong Kong Limited	06/04/2010

RECEIVING PARTY DATA

Name:	JPMorgan Chase Bank, N.A., as Collateral Agent
Street Address:	P.O. Box 2558
City:	Houston
State/Country:	TEXAS
Postal Code:	77252

PROPERTY NUMBERS Total: 78

Property Type	Number
Patent Number:	6821817
Patent Number:	6841859
Patent Number:	6982491
Patent Number:	7344920
Patent Number:	7348663
Patent Number:	6800948
Patent Number:	6818472
Patent Number:	6933176
Patent Number:	6987032
Patent Number:	7315080
Patent Number:	7372151
Patent Number:	7091581
Patent Number:	7411289
Patent Number:	5596231
Patent Number:	6285075

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Patent Number:	6326678
Patent Number:	6552417
Patent Number:	6724071
Patent Number:	6667191
Patent Number:	7224048
Patent Number:	6111324
Patent Number:	6284569
Patent Number:	6734552
Patent Number:	6979594
Patent Number:	7015072
Patent Number:	6242281
Patent Number:	6294100
Patent Number:	6545347
Patent Number:	6585905
Patent Number:	6734044
Patent Number:	6940154
Patent Number:	7071545
Patent Number:	7247526
Patent Number:	7270867
Patent Number:	7381588
Patent Number:	7410830
Patent Number:	7449771
Patent Number:	6737755
Patent Number:	7358119
Patent Number:	6781242
Patent Number:	6790710
Patent Number:	7439099
Patent Number:	6903304
Patent Number:	6818978
Patent Number:	6818980
Patent Number:	6635957
Patent Number:	6872661
Patent Number:	6933594
Patent Number:	6946324
Patent Number:	6964918

Patent Number:	6989294
Patent Number:	6995460
Patent Number:	7009286
Patent Number:	7033517
Patent Number:	7081403
Patent Number:	7226811
Patent Number:	7232755
Patent Number:	7271032
Patent Number:	7371610
Patent Number:	7482690
Patent Number:	5397921
Patent Number:	5409865
Patent Number:	5843808
Patent Number:	6984785
Patent Number:	7342305
Patent Number:	6429048
Patent Number:	6229200
Patent Number:	6498099
Patent Number:	7049177
Application Number:	10985233
Application Number:	11377425
Application Number:	11008593
Application Number:	11916242
Application Number:	11061895
Application Number:	12418262
Application Number:	11797457
Application Number:	10957576
Application Number:	12400391

CORRESPONDENCE DATA

Fax Number: (212)455-2502

Correspondence will be sent via US Mail when the fax attempt is unsuccessful.

Phone: (212) 455-7976

Email: ksolomon@stblaw.com

Correspondent Name: Mindy M. Lok, Esq.

Address Line 1: Simpson Thacher & Bartlett LLP

Address Line 2: 425 Lexington Avenue

Address Line 4:	New York, NEW YORK 10017
ATTORNEY DOCKET NUMBER:	509335/1129
NAME OF SUBMITTER:	Mindy M. Lok

Total Attachments: 7
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GRANT OF SECURITY INTEREST IN PATENT RIGHTS

This GRANT OF SECURITY INTEREST IN PATENT RIGHTS ("Agreement"), effective as of June 4, 2010 is made by UTAC Hong Kong Limited, a company incorporated under the laws of Hong Kong, located at 14/F Texaco Centre, 138 Texaco Road, Tsuen Wan, N.T., Hong Kong (the "Chargor"), in favor of JPMorgan Chase Bank, N.A., a national banking association, with an address at P.O Box 2558, Houston, Texas 77252, as Collateral Agent (the "Agent") for itself and the Secured Parties, parties to the Credit Agreements dated as of October 30, 2007 (as amended, supplemented or otherwise modified from time to time, the "Credit Agreements"), among Global A&T Electronics Ltd., a corporation organized and existing under the laws of the Cayman Islands and parent of Chargor (the "Borrower"), Global A&T Finco Ltd., each lender from time to time party thereto, ABN AMRO Bank N.V. as Taiwan Collateral Agent and JPMorgan Chase Bank, N.A. as Administrative Agent and the Agent.

W I T N E S S E T H:

WHEREAS, pursuant to the Credit Agreements, the Secured Parties have severally agreed to make loans and other extensions of credit to the Borrower upon the terms and subject to the conditions set forth therein; and

WHEREAS, in connection with the Credit Agreements, the Chargor has executed and delivered a Second Priority Security Deed, dated as of May 4, 2010, in favor of the Agent (together with all amendments and modifications, if any, from time to time thereafter made thereto, the "Second Priority Security Deed");

WHEREAS, pursuant to the Second Priority Security Deed, the Chargor pledged and granted to the Agent for the benefit of the Agent and the Secured Parties a second priority fixed charge ranking pari passu with the Indenture Security in all intellectual property, including the patents, patent applications and interests in licenses listed on Schedule A hereto; and

WHEREAS, the Chargor has duly authorized the execution, delivery and performance of this Agreement;

NOW THEREFORE, for good and valuable consideration, the receipt of which is hereby acknowledged, and in order to induce the Secured Parties to make loans and other financial accommodations to the Borrower pursuant to the Credit Agreements, the Chargor agrees, for the benefit of the Agent and the Secured Parties, as follows:

SECTION 1. Definitions. Unless otherwise defined herein or the context otherwise requires, terms used in this Agreement, including its preamble and recitals, have the meanings provided or provided by reference in the Credit Agreement and the Second Priority Security Deed.

SECTION 2. Grant of Security Interest. The Chargor hereby creates and grants a Security Interest in all of the Chargor's right, title and interest in, to and under its present and future patents, patent applications and interests in licenses (including, without limitation, those

items listed on Schedule A hereto) (collectively, the "Collateral"), to the Agent for the benefit of the Agent and the Secured Parties to secure payment, discharge and performance of all the Obligations.

SECTION 3. Purpose. This Agreement has been executed and delivered by the Chargor for the purpose of recording the grant of Security Interest herein with the United States Patent and Trademark Office. The security interest granted hereby has been granted to the Secured Parties in connection with the Second Priority Security Deed and is expressly subject to the terms and conditions thereof. The Second Priority Security Deed (and all rights and remedies of the Secured Parties thereunder) shall remain in full force and effect in accordance with its terms.

SECTION 4. Acknowledgment. The Chargor does hereby further acknowledge and affirm that the rights and remedies of the Secured Parties with respect to the Security Interest in the Collateral granted hereby are more fully set forth in the Credit Agreement and the Second Priority Security Deed, the terms and provisions of which (including the remedies provided for therein) are incorporated by reference herein as if fully set forth herein. In the event of any conflict between the terms of this Agreement and the terms of the Second Priority Security Deed, the terms of the Second Priority Security Deed shall govern.

SECTION 5. Counterparts. This Agreement may be executed in counterparts, each of which will be deemed an original, but all of which together constitute one and the same original.

IN WITNESS WHEREOF, the parties hereto have caused this Agreement to be duly executed and delivered by their respective officers thereunto duly authorized as of the day and year first above written.

UTAC HONG KONG LIMITED

By: _____
Name: Tan Chee Keong
Title: Director
Date: June 4, 2010

JPMORGAN CHASE BANK, N.A.
as Collateral Agent for the Secured Parties

By: _____
Name: ELSA GUNG
Title: ASSOCIATE
Date: June 4, 2010

SCHEDULE A

U.S. Patents and Patent Applications

Title	Patent / Application Number
Premolded Cavity IC Package	US 6,821,817
Premolded Cavity IC Package	US 6,841,859
Sensor Semiconductor Package and Method of Manufacturing the Same	US 6,982,491
Integrated Circuit Package and Method for Fabricating Same	US 7,344,920
Integrated Circuit Package and Method for Fabricating Same	US 7,348,663
Ball Grid Array Package	US 6,800,948
Ball Grid Array Package	US 6,818,472
Ball Grid Array Package and Process for Manufacturing Same	US 6,933,176
Ball Grid Array Package and Process for Manufacturing Same	US 6,987,032
Ball Grid Array Package that Includes a Collapsible Spacer for Separating Die Adapter from a Heat Spreader	US 7,315,080
Improved Ball Grid Array Package and Method of Manufacturing Same	US 7,372,151
Integrated Circuit Package and Process for Fabricating the Same	US 7,091,581
Integrated Circuit with Partially Exposed Contact Pads and Process for Fabricating the Same	US 7,411,289
High Power Dissipation Plastic Encapsulated Package for Integrated Circuit Die	US 5,596,231
Integrated Circuit Package with Bonding Planes on a Ceramic Ring using an Adhesive Assembly	US 6,285,075
Molded Plastic Package with Heat Sink and Enhanced Electrical Performance	US 6,326,678
Molded Plastic Package with Heat Sink and Enhanced Electrical Performance	US 6,552,417
Molded Plastic Package with Heat Sink and Enhanced Electrical Performance	US 6,724,071
Chip Scale Integrated Circuit Package	US 6,667,191
Flip Chip Ball Grid Array Package	US 7,224,048
Integrated Chip Carrier Ring/Stiffener & Method for Manufacturing a Flexible Integrated Circuit Package	US 6,111,324
Method of Manufacturing a Flexible Integrated Circuit Package Utilizing an Integrated Carrier Ring/ Stiffener	US 6,284,569
Enhanced Thermal Dissipation Integrated Circuit Package	US 6,734,552
Process for Manufacturing Ball Grid Array Package	US 6,979,594
Method of Manufacturing an Enhanced Thermal Dissipation Integrated Circuit Package	US 7,015,072
Saw-Singulated Leadless Plastic Chip Carrier	US 6,242,281
Exposed Die Leadless Plastic Chip Carrier	US 6,294,100
Enhanced Leadless Chip Carrier	US 6,545,347

Leadless Plastic Chip Carrier with Partial Etch Die Attach Pad	US 6,585,905
Multiple Leadframe Laminated IC package	US 6,734,044
Integrated Circuit Package and Method of Manufacturing the IC Package	US 6,940,154
Shielded Integrated Circuit Package	US 7,071,545
Process for Fabricating an Integrated Circuit Package	US 7,247,526
Leadless Plastic Chip Carrier	US 7,270,867
Shielded Integrated Circuit Package	US 7,381,588
Leadless Plastic Chip Carrier and Method of Fabricating Same	US 7,410,830
Multiple Leadframe Laminated IC Package	US 7,449,771
Ball Grid Array Package with Enhanced Thermal Characteristics	US 6,737,755
Thin Array Plastic Package Without Die Attach Pad and Process for Fabricating the Same	US 7,358,119
Thin Ball Grid Array Package	US 6,781,242
Method of Manufacturing an Integrated Circuit Package	US 6,790,710
Thin Ball Grid Array Package	US 7,439,099
Process for Dressing Molded Array Package Saw Blade	US 6,903,304
Ball Grid Array Package with Shielding	US 6,818,978
Stacked Semiconductor Package and Method of Manufacturing the Same	US 6,818,980
Leadless Plastic Chip Carrier with Etch Back Pad Singulation and Die Attach Pad Array	US 6,635,957
Leadless Plastic Chip Carrier with Etch Back Pad Singulation and Die Attach Pad Array	US 6,872,661
Leadless Plastic Chip Carrier with Etch Back Pad Singulation	US 6,933,594
Process for Fabricating a Leadless Plastic Chip Carrier	US 6,946,324
Electronic Components Such as Thin Array Plastic Packages and Process for Fabricating Same	US 6,964,918
Leadless Plastic Chip Carrier with Etch Back Pad Singulation	US 6,989,294
Leadless Plastic Chip Carrier with Etch Back Pad Singulation	US 6,995,460
Thin Leadless Plastic Chip Carrier	US 7,009,286
Method of Fabricating a Leadless Plastic Chip Carrier	US 7,033,517
Thin Leadless Plastic Chip Carrier	US 7,081,403
Process for Fabricating a Leadless Plastic Chip Carrier	US 7,226,811
Process for Fabricating Pad Frame and Integrated Circuit Package	US 7,232,755
Leadless Plastic Chip Carrier with Etch Back Pad Singulation	US 7,271,032
Process for Fabricating an Integrated Circuit Package with Reduced Mold Warping	US 7,371,610
Electronic Components Such as Thin Array Plastic Packages and Process for Fabricating Same	US 7,482,690
Tab Grid Array	US 5,397,921
Process for Assembling a TAB Grid Array Package for an Integrated Circuit	US 5,409,865
Structure and Method for Automated Assembly of a TAB Grid Array Package	US 5,843,808
Thermally Enhanced Cavity Down Integrated Circuit Package	US 6,984,785

Thermally Enhanced Cavity Down Integrated Circuit Package	US 7,342,305
Metal Foil Laminated IC Package	US 6,429,048
Saw-Singulated Leadless Plastic Chip Carrier	US 6,229,200
Leadless Plastic Chip Carrier with Etch Back Pad Singulation	US 6,498,099
Leadless Plastic Chip Carrier with Standoff Contacts and Die Attach Pad	US 7,049,177
Cavity IC Package and Process for Manufacturing Same	(10/985,233)
Improved Ball Grid Array Package and Process for Manufacturing the Same	(11/377,425)
Integrated Circuit Package and Process for Fabricating the Same	(11/008,593)
Etch Isolation LPCC/QFN Strip	(11/916,242)
Ball Grid Array Package with Improved Thermal Characteristics	(11/061,895)
Package-on-Package Interconnection by Embedded Columns	(12/418,262)
Process for Fabricating a Leadless Plastic Chip Carrier	(11/797,457)
Leadless Plastic Chip Carrier with Contact Standoff	(10/957,576)
Leadless Integrated Circuit Package Having Standoff Contacts And Die Attach Pad	(12/400,391)