

PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT
CONVEYING PARTY DATA	
Name	Execution Date
Nanonexus (Assignment for the Benefit of Creditors), LLC	06/01/2010
RECEIVING PARTY DATA	
Name:	Verigy (Singapore) Pte. Ltd.
Street Address:	No. 1 Yishun Avenue 7
City:	Singapore
State/Country:	SINGAPORE
Postal Code:	768923
PROPERTY NUMBERS Total: 68	
Property Type	Number
Patent Number:	6917525
Patent Number:	7349223
Patent Number:	7382142
Patent Number:	6812718
Patent Number:	7009412
Patent Number:	6799976
Patent Number:	6815961
Patent Number:	7126358
Patent Number:	6791171
Patent Number:	7247035
Patent Number:	7153399
Patent Number:	7126220
Patent Number:	7137830
Patent Number:	6710609
Patent Number:	7579848

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REEL: 024640 FRAME: 0301

CH \$2720.00 6917525

Patent Number:	7138818
Patent Number:	7403029
Patent Number:	7621761
Application Number:	60365625
Application Number:	60797886
Application Number:	60255099
Application Number:	60718137
Application Number:	11552110
Application Number:	12517528
Application Number:	60868535
Application Number:	60941890
Application Number:	60938551
Application Number:	11692138
Application Number:	60787473
Application Number:	60891192
Application Number:	12546432
Application Number:	11858064
Application Number:	12354520
Application Number:	12175393
Application Number:	60136637
Application Number:	11995490
Application Number:	60699647
Application Number:	11563664
Application Number:	60212923
Application Number:	60213729
Application Number:	60146241
Application Number:	11556134
Application Number:	10717813
Application Number:	60651294
Application Number:	60592908
Application Number:	60568216
Application Number:	60573541
Application Number:	60314776
Application Number:	10888761
Application Number:	60810037

Application Number:	12525051
Application Number:	60898964
Application Number:	60136636
PCT Number:	US0308520
PCT Number:	US0768285
PCT Number:	US0014164
PCT Number:	US0021012
PCT Number:	US0786394
PCT Number:	US0319963
PCT Number:	US0765400
PCT Number:	US0604502
PCT Number:	US0517881
PCT Number:	US0014768
PCT Number:	US0627423
PCT Number:	US0226785
PCT Number:	US0321579
PCT Number:	US0852644
PCT Number:	US0119792

CORRESPONDENCE DATA

Fax Number: (303)713-6260

Correspondence will be sent via US Mail when the fax attempt is unsuccessful.

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Address Line 4: Denver, COLORADO 80201

NAME OF SUBMITTER:

Gregory W. Osterloth

Total Attachments: 8

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EXHIBIT B

PATENT ASSIGNMENT AGREEMENT

Whereas, NanoNexus (assignment for the benefit of creditors), LLC, a California limited liability company (the "**Seller**"), with principal offices located at 1100 La Avenida Street, Building A, Mountain View, California 94043 is the sole and exclusive owner of those certain patents and patent applications set forth in Attachment A to this Assignment (referred to as the "**Patent Portfolio**"); and

Whereas Verigy (Singapore) Pte. Ltd., a Singapore corporation having its principal place of business at No. 1 Yishun Avenue 7, Singapore 768923 (hereinafter "**Buyer**") is desirous of acquiring the entire right, title and interest in, to and under the said Patent Portfolio, including the entire right, title and interest in, to and under any international or foreign counterpart patent owned or controlled by Seller, and any continuation, continuation-in-part, divisional, renewal, reexamination, reissue, national phase filing of, or substitute for any of the patents or patent applications in the Patent Portfolio, including the right to file same in the future based on the patents and patent applications of the Patent Portfolio.

Now, Therefore, for good and valuable consideration, the receipt of which is hereby acknowledged, Seller does hereby sell, assign, transfer and set over, and agrees to sell, assign, transfer and set over, the entire right, title and interest to Verigy, in, to and under the patents and patent applications of the Patent Portfolio set forth in Attachment A to this Assignment, and any inventions described in the patents and patent applications of the Patent Portfolio, any reissue or reissues of said patents and patent applications already granted and which may be granted, any certificates of reexamination already granted and which may be granted, the same to be held and enjoyed by Verigy for its own use and enjoyment, and for the use and enjoyment of its successors, assigns or other legal representatives, to the end of the term or terms for which any patents are or may be granted, reissued or extended, as fully and entirely as the same would have been held and enjoyed by Seller if this assignment and sale had not been made; together with all claims for damages or profits due or accrued by reason of past, present or future infringement of one or more of said patents or patent applications, with the right and discretion to sue for said damages or profits, and to collect said damages or profits for Seller's own use and behalf, and for the use and behalf of its successors, assigns or other legal representatives, without the involvement or participation of Seller; together with all rights to encumber part or all of the Patent Portfolio.

Seller hereby authorizes and requests the Commissioner of Patents and Trademarks or an equivalent officer in any jurisdiction in which said patents have issued, or in which said patent applications are pending, or in which patent applications claiming said inventions will be filed, to issue any and all Letters Patent on said inventions to Verigy as assignee of the entire right, title and interest in and to said Patent Portfolio and inventions, and hereby covenants that Seller has full right to convey the entire interest herein assigned, and that, except as otherwise provided between the parties, Seller has not executed, and will not execute, any agreements in conflict therewith.

Seller also agrees to execute any Confirmation Assignment relating to the assigned patents and patent applications in the Patent Portfolio, or to the inventions described therein.

In Witness Whereof, the parties, by their duly authorized representatives, have executed this Assignment.

SELLER:

NanoNexus (assignment for the
benefit of creditors), LLC

By: _____

Its: _____

Manager

BUYER:

Verigy (Singapore) Pte. Ltd.

By: _____

Its: _____

SELLER:

NanoNexus (assignment for the
benefit of creditors), LLC,

By: _____

Its: _____

BUYER:

Verigy (Singapore) Pte. Ltd.

By: Paul Lau

Its: Paul Lau
Director
Verigy (Singapore) Pte Ltd

ATTACHMENT A

SCHEDULE OF TRANSFERRED INTELLECTUAL PROPERTY

NanoNexus (assignment for the benefit of creditors), LLC is not making any representations or warranties as to the status of the patents listed in this schedule of transferred intellectual property regarding whether said patents have been issued, allowed, are currently being prosecuted or have expired.

Issued Patents in US

Title	Country	Filing Date	Patent #	Grant Date
Construction Structures and Manufacturing Processes for Probe Card Assemblies and Packages Having Wafer Level Springs	USA	6/24/2002	6,917,525	7/12/2005
Enhanced Compliant Probe Card Systems Having Improved Planarity	USA	6/16/2004	7,349,223	3/25/2008
High Density Interconnect System Having Rapid Fabrication Cycle	USA	5/18/2005	7,382,142	6/3/2008
Massively Parallel Interface for Electronic Circuits	USA	5/26/2000	6,812,718	11/2/2004
Massively Parallel Interface for Electronic Circuit	USA	8/12/2004	7,009,412	3/7/2006
Construction Structures and Manufacturing Processes for Integrated Circuit Wafer Probe Card Assemblies	USA	7/27/2000	6,799,976	10/5/2004
Construction Structures and Manufacturing Processes for Integrated Circuit Wafer Probe Card Assemblies	USA	3/8/2002	6,815,961	11/9/2004
Construction Structures and Manufacturing Processes for Integrated Circuit Wafer Probe Card Assemblies	USA	9/27/2004	7,126,358	10/24/2006
Systems For Testing And Packaging Integrated Circuits	USA	6/20/2001	6,791,171	9/14/2004
Enhanced Stress Metal Spring Contactor	USA	9/1/2004	7,247,035	7/24/2007
Method and Apparatus for Producing Uniform, Isotropic Stresses in a Sputtered Film	USA	8/23/2002	7,153,399	12/26/2006
A Miniaturized Contact Spring	USA	3/17/2003	7,126,220	10/24/2006
Miniaturized Contact Spring	USA	3/17/2003	7,137,830	11/21/2006
Mosaic Decal Probe	USA	7/15/2002	6,710,609	3/23/2004
High Density Interconnect System for IC Packages and Interconnect Assemblies	USA	2/7/2006	7,579,848	8/25/2009
Massively Parallel Interface for Electronic Circuit	USA	1/5/2006	7,138,818	11/21/2006
Massively Parallel Interface for Electronic Circuit	USA	11/1/2006	7,403,029	7/22/2008
Systems For Testing And Packaging Integrated Circuits	USA	7/20/2007	7,621,761	11/24/2009

Issued Patents Outside of US

Title	Country	Filing Date	Patent #	Grant Date
A Miniaturized Contact Spring	TAIW	3/17/2003	1 288958	10/21/2007
Construction Structures and Manufacturing Processes for Integrated Circuit Wafer Probe Card Assemblies	KORS	5/23/2000	10-0707044	4/5/2007
Method and Apparatus for Producing Uniform Isotropic Stresses in a Sputtered Film	JAPA	8/23/2002	3,794,586	4/21/2006
Systems For Testing And Packaging Integrated Circuits	GERM	6/20/2001	60115437.1-08	11/30/2005

Patent Applications in US

Title	Country	Application #	Filing Date
A Miniaturized Contact Spring	USA	60/365,625	3/18/2002
Apparatus and Methods for Processing, Testing, and Packaging of Semiconductor ICs and Image Sensors	USA	60/797,886	5/5/2006
Apparatus for Optical Switching	USA	60/255,099	12/12/2000
Compliant NanoContactors for Application in Portable and High Density Electronic Systems	USA	60/718,137	9/16/2005
Construction Structures and Manufacturing Processes for Integrated Circuit Wafer Probe Card Assemblies	USA	11/552,110	10/23/2006
Construction Structures and Manufacturing Processes for Integrated Circuit Wafer Probe Card Assemblies	USA	12/517,528	12/4/2007
Construction Structures and Manufacturing Processes for Integrated Circuit Wafer Probe Card Assemblies	USA	60/868,535	12/4/2006
Enhanced Contactors for ATE Tester Interfaces and Microbump Contacts	USA	60/941,890	6/4/2007
Enhanced Fabrication Process for Electrically Conductive Through Vias	USA	60/938,551	5/17/2007
Fine Pitch Microfabricated Spring Contact Structure & Method	USA	11/692,138	3/27/2007
Fine Pitch Microfabricated Spring Contacts	USA	60/787,473	3/29/2006
Fine Pitch Probe Card Having Rapid Fabrication Cycle	USA	60/891,192	2/22/2007
Form Factor - Phicom Litigation	USA		
High Density Interconnect System for IC Packages and Interconnect Assemblies	USA	12/546,432	8/24/2009
High Density Interconnect System Having Rapid Fabrication Cycle	USA	11/858,064	9/19/2007
High Density Interconnect System Having Rapid Fabrication Cycle	USA	12/354,520	1/15/2009
Massively Parallel Interface for Electronic Circuit	USA	12/175,393	7/17/2008
Massively Parallel Interface for Electronic Circuits	USA	60/136,637	5/27/1999
Method and Apparatus for Producing Controlled Stresses and Stress Gradients in Sputtered Films	USA	11/995,490	7/14/2006
Method and Apparatus for Producing Controlled Stresses and Stress Gradients in Sputtered Films	USA	60/699,647	7/14/2005
Method and Apparatus for Producing Uniform Stresses and Stress Gradients in Sputtered Films on Large Area Substrates	USA	NOT FILED	NOT FILED
Method and Apparatus for Producing Uniform, Isotropic Stresses in a Sputtered Film	USA	11/563,664	11/27/2006
Method For Testing And Packaging Intergrated Circuits	USA	60/212,923	6/20/2000
Method For Testing And Packaging Intergrated Circuits	USA	60/213,729	6/22/2000
Method of Massively Parallel Testing of Circuits	USA	60/146,241	7/28/1999
Miniaturized Contact Spring	USA	11/556,134	11/2/2006
Miniaturized Contact Spring	USA		
Mosaic Decal Probe	USA	10/717,813	11/19/2003
Nano-Contactor Embodiments for IC Packages and Interconnect Components	USA	60/651,294	2/8/2005
Probe Card Assembly with Rapid Fabrication Cycle	USA	60/592,908	7/29/2004

Probe Card with Improved Probe Spring and Titanium/Ceramic Laminate Siffener	USA	NOT FILED	NOT FILED
ProbeChip Cleaning Wafer	USA	60/568,216	5/4/2004
Quick-Change Probe Chip	USA	60/573,541	5/20/2004
Soldered Probe Chip Platform	USA	NOT FILED	NOT FILED
Sputtering Technique	USA	60/314,776	8/24/2001
Standardized Layout Patterns and Routing Structures for Integrated Circuit Wafer Probe Card Assemblies	USA	10/888,761	7/9/2004
Stress Metal Spring with Interface Stress Decoupling Layer	USA	60/810,037	5/31/2006
Structures and Processes for Fabrication of Probe Card Assemblies with Multi-Layer Interconnect	USA	12/525,051	1/31/2008
Structures and Processes for Fabrication of Probe Card Assemblies with Multi-Layer Interconnect	USA	60/898,964	1/31/2007
Wafer Interface for High Density Wafer Probe Card	USA	60/136,636	5/27/1999

Patent Applications Outside of US

Title	Country	Application #	Filing Date
Apparatus and Methods for Processing, Testing, and Packaging of Semiconductor ICs and Image Sensors	TAIW	96116185	5/7/2007
Construction Structures and Manufacturing Processes for Probe Card Assemblies and Packages Having Wafer Level Springs	TAIW	92117023	6/23/2003
Fine Pitch Microfabricated Spring Contacts	TAIW	96111117	3/29/2007
Method and Apparatus for Producing Uniform Isotropic Stresses in a Sputtered Film	TAIW	93104363	2/20/2004
Structures and Processes for Fabrication of Probe Card Assemblies with Multi-Layer Interconnect	TAIW	97103779	1/31/2008
A Miniaturized Contact Spring	PCT	PCT/US03/08520	3/18/2003
Apparatus and Methods for Processing, Testing, and Packaging of Semiconductor ICs and Image Sensors	PCT	PCT/US07/68285	5/4/2007
Construction Structures and Manufacturing Processes for Integrated Circuit Wafer Probe Card Assemblies	PCT	PCT/US00/14164	5/23/2000
Construction Structures and Manufacturing Processes for Integrated Circuit Wafer Probe Card Assemblies	PCT	PCT/US00/21012	7/27/2000
Construction Structures and Manufacturing Processes for Integrated Circuit Wafer Probe Card Assemblies	PCT	PCT/US07/86394	12/4/2007
Construction Structures and Manufacturing Processes for Probe Card Assemblies and Packages Having Wafer Level Springs	PCT	PCT/US03/19963	6/23/2003
Fine Pitch Microfabricated Spring Contact Structure and Method	PCT	PCT/US07/65400	3/28/2007
High Density Interconnect System for IC Packages and Interconnect Assemblies	PCT	PCT/US06/04502	2/8/2006
High Density Interconnect System Having Rapid Fabrication Cycle	PCT	PCT/US05/17881	5/20/2005
Massively Parallel Interface for Electronic Circuits	PCT	PCT/US00/14768	5/26/2000
Method and Apparatus for Producing Controlled Stresses and Stress Gradients in Sputtered Films	PCT	PCT/US06/27423	7/14/2006
Method and Apparatus for Producing Uniform Isotropic Stresses in a Sputtered Film	PCT	PCT/US02/26785	8/23/2002
Mosaic Decal Probe	PCT	PCT/US03/21579	7/10/2003

Structures and Processes for Fabrication of Probe Card Assemblies with Multi-Layer Interconnect	PCT	PCT/US08/52644	1/31/2008
Systems For Testing And Packaging Integrated Circuits	PCT	PCT/US01/19792	6/20/2001
A Miniaturized Contact Spring	KORS	10-2004-7014722	3/18/2003
Construction Structures and Manufacturing Processes for Probe Card Assemblies and Packages Having Wafer Level Springs	KORS	10-2004-7021199	6/23/2003
High Density Interconnect System for IC Packages and Interconnect Assemblies	KORS	10-2007-7018104	2/8/2006
High Density Interconnect System Having Rapid Fabrication Cycle	KORS	10-2006-7026713	5/20/2005
Massively Parallel Interface for Electronic Circuits	KORS	10-2001-7015187	5/26/2000
Method and Apparatus for Producing Controlled Stresses and Stress Gradients in Sputtered Films	KORS	10-2008-7003566	7/14/2006
Method and Apparatus for Producing Uniform Isotropic Stresses in a Sputtered Film	KORS	10-2004-7002479	8/23/2002
Systems For Testing And Packaging Integrated Circuits	KORS	10-2002-7002170	6/20/2001
A Miniaturized Contact Spring	JAPA	2003-579319	3/18/2003
Construction Structures and Manufacturing Processes for Integrated Circuit Wafer Probe Card Assemblies	JAPA	2001-500317	5/23/2000
Construction Structures and Manufacturing Processes for Integrated Circuit Wafer Probe Card Assemblies	JAPA	2001-514582	7/27/2000
Construction Structures and Manufacturing Processes for Probe Card Assemblies and Packages Having Wafer Level Springs	JAPA	2004-516216	6/23/2003
High Density Interconnect System for IC Packages and Interconnect Assemblies	JAPA	2007-554348	2/8/2006
High Density Interconnect System Having Rapid Fabrication Cycle	JAPA	2007-527504	5/20/2005
Massively Parallel Interface for Electronic Circuits	JAPA	2001-0500957	5/26/2000
Systems For Testing And Packaging Integrated Circuits	JAPA	2002-504502	6/20/2001
A Miniaturized Contact Spring	GERM	10392441.8-34	3/18/2003
Construction Structures and Manufacturing Processes for Integrated Circuit Wafer Probe Card Assemblies	EPC	952386.1	7/27/2000
Construction Structures and Manufacturing Processes for Probe Card Assemblies and Packages Having Wafer Level Springs	EPC	3754376.6	6/23/2003
Massively Parallel Interface for Electronic Circuits	EPC	936397.9	5/26/2000
Method and Apparatus for Producing Uniform Isotropic Stresses in a Sputtered Film	EPC	2768666.6	8/23/2002
Systems For Testing And Packaging Integrated Circuits	EPC	1946604.4	6/20/2001
A Miniaturized Contact Spring	CHIN	3806293.3	3/18/2003
Construction Structures and Manufacturing Processes for Probe Card Assemblies and Packages Having Wafer Level Springs	CHIN	03814848.X	6/23/2003
High Density Interconnect System Having Rapid Fabrication Cycle	CHIN	200580016256	5/20/2005
Method and Apparatus for Producing Uniform Isotropic Stresses in a Sputtered Film	CHIN	2816612.4	8/23/2002

ALL-PURPOSE ACKNOWLEDGMENT

State of California

County of **Santa Clara**

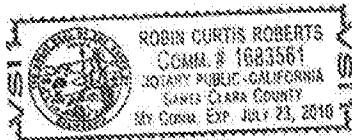
} SS.

On 5-26-10, before me, Robin Curtis Roberts, Notary Public, Notary Public,

personally appeared Maria Pichardo, who proved to me on the

basis of satisfactory evidence to be the person(s) whose name(s) is/are subscribed to the within instrument and acknowledged to me that he/she/they executed the same in his/her/their authorized capacity(ies), and that by his/her/their signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of California that the foregoing paragraph is true and correct.



WITNESS my hand and official seal.

[Signature]

Robin Curtis Roberts
Notary for the State of California
My commission expires July 23rd, 2010
Commission Number # 1683651

OPTIONAL INFORMATION

The information below is optional. However, it may prove valuable and could prevent fraudulent attachment of this form to an unauthorized document.

CAPACITY CLAIMED BY SIGNER (PRINCIPAL)

- ☐ INDIVIDUAL
☐ CORPORATE OFFICER _____ TITLE(S)
☐ PARTNER(S)
☐ ATTORNEY-IN-FACT
☐ TRUSTEE(S)
☐ GUARDIAN/CONSERVATOR
☐ OTHER: _____

DESCRIPTION OF ATTACHED DOCUMENT

TITLE OR TYPE OF DOCUMENT

NUMBER OF PAGES

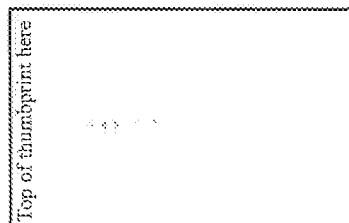
DATE OF DOCUMENT

SIGNER (PRINCIPAL) IS REPRESENTING:

NAME OF PERSON(S) OR ENTITY(IES)

RIGHT
THUMBPRINT
OF
SIGNER

OTHER



PATENT

RECORDED: 07/07/2010

REEL: 024640 FRAME: 0311