PATENT ASSIGNMENT

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Silicon Aquarius, Incorporated	04/23/2007

RECEIVING PARTY DATA

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PROPERTY NUMBERS Total: 4

Property Type	Number
Application Number:	12767517
Application Number:	12751632
Application Number:	12545730
Application Number:	11771689

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Total Attachments: 8

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ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, Silicon Aquarius, Incorporated, a Texas corporation, with an office at 1701 North Greenville Avenue, Suite 1108, Richardson, Texas 75081, ("***Assignor***"), does hereby sell, assign, transfer, and convey unto S. Aqua Semiconductor, LLC, a Delaware limited liability company, with an address at 2711 Centerville Road, Suite 400, Wilmington, DE 19808 ("***Assignee***"), or its designees, all right, title, and interest that exist today and may exist in the future in and to any and all of the following (collectively, the "***Patent Rights***"):

(a) the provisional patent applications, patent applications and patents listed in the table below (the "***Patents***");

(b) all patents and patent applications (i) to which any of the Patents directly or indirectly claims priority, (ii) for which any of the Patents directly or indirectly forms a basis for priority, and/or (iii) that were co-owned applications that directly or indirectly incorporate by reference the Patents;

(c) all reissues, reexaminations, extensions, continuations, continuations in part, continuing prosecution applications, requests for continuing examinations, divisions, registrations of any item in any of the foregoing categories (a) and (b);

(d) all foreign patents, patent applications, and counterparts relating to any item in any of the foregoing categories (a) through (c), including, without limitation, certificates of invention, utility models, industrial design protection, design patent protection, and other governmental grants or issuances;

(e) all items in any of the foregoing in categories (b) through (d), whether or not expressly listed as Patents below and whether or not claims in any of the foregoing have been rejected, withdrawn, cancelled, or the like;

(f) all inventions, invention disclosures, and discoveries described in any item in any of the foregoing categories (a) through (e) and all other rights arising out of such inventions, invention disclosures, and discoveries;

(g) all rights to apply in any or all countries of the world for patents, certificates of invention, utility models, industrial design protections, design patent protections, or other governmental grants or issuances of any type related to any item in any of the foregoing categories (a) through (f), including, without limitation, under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement, or understanding;

(h) all causes of action (whether known or unknown or whether currently pending, filed, or otherwise) and other enforcement rights under, or on account of, any of the

Patents and/or any item in any of the foregoing categories (b) through (g), including, without limitation, all causes of action and other enforcement rights for

(i) damages,
(ii) injunctive relief, and
(iii) any other remedies of any kind

for past, current, and future infringement; and

(i) all rights to collect royalties and other payments under or on account of any of the Patents and/or any item in any of the foregoing categories (b) through (h) arising after the date hereof.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
5,835,932	US	3/13/1997	Methods and systems for maintaining data locality in a multiple memory bank system having DRAM with integral SRAM G. R. Mohan Rao
5890195	US	5/14/1997	DRAM with integral SRAM comprising a plurality of sets of address latches each associated with one of a plurality of SRAM G. R. Mohan Rao
TW115131 (TW19980103567)	TW	3/11/1998	DRAM with integral SRAM and systems and methods using the same G. R. Mohan Rao
JP10-539883T	JP	3/11/1998	DRAM with integral SRAM and systems and methods using the same G. R. Mohan Rao
EP0966741	EP	3/11/1998	DRAM with integral SRAM and systems and methods using the same

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
			G. R. Mohan Rao
EP0966741(GB)	GB	3/11/1998	DRAM with integral SRAM and systems and methods using the same G. R. Mohan Rao
EP0966741(IT)	IT	3/11/1998	DRAM with integral SRAM and systems and methods using the same G. R. Mohan Rao
5,856,940	US	8/15/1997	Low latency DRAM cell and method therefor G. R. Mohan Rao
TW121810 (TW19980112906)	TW	8/15/1998	Low latency DRAM cell and method therefor G. R. Mohan Rao
5,940,329	US	12/17/1997	Memory architecture and systems and methods using the same Stephen Earl Seitsinger
6,418,063	US	5/14/1999	Memory architecture and systems and methods using the same Stephen Earl Seitsinger
5,953,738	US	7/02/1997	DRAM with integral SRAM and arithmetic-logic units G. R. Mohan Rao
5,963,468	US	1/30/1998	Low latency memories and systems using the same G. R. Mohan Rao
6,256,256	US	8/28/1998	Dual port random access memories and systems using the same G. R. Mohan Rao

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
6,256,221	US	2/17/2000	Arrays of two-transistor, one-capacitor dynamic random access memory cells with interdigitated bitlines Wayland Bart Holland
5,963,497	US	5/18/1998	Dynamic random access memory system with simultaneous access and refresh operations and methods for using the same Wayland Bart Holland
6,233,193	US	4/20/1999	Dynamic random access memory system with a static random access memory interface and methods for using the same Wayland Bart Holland
5,991,191	US	12/05/1997	Methods and circuits for single-memory cell multivalue data storage G. R. Mohan Rao
5,995,409	US	3/20/1998	Electrically-programmable read-only memory fabricated using a dynamic random access memory fabrication process and methods for programming same Wayland Bart Holland
6,005,799	US	8/06/1998	Methods and circuits for single-memory dynamic cell multivalue data storage G. R. Mohan Rao
6,173,356	US	2/20/1998	Multi-port DRAM with integral SRAM and systems and methods using the same

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
			G. R. Mohan Rao
6,504,785	US	7/20/2000	Multiprocessor system with integrated memory G. R. Mohan Rao
6,222,216	US	10/21/1997	Non-volatile and memory fabricated using a dynamic memory process and method therefor G. R. Mohan Rao
TW164666 (TW19980114070)	TW	9/21/2002	Non-volatile and memory fabricated using a dynamic memory process and method therefore G. R. Mohan Rao
6,222,786	US	11/02/1999	Dynamic random access memory with write-without-restore and systems and methods using the same Wayland Bart Holland
6,282,606	US	4/02/1999	Dynamic random access memories with hidden refresh and utilizing one-transistor, one-capacitor cells, systems and methods Wayland Bart Holland
TW147109 (TW20000104889)	TW	12/01/2001	Dynamic random access memories with hidden refresh and utilizing one-transistor, one-capacitor cells, systems and methods Wayland Bart Holland
6,310,880	US	3/17/2000	Content addressable memory cells and systems and devices using the same

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
			Craig Waller
6,597,594	US	4/10/2001	Content addressable memory cells and systems and devices using the same Craig Waller
6,396,764	US	11/16/2000	Segmented memory architecture and systems and methods using the same Wayland Bart Holland
7,139,213	US	5/12/2004	Multiple data path memories G. R. Mohan Rao
10/850,719	US	5/20/2004	Pipelined Semiconductor memories and systems G. R. Mohan Rao
10/665,906	US	9/18/2003	Memories for electronic systems G. R. Mohan Rao
60/819,296	US	07/07/2006	Low power memories with selective precharge G. R. Mohan Rao
60/819,263	US	07/07/2006	Novel addressing scheme in semiconductor memories for reduced power consumption and high speed G. R. Mohan Rao

Assignor represents, warrants and covenants that:

(1) Assignor has the full power and authority, and has obtained all third party consents, approvals and/or other authorizations required to enter into this Agreement and to carry out its obligations hereunder, including the assignment of the Patent Rights to Assignee; and

(2) Assignor owns, and by this document assigns to Assignee, all right, title, and interest to the Patent Rights, including, without limitation, all right, title, and interest to sue for infringement of the Patent Rights. Assignor has obtained and properly recorded previously executed assignments for the Patent Rights as necessary to fully perfect its rights and title therein in accordance with governing law and regulations in each respective jurisdiction.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

Assignor will, at the reasonable request of Assignee and without demanding any further consideration therefore, do all things necessary, proper, or advisable, including without limitation, the execution, acknowledgment, and recordation of specific assignments, oaths, declarations, and other documents on a country-by-country basis, to assist Assignee in obtaining, perfecting, sustaining, and/or enforcing the Patent Rights, at no cost to Assignor. Such assistance will include providing, and obtaining from the respective inventors, prompt production of pertinent facts and documents, giving of testimony, execution of petitions, oaths, powers of attorney, specifications, declarations or other papers, and other assistance reasonably necessary for filing patent applications, complying with any duty of disclosure, and conducting prosecution, reexamination, reissue, interference or other priority proceedings, opposition proceedings, cancellation proceedings, public use proceedings, infringement or other court actions and the like with respect to the Patent Rights. With prior written approval by Assignee, Assignee will pay Assignor's reasonable costs and expenses.

The terms and conditions of this Assignment of Patent Rights will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed at Richardson, Texas on April 23, 2007.

ASSIGNOR:

Silicon Aquarius, Incorporated

By: G R Mohan Rao
Name: G. R. MOHAN RAO
Title: PRESIDENT
(Signature MUST be notarized)

STATE OF Texas)
) ss.
COUNTY OF Dallas)

On 3rd April, 2007 before me, Jeanene L. Phillips, Notary Public in and for said State, personally appeared G.R. Mohan, personally known to me (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed to the within instrument and acknowledged to me that he/she executed the same in his/her authorized capacity, and that by his/her signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

WITNESS my hand and official seal.

Signature _____

JEANENE L. PHILLIPS
Notary Public, State of Texas
My Commission Expires
March 28, 2009
(Seal)