# Electronic Version v1.1 Stylesheet Version v1.1

SUBMISSION TYPE:	CORRECTIVE ASSIGNMENT	
NATURE OF CONVEYANCE:	Corrective Assignment to correct the error on Page 2 in serial number 11968899, which should be 11967899, on the assignment previously recorded on Reel 024252 Frame 0056. Assignor(s) hereby confirms the assignment from Chipldea to Synopsys, Inc	

### **CONVEYING PARTY DATA**

Name	Execution Date
SNPS PORTUGAL, LDA	04/19/2010
MIPSABG CHIPIDEA, LDA	04/19/2010
CHIPIDEA MICROELECTRONICA S.A.	04/19/2010

#### **RECEIVING PARTY DATA**

Name:	Synopsys, Inc.	
Street Address:	700 East Middlefield Road	
City:	Mountain View	
State/Country:	CALIFORNIA	
Postal Code:	94043	

#### PROPERTY NUMBERS Total: 1

Property Type	Number	
Application Number:	11967899	

### CORRESPONDENCE DATA

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Address Line 1: 901 Campisi Way

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Address Line 4: Campbell, CALIFORNIA 95008

ATTORNEY DOCKET NUMBER:	SYN-C001
NAME OF SUBMITTER:	Jeanette S. Harms

501259882 PATENT REEL: 024826 FRAME: 0061

OP \$40 00 11967899

Total Attachments: 5

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PATENT REEL: 024826 FRAME: 0062

## TO:BEVER HOFFMAN & HARMS, LLP COMPANY:901 CAMPISI WAY



## UNITED STATES PATENT AND TRADEMARK OFFICE

UNDER SECRETARY OF COMMERCE FOR INTELLECTUAL PROPERTY AND DIRECTOR OF THE UNITED STATES PATENT AND TRADEMARK OFFICE



\*501151933A\*

APRIL 19, 2010

PTAS

BEVER HOFFMAN & HARMS, LLP 901 CAMPISI WAY SUITE 370 CAMPBELL, CA 95008

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RECORDATION DATE: 04/19/2010

REEL/FRAME: 024252/0056 NUMBER OF PAGES: 1

BRIEF: ASSIGNMENT OF ASSIGNOR'S INTEREST (SEE DOCUMENT FOR DETAILS). DOCKET NUMBER: SYN-CHIPIDEA

ASSIGNOR:

SNPS PORTUGAL, LDA

DOC DATE: 04/19/2010

ASSIGNOR:

MIPSABG CHIPIDEA, LDA

DOC DATE: 04/19/2010

ASSIGNOR:

CHIPIDEA MICROELECTRONICS S.A.

DOC DATE: 04/19/2010

Assignee:

SYNOPYS, INC.

700 EAST MIDDLEFIELD ROAD

MOUNTAIN VIEW, CALIFORNIA 94043

P.O. Box 1450, Alexandria, Virginia 22313-1450 - www.userto.gov

**REEL: 024826 FRAME: 0063** 

From: USPTO Page: 3/6 Date: 4/19/2010 6:03:59 PM

#### TO:BEVER HOFFMAN & HARMS, LLP COMPANY:901 CAMPISI WAY

024252/0056 PAGE 2

SERIAL NUMBER: 119501/9 FILING DATE: 12/04/2007

PATENT NUMBER: ISSUE DATE:

TITLE: DATA RECOVERY ARCHITECTURE (CDR) FOR LOW-VOLTAGE DIFFERENTIAL

SIGNALING (LVDS) VIDEO TRANSCEIVER APPLICATIONS

SERIAL NUMBER: 11968101 FILING DATE: 12/31/2007

PATENT NUMBER: ISSUE DATE:

TITLE: CLASS D AMPLIFIER HAVING PWM CIRCUIT WITH LOOK-UP TABLE

SERIAL NUMBER: 11967936 FILING DATE: 12/31/2007

PATENT NUMBER: ISSUE DATE:

TITLE: HIGH DEFINITION MEDIA INTERFACE CONTROLLER HAVING A MODULAR DESIGN

INTERNAL BUS STRUCTURE, AND APPLICATIONS THEREOF

SERIAL NUMBER: 11968108 FILING DATE: 12/31/2007

PATENT NUMBER: ISSUE DATE:

TITLE: AMPLIFIER GAIN CONTROL

SERIAL NUMBER: 1196/891 FILING DATE: 12/31/2007

PATENT NUMBER: ISSUE DATE:

TITLE: GPS BASEBAND ARCHITECTURE

SERIAL NUMBER: 11968112 FILING DATE: 12/31/2007

PATENT NUMBER: ISSUE DATE:

TITLE: VOLTAGE-CONTROLLED OSCILLATOR

SERIAL NUMBER: 11968103 FILING DATE: 12/31/2007

PATENT NUMBER: ISSUE DATE:

TITLE: LOW NOISE AMPLIFIER

SERIAL NUMBER: 11968899 > //967899 FILING DATE: 01/03/2008

PATENT NUMBER: ISSUE DATE:

TITLE: SPLIT BODY SWELLING PACKER

SERIAL NUMBER: 11971611 FILING DATE: 01/09/2008

PATENT NUMBER: ISSUE DATE:

TITLE: PROGRAMMABLE MODULAR CIRCUIT FOR TESTING AND CONTROLLING A SYSTEM-

ON-A-CHIP INTEGRATED CIRCUIT, AND APPLICATIONS THEREOF

SERIAL NUMBER: 12211786 FILING DATE: 09/16/2008

PATENT NUMBER: ISSUE DATE:

TITLE: HIGH SPEED PLL CLOCK MULTIPLIER

SERIAL NUMBER: 12369412 FILING DATE: 02/11/2009

PATENT NUMBER: ISSUE DATE: TITLE: DIFFERENTIAL AMPLIFIER AND APPLICATIONS THEREOF

SERIAL NUMBER: 12057171 FILING DATE: 03/27/2008

PATENT NUMBER: ISSUE DATE:

TITLE: DC-DC CONVERTER

SERIAL NUMBER: 12608863 FILING DATE: 10/29/2009

PATENT NUMBER: ISSUE DATE:

TITLE: PROGRAMMABLE IF OUTPUT RECEIVER, AND APPLICATIONS THEREOF

REEL: 024826 FRAME: 0064

From: USPTO Page: 4/6 Date: 4/19/2010 6:03:59 PM

#### TO:BEVER HOFFMAN & HARMS, LLP COMPANY:901 CAMPISI WAY

024252/0056 PAGE 3

SERIAL NUMBER: 09415874 FILING DATE: 10/08/1999 PATENT NUMBER: 6166595 ISSUE DATE: 12/26/2000 TITLE: LINEARIZATION TECHNIQUE FOR ANALOG TO DIGITAL CONVERTERS

 SERIAL NUMBER:
 09521013
 FILING DATE:
 03/08/2000

 PATENT NUMBER:
 6310515
 ISSUE DATE:
 10/30/2001

TITLE: CMOS TRACK AND HOLD AMPLIFIER

 SERIAL NUMBER:
 10866438
 FILING DATE:
 06/12/2004

 PATENT NUMBER:
 6970120
 ISSUE DATE:
 11/29/2005

TITLE: METHOD AND APPARATUS FOR START-UP OF ANALOG-TO-DIGITAL CONVERTERS

SERIAL NUMBER: 11150025 FILING DATE: 06/10/2005
PATENT NUMBER: 7129866 ISSUE DATE: 10/31/2006
TITLE: METHOD AND APPARATUS FOR OPERATING A DELTA SIGMA ADC CIRCUIT

SERIAL NUMBER: 11149899 FILING DATE: 06/10/2005
PATENT NUMBER: 7129874 ISSUE DATE: 10/31/2006
TITLE: METHOD AND APPARATUS FOR OPERATING A PIPELINED ADC CIRCUIT

 SERIAL NUMBER:
 11151934
 FILING DATE:
 06/13/2005

 PATENT NUMBER:
 7221299
 ISSUE DATE:
 05/22/2007

TITLE: METHOD AND APPARATUS FOR AN ADC CIRCUIT WITH WIDER INPUT SIGNAL

SWING

SERIAL NUMBER: FILING DATE: 07/31/2009

PATENT NUMBER: ISSUE DATE:

PCT NUMBER: US0952459

TITLE: HIGH SPEED PLL CLOCK MULTIPLIER

SERIAL NUMBER: FILING DATE: 10/29/2009

PATENT NUMBER: ISSUE DATE:

PCT NUMBER: US0962628

TITLE: PROGRAMMABLE IF OUTPUT RECEIVER, AND APPLICATIONS THEREOF

ASSIGNMENT SERVICES BRANCH PUBLIC RECORDS DIVISION

**REEL: 024826 FRAME: 0065** 

## **CHIPIDEA CONFIRMATORY ASSIGNMENT**

This Chipidea Confirmatory Assignment (this "<u>Assignment</u>") is entered as of April 19, 2010 (the "<u>Effective Date</u>") by and between Synopsys, Inc. ("<u>Buyer</u>"), a corporation organized and existing under the laws of Delaware, USA and SNPS Portugal, Lda. a Portuguese company with registered head office at Taguspark, Av. Dr. Mário Soares, 33 - Porto Salvo, Oeiras, tax payer no. 503835420, registered at the Commercial Registry Office of Cascais, with a share capital of €5.557.143, (previously MIPSABG CHIPIDEA, Lda; previously Chipidea Microelectronica S.A.) and its affiliates (including Synopsys Technologies Holding, LLC (previously MIPS Technologies Holding LLC), a Delaware company) (collectively, "Seller"),

#### **BACKGROUND**

- A. Pursuant to that certain Membership Interest Purchase Agreement, dated May 7, 2009, by and between Buyer and MIPS Technologies, Inc., a Delaware corporation, Buyer has purchased all of the business of Seller, including but not limited to the patents and patent applications listed in <a href="Exhibit A">Exhibit A</a> (the "Patent Assets").
  - B. As of the date of Buyer's purchase, Seller was the owner of record of the Patent Assets.
  - C. Buyer and Seller desire for Buyer to be the owner of record of the Patent Assets.

Now, therefore, for good and valuable consideration, the receipt of which is hereby acknowledged, Buyer and Seller agree as follows:

- 1. Seller has sold, assigned, and transferred and does hereby sell, assign, and transfer to Buyer, for itself and its successors, transferees, and assignees, (a) the entire worldwide right, title, and interest in and to the Patent Assets, including any right of priority; (b) any provisional, divisional, continuation, substitute, renewal, reissue, and other related applications thereto which have been or may be filed in the United States or elsewhere in the world; (c) any patents which may be granted on any of the applications set forth in (a) and (b) above; and (d) the right to sue in its own name and to recover for past infringement of any or all of any applications or patents issuing therefrom together with all rights to recover damages for infringement of provisional rights.
- 2. Seller hereby grants to Buyer a limited power of attorney to do the following on behalf of Seller in order to carry out the intent of this Assignment: (1) execute all oaths, assignments, powers of attorney, applications, and other papers necessary or desirable to fully secure to Buyer the rights, titled and interests herein conveyed; and (2) generally do all lawful acts that Buyer shall consider desirable for securing, maintaining, and enforcing worldwide patent protection relating to the Patent Assets and for vesting in Buyer the rights, titles, and interests herein conveyed.

Duly Authorized Representative of Seller

Douglas Lowell W

Manager

Duly Authorized Representative of Buyer

Brian E. Cabrera

VP, General Counsel, & Corporate Secretary

Date of Signature

19 April 2010, 10:38 AM

Date of Signature

04/19/10 , 10:38 AM

# EXHIBIT A TO CHIPIDEA CONFIRMATORY ASSIGNMENT (CORRECTED)

# **Listing of Patent Assets**

DOCKET NO.	FILING DAT	E SERIAL NO.	ISSUE DATE	PATENT NO.
SYN-1213F1 US	10/8/1999	09/415,874	12/26/2000	6,166,595
SYN-1214 US	3/8/2000	09/521,013	10/30/2001	6,310,515
SYN-1215 US	6/12/2004	10/866,438	11/29/2005	6,970,120
SYN-1216 US	6/10/2005	11/150,025	10/31/2006	7,129,866
SYN-1217 US	6/10/2005	11/149,899	10/31/2006	7,129,874
SYN-1218 US	6/13/2005	11/151,934	5/22/2007	7,221,299
SYN-1219 US	12/4/2007	11/950,179		
SYN-1220 US	12/31/2007	11/968,101		
SYN-1221 US	12/31/2007	11/967,936		
SYN-1222 US	12/31/2007	11/968,108		
SYN-1223 US	12/31/2007	11/967,891		
SYN-1224 US	12/31/2007	11/968,112		
SYN-1225 US	12/31/2007	11/968,103		
SYN-1226 US	12/31/2007	11/96 <u>7</u> ,899		
SYN-1227 US	1/9/2008	11/971,611		
SYN-1229 US	9/16/2008	12/211,786		
SYN-1229F1 WO	7/31/2009	PCT/US09/52459		
SYN-1230 US	2/11/2009	12/369,412		
SYN-1231 US	3/27/2008	12/057,171		
SYN-1232 US	10/29/2009	12/608,863		
SYN-1232F1 WO	10/29/2009	PCT/US09/62628		

**RECORDED: 08/11/2010** 

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PATENT REEL: 024826 FRAME: 0067