PATENT ASSIGNMENT

Electronic Version v1.1
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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Cirrus Logic, Inc.	08/24/2010

RECEIVING PARTY DATA

Name:	Huai Technologies, LLC
Street Address:	2711 Centerville Road, Suite 400
City:	Wilmington
State/Country:	DELAWARE
Postal Code:	19808

PROPERTY NUMBERS Total: 67

Property Type	Number
Patent Number:	5442588
Patent Number:	5452244
Patent Number:	5567963
Patent Number:	5529945
Patent Number:	5473566
Patent Number:	5568431
Patent Number:	5473573
Patent Number:	5583822
Patent Number:	5701270
Patent Number:	5500819
Patent Number:	5506810
Patent Number:	5570320
Patent Number:	5530392
Patent Number:	5535165
Patent Number:	5537353

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Patent Number:	5600606
Patent Number:	5581513
Patent Number:	5585744
Patent Number:	5644255
Patent Number:	5592077
Patent Number:	5596291
Patent Number:	5598374
Patent Number:	5745428
Patent Number:	5657285
Patent Number:	5612644
Patent Number:	5636174
Patent Number:	5654932
Patent Number:	5657281
Patent Number:	5663984
Patent Number:	5687132
Patent Number:	5701143
Patent Number:	5732024
Patent Number:	5914900
Patent Number:	5909401
Patent Number:	5910919
Patent Number:	5761694
Patent Number:	5764082
Patent Number:	5815456
Patent Number:	5829016
Patent Number:	5835965
Patent Number:	5844856
Patent Number:	5848101
Patent Number:	5861767
Patent Number:	5906003
Patent Number:	5950219
Patent Number:	5920885
Patent Number:	6282603
Patent Number:	5945974
Patent Number:	5978293
Patent Number:	5982696

Patent Number:	6025840
Patent Number:	6058464
Patent Number:	6118461
Patent Number:	6041389
Patent Number:	6108015
Patent Number:	6157366
Patent Number:	6510098
Patent Number:	6513130
Patent Number:	5455526
Patent Number:	6425020
Application Number:	08418649
Application Number:	08349894
Application Number:	08340163
Application Number:	08725274
Application Number:	08519992
Application Number:	08512574
Application Number:	08611061

CORRESPONDENCE DATA

Fax Number: (302)397-2678

Correspondence will be sent via US Mail when the fax attempt is unsuccessful.

Phone: (310)6915449

Email: AssignmentRecordation@gmail.com

Correspondent Name: Huai Technologies, LLC

Address Line 1: 2711 Centerville Road, Suite 400

Address Line 4: Wilmington, DELAWARE 19808

NAME OF SUBMITTER:	Rebecca Tu

Total Attachments: 20

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EXHIBIT B

ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, Seller, Cirrus Logic, Inc., a Delaware Corporation having an office at 2901 Via Fortuna, Austin, Texas 78746, U.S.A. (***"Assignor"***), does hereby sell, assign, transfer, and convey unto Huai Technologies, LLC, a Delaware company, having an office at 2711 Centerville Road, Suite 400, Wilmington, Delaware 19808, U.S.A. (***"Assignee"***), or its designees, all right, title, and interest that exist today and may exist in the future in and to all of the following (collectively, the ***"Patent Rights"***), including:

(a) the provisional patent applications, patent applications and patents listed in the **Attachment** hereto (***"Listed Patents"***);

(b) all patents or patent applications to which any of the foregoing claim priority;

(c) all patents or patent applications filed by Assignee (or any subsequent transferee of any Patent Rights) after the date of this Assignment of Patent Rights (i) to which any of the foregoing forms a basis for priority, (ii) that are reissues, reexaminations, extensions, continuations, continuations in part, continuing prosecution applications, or divisions of any of the foregoing, and/or (iii) that are foreign counterparts to any of the foregoing, including certificates of invention, utility models, industrial design protection, design patent protection, and other governmental grants;

(d) all patents, patent applications, and/or other governmental grants or issuances of any type that (i) are filed by Assignee (or any transferee of any Patent Rights) after the date of this Assignment of Patent Rights and claim priority to any Listed Patent and (ii) are related to any of the inventions, invention disclosures, and discoveries described in any of the Listed Patents to the extent that any such inventions, invention disclosures, and discoveries (x) are included in any claim in the Listed Patents, (y) are subject matter capable of being reduced to a patent claim in any reissue or reexamination proceedings brought on any of the Listed Patents and/or (z) could have been and/or could be included as a claim in any continuations, continuing prosecution applications, requests for continuing examinations and/or divisions of the Listed Patents;

(e) rights to apply in any or all countries of the world for patents, certificates of invention, utility models, industrial design protections, design patent protections or other governmental grants of any type related to the any of the foregoing categories (a), (b), (c) and/or (d), including, without limitation, under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement or understanding;

(f) causes of action (whether currently pending, filed, or otherwise) and other enforcement rights, including, without limitation, all rights under the Listed Patents and/or under or on account of any of the foregoing categories (b), (c), (d) and/or (e) to

(i) damages,
(ii) injunctive relief and
(iii) other remedies of any kind

for past, current and future infringement; and

(g) all rights to collect royalties and other payments under or on account of any of the Listed Patents or any of the foregoing categories (b) through (f), except for compensation (e.g. royalties) due to Assignor pursuant to any agreements, executed by Assignor prior to the date of this Assignment of Patent Rights, which granted non-exclusive licenses under the Listed Patents or interests or rights in the foregoing category (f).

The terms and conditions of this Assignment of Patent Rights will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed at AUSTIN, TEXAS on 24 AUGUST 2010.

ASSIGNOR

Cirrus Logic, Inc.

By: _____

Name: JASON RHODE

Title: PRESIDENT & CHIEF EXECUTIVE OFFICER

(Signature MUST be notarized)

STATE OF TEXAS)
) ss.
COUNTY OF TRAVIS)

On 24 AUGUST 2010, before me, _____, Notary Public in and for said State, personally appeared JASON RHODE, personally known to me (or proved to me on the basis of satisfactory evidence) to be the person whose name is subscribed to the within instrument and acknowledged to me that he/she executed the same in his/her authorized capacity, and that by his/her signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

WITNESS my hand and official seal.

Signature _____ (Seal)

BONNIE J. NIEMTSCHK
My Commission Expires
March 19, 2013

Attachment

Listed Patents

Patent No. / Application No.	Country	Title	Inventors	Filing Date
5,442,588	US	Circuits and methods for refreshing a dual bank memory	Runas, Michael E.	8/16/1994
EP0698887	EP	Circuits and methods for refreshing a dual bank memory	Runas, Michael E.	8/10/1995
DE69517888.1	DE	Circuits and methods for refreshing a dual bank memory	Runas, Michael E.	8/10/1995
FR95410085.5	FR	Circuits and methods for refreshing a dual bank memory	Runas, Michael E.	8/10/1995
GB95410085.5	GB	Circuits and methods for refreshing a dual bank memory	Runas, Michael E.	8/10/1995
JP3186534	JP	Method and circuit for refreshing relative bank memory	Runas, Michael E.	8/14/1995
KR10-0176739	KR	Circuits and methods for refreshing a dual bank memory	Runas, Michael E.	8/14/1995
5,452,244	US	Electronic memory and methods for making and using the same	Mohan Rao, G. R.	8/10/1994
5,567,963	US	Multi-bit data storage location	Rao, G. R. Mohan	3/27/1995
5,529,945	US	Methods for fabricating a multi-bit storage cell	Rao, G. R. Mohan	3/27/1995
EP95401853.7	EP	An improved electronic memory and methods for making and using the same	Rao, G. R. Mohan	8/8/1995
JP07-203389	JP	Improved electronic memory, fabrication and usage therof	Rao, G. R. Mohan	8/9/1995
KR10-1995-0024512	KR	An improved electronic memory and methods for making and using the same	Rao, G. R. Mohan	8/9/1995
5,473,566	US	Memory architecture and devices, systems and methods utilizing the same	Rao, G. R. Mohan	9/12/1994
5,568,431	US	Memory architecture and devices, systems and methods utilizing the same	Rao, G. R. Mohan	9/21/1995
PCT/US1995/012088	WO	An improved memory architecture and devices, systems and methods utilizing the same	Rao, G. R. Mohan	9/11/1995
EP0781443	EP	Memory device and data processing system with such a memory device	Rao, G. R. Mohan	9/11/1995
DE69516881.9	DE	Memory device and data processing system with such a memory device	Rao, G. R. Mohan	9/11/1995

Patent No. / Application No.	Country	Title	Inventors	Filing Date
FR0781443	FR	Memory device and data processing system with such a memory device	Rao, G. R. Mohan	9/11/1995
IT0781443	IT	Memory device and data processing system with such a memory device	Rao, G. R. Mohan	9/11/1995
NL0781443	NL	Memory device and data processing system with such a memory device	Rao, G. R. Mohan	9/11/1995
JP08-510422	JP	Memory architecture and devices, systems and methods utilizing the same	Rao, G. R. Mohan	9/11/1995
KR10-0279039	KR	Memory architecture and devices, systems and methods utilizing the same	Rao, G. R. Mohan	9/11/1995
KR10-2000-7005159	KR	Memory architecture and devices, systems and methods utilizing the same	Rao, G. R. Mohan	5/12/2000
5,473,573	US	Single chip controller-memory device and a memory architecture and methods suitable for implementing the same	Rao, G. R. Mohan	5/9/1994
5,583,822	US	Single chip controller-memory device and a memory architecture and methods suitable for implementing the same	Rao, G. R. Mohan	11/1/1995
5,701,270	US	Single chip controller-memory device with interbank cell replacement capability and a memory architecture and methods suitble for implementing the same	Mohan Rao, G. R.	2/1/1996
EP0895246	EP	A single chip controller-memory device and a memory architecture and methods suitable for implementing the same	Rao, G. R. Mohan	5/8/1995
DE69528851.2	DE	A single chip controller-memory device and a memory architecture and methods suitable for implementing the same	Rao, G. R. Mohan	5/8/1995
FR0895246	FR	A single chip controller-memory device and a memory architecture and methods suitable for implementing the same	Rao, G. R. Mohan	5/8/1995
GB0895246	GB	A single chip controller-memory device and a memory architecture and methods suitable for implementing the same	Rao, G. R. Mohan	5/8/1995

Patent No. / Application No.	Country	Title	Inventors	Filing Date
NL0895246	NL	A single chip controller-memory device and a memory architecture and methods suitable for implementing the same	Rao, G. R. Mohan	5/8/1995
PCT/US1995/005761	WO	A single chip controller-memory device and a memory architecture and methods suitable for implementing the same	Rao, G. R. Mohan	5/8/1995
EP0760155	EP	A single chip controller-memory device and a memory architecture and methods suitable for implementing the same	Rao, G. R. Mohan	5/8/1995
DE69513516.3	DE	A single chip controller-memory device and a memory architecture and methods suitable for implementing the same	Rao, G. R. Mohan	5/8/1995
FR0760155	FR	A single chip controller-memory device and a memory architecture and methods suitable for implementing the same	Rao, G. R. Mohan	5/8/1995
GB0760155	GB	A single chip controller-memory device and a memory architecture and methods suitable for implementing the same	Rao, G. R. Mohan	5/8/1995
IE0760155	IE	A single chip controller-memory device and a memory architecture and methods suitable for implementing the same	Rao, G. R. Mohan	5/8/1995
NL0760155	NL	A single chip controller-memory device and a memory architecture and methods suitable for implementing the same	Rao, G. R. Mohan	5/8/1995
HK1010011	HK	A single chip controller-memory device and a memory architecture and methods suitable for implementing the same	Rao, G. R. Mohan	9/18/1998
JP07-529176	JP	A single chip controller-memory device and a memory architecture and methods suitable for implementing the same	Rao, G. R. Mohan	5/8/1995
KR10-1996-0706403	KR	Single chip controller-memory device and memory architecture and methods suitable for implementing the same	Rao, G. R. Mohan	5/8/1995
5,500,819	US	Circuits, systems and methods for improving page accesses and block transfers in a memory system	Runas, Michael E.	9/30/1994

Patent No. / Application No.	Country	Title	Inventors	Filing Date
PCT/US1995/012903	WO	Circuits, systems and methods for improving page accesses and block transfers in a memory system	Runas, Michael E.	9/29/1995
EP0784851	EP	Circuits, systems and methods for improving page accesses and block transfers in a memory system	Runas, Michael E.	9/29/1995
BE0784851	BE	Circuits, systems and methods for improving page accesses and block transfers in a memory system	Runas, Michael E.	9/29/1995
DE69510077.7	DE	Circuits, systems and methods for improving page accesses and block transfers in a memory system	Runas, Michael E.	9/29/1995
FR0784851	FR	Circuits, systems and methods for improving page accesses and block transfers in a memory system	Runas, Michael E.	9/29/1995
GB0784851	GB	Circuits, systems and methods for improving page accesses and block transfers in a memory system	Runas, Michael E.	9/29/1995
IE0784851	IE	Circuits, systems and methods for improving page accesses and block transfers in a memory system	Runas, Michael E.	9/29/1995
IT0784851	IT	Circuits, systems and methods for improving page accesses and block transfers in a memory system	Runas, Michael E.	9/29/1995
NL0784851	NL	Circuits, systems and methods for improving page accesses and block transfers in a memory system	Runas, Michael E.	9/29/1995
JP08-512143	JP	Circuits, systems and methods for improving page accesses and block transfers in a memory system	Runas, Michael E.	9/29/1995
KR10-1997-0702035	KR	Circuits, systems and methods for improving page accesses and block transfers in a memory system	Runas, Michael E.	9/29/1995
5,606,810	US	Dual bank memory and systems using the same	Runas, Michael E.	8/16/1994
5,570,320	US	Dual bank memory system with output multiplexing and methods using the same	Runas, Michael E.	11/6/1995

Patent No. / Application No.	Country	Title	Inventors	Filing Date
PCT/US1995/010446	WO	A dual bank memory and systems using the same	Runas, Michael E.	8/15/1995
EP0803124	EP	A dual bank memory and systems using the same	Runas, Michael E.	8/15/1995
DE69509134.4	DE	A dual bank memory and systems using the same	Runas, Michael E.	8/15/1995
FR0803124	FR	A dual bank memory and systems using the same	Runas, Michael E.	8/15/1995
GB0803124	GB	A dual bank memory and systems using the same	Runas, Michael E.	8/15/1995
NL0803124	NL	A dual bank memory and systems using the same	Runas, Michael E.	8/15/1995
HK1004169	HK	A dual bank memory and systems using the same	Runas, Michael E.	4/28/1998
JP3046075	JP	A dual bank memory and systems using the same	Runas, Michael E.	8/15/1995
KR10-0245535	KR	A dual bank memory and systems using the same	Runas, Michael E.	8/15/1995
IE0803124	IE	A dual bank memory and systems using the same	Runas, Michael E.	8/15/1995
5,530,392	US	Bus driver/receiver circuitry and systems and methods using the same	Runas, Michael E.; Patel, Kirit B.	4/11/1995
5,535,165	US	Circuits, systems and methods for testing integrated circuit devices including logic and memory circuitry	Davis, Phillip D.; Sharma, Sudhir; Long, Hai	6/30/1995
5,537,353	US	Low pin count-wide memory devices and systems and methods using the same	Rao, G. R. Mohan; Taylor, Ronald T.; Sharma, Sudhir	8/31/1995
5,600,606	US	Low pin count - wide memory devices using non-multiplexed addressing and systems and methods using t	Rao, G. R. Mohan	3/7/1996
EP0760512	EP	Low pin count - wide memory devices and systems and methods using the same	Rao, G. R. Mohan; Taylor, Ronald T.; Sharma, Sudhir	10/31/1995
GB0760512	GB	Low pin count - wide memory devices and systems and methods using the same	Rao, G. R. Mohan; Taylor, Ronald T.; Sharma, Sudhir	10/31/1995
IE0760512	IE	Low pin count - wide memory devices and systems and methods using the same	Rao, G. R. Mohan; Taylor, Ronald T.; Sharma, Sudhir	10/31/1995
HK1010012	HK	Low pin count - wide memory devices and systems and methods using the same	Rao, G. R. Mohan; Taylor, Ronald T.; Sharma, Sudhir	9/18/1998

Patent No. / Application No.	Country	Title	Inventors	Filing Date
JP4128234	JP	Memory element, processing system, method for control of memory element and method for operation of dynamic random-access memory	Rao, G. R. Mohan; Taylor, Ronald T.; Sharma, Sudhir	11/9/1995
KR10-1996-0002003	KR	Low pin count - wide memory devices and systems and methods using the same	Rao, G. R. Mohan; Taylor, Ronald T.; Sharma, Sudhir	1/30/1996
TW079238	TW	Low pin count - wide memory devices and systems and methods using the same	Rao, G. R. Mohan; Taylor, Ronald T.; Sharma, Sudhir	10/19/1995
5,581,513	US	Continuous page random access memory and systems and methods using the same	Mohan Rao, G. R.	4/19/1995
PCT/US1996/005313	WO	A continuous page random access memory and systems and methods using the same	Mohan Rao, G. R.	4/19/1996
EP0766866	EP	A continuous page random access memory and systems and methods using the same	Mohan Rao, G. R.	4/19/1996
GB0766866	GB	A continuous page random access memory and systems and methods using the same	Mohan Rao, G. R.	4/19/1996
IE0766866	IE	A continuous page random access memory and systems and methods using the same	Mohan Rao, G. R.	4/19/1996
JP2931412	JP	A continuous page random access memory and systems and methods using the same	Mohan Rao, G. R.	4/19/1996
KR10-0295031	KR	A continuous page random access memory and systems and methods using the same	Mohan Rao, G. R.	4/19/1996
5,585,744	US	Circuits systems and methods for reducing power loss during transfer of data across a conductive line	Runas, Michael E.; Taylor, Ronald T.	10/13/1995
5,644,255	US	Circuits systems and methods for reducing power loss during transfer of data across a conductive line	Taylor, Ronald T.	3/21/1996
EP96307403.4	EP	Circuits, systems and methods for reducing power loss during transfer of data across a conductive line	Runas, Michael E.; Taylor, Ronald T.	10/11/1996
HK98110706.7	HK	Circuits, systems and methods for reducing power loss during transfer of data across a conductive line	Runas, Michael E.; Taylor, Ronald T.	10/11/1996

Patent No. / Application No.	Country	Title	Inventors	Filing Date
JP08-271222	JP	Circuit, system and method for decreasing power loss during data transmission through conductive wire	Runas, Michael E.; Taylor, Ronald T.	10/14/1996
KR10-0212585	KR	Circuits, systems and methods for reducing power loss during transfer of data across a conductive line	Runas, Michael E.; Taylor, Ronald T.	10/14/1996
5,592,077	US	Circuits, systems and methods for testing ASIC and RAM memory devices	Runas, Michael E.; Patel, Kirit B.	2/13/1995
08/418,649	US	Circuits, systems and methods for the high speed transfer of data across a conductive line	Runas, Michael E.	4/10/1995
5,596,291	US	Circuits, systems and methods for the high speed transfer of data across a conductive line	Runas, Michael E.	5/2/1996
5,598,374	US	Pipelined address memories, and systems and methods using the same	Rao, G. R. Mohan	7/14/1995
5,745,428	US	Pipelined address memories, and systems and methods using the same	Rao, G. R. Mohan	6/14/1996
5,657,285	US	Pipelined address memories, and systems and methods using the same	Rao, G. R. Mohan	6/14/1996
PCT/IB1996/001001	WO	Pipelined address memories, and systems and methods using the same	Rao, G. R. Mohan	7/12/1996
EP0839375	EP	Pipelined address memory system and method of operating such system	Rao, G. R. Mohan	7/12/1996
DE69602946.4	DE	Pipelined address memory system and method of operating such system	Rao, G. R. Mohan	7/12/1996
FR0839375	FR	Pipelined address memory system and method of operating such system	Rao, G. R. Mohan	7/12/1996
GB0839375	GB	Pipelined address memory system and method of operating such system	Rao, G. R. Mohan	7/12/1996
IE0839375	IE	Pipelined address memory system and method of operating such system	Rao, G. R. Mohan	7/12/1996
NL0839375	NL	Pipelined address memory system and method of operating such system	Rao, G. R. Mohan	7/12/1996

Patent No. / Application No.	Country	Title	Inventors	Filing Date
JP09-506502	JP	Pipelined address memories, and systems and methods using the same	Rao, G. R. Mohan	7/12/1996
KR10-1998-0700293	KR	Pipelined address memories, and systems and methods using the same	Rao, G. R. Mohan	7/12/1996
5,612,644	US	Circuits, systems and methods for controlling substrate bias in integrated circuits	Runas, Michael E.	8/31/1995
PCT/US1996/013869	WO	Circuits, systems and methods for controlling substrate bias in integrated circuits	Runas, Michael E.	8/29/1996
EP96930621.6	EP	Circuits, systems and methods for controlling substrate bias in integrated circuits	Runas, Michael E.	8/29/1996
JP09-510555	JP	Circuits, systems and methods for controlling substrate bias in integrated circuits	Runas, Michael E.	8/29/1996
KR10-1997-0702852	KR	Circuits, systems and methods for controlling substrate bias in integrated circuits	Runas, Michael E.	8/29/1996
5,636,174	US	Fast cycle time-low latency dynamic random access memories and systems and methods using the same	Rao, G. R. Mohan	1/11/1996
5,654,932	US	Memory devices with selectable access type and methods using the same	Rao, G. R. Mohan	10/4/1995
EP96307293.9	EP	Memory devices with selectable access type and systems and methods using the same	Rao, G. R. Mohan	10/4/1996
HK98110704.9	HK	Memory devices with selectable access type and systems and methods using the same	Rao, G. R. Mohan	10/4/1996
JP2978784	JP	Memory, processing system and access method	Rao, G. R. Mohan	10/4/1996
5,657,281	US	Systems and methods for implementing inter-device cell replacements	Rao, G. R. Mohan	3/11/1996
EP97301404.6	EP	Systems and methods for implementing inter-device cell replacements	Rao, G. R. Mohan	3/4/1997
HK98101986.7	HK	Systems and methods for implementing inter-device cell replacements	Rao, G. R. Mohan	3/4/1997
JP4031547	JP	Memory system and method for substituting memory cell	Rao, G. R. Mohan	3/6/1997

Patent No. / Application No.	Country	Title	Inventors	Filing Date
JP2006-285332	JP	Memory system and method for substituting memory cell	Rao, Mohan	10/19/2006
KR10-0466953	KR	Systems and methods for implementing inter-device cell replacements	Rao, G. R. Mohan	3/11/1997
TW093775	TW	Systems and methods for implementing inter-device cell replacements	Rao, G. R. Mohan	2/27/1997
5,663,984	US	High performance bus driving/receiving circuits, systems and methods	Runas, Michael E.	5/4/1995
5,687,132	US	Multiple-bank memory architecture and systems and methods using the same	Rao, G. R. Mohan	10/26/1995
EP0771008	EP	Multiple-bank memory architecture and systems and methods using the same	Rao, G. R. Mohan	10/25/1996
HK1010017	HK	Multiple-bank memory architecture and systems and methods using the same	Rao, G. R. Mohan	10/25/1996
IE0771008	IE	Multiple-bank memory architecture and systems and methods using the same	Rao, G. R. Mohan	10/25/1996
JP2828626	JP	Multiple-bank memory architecture and systems and methods using the same	Rao, G. R. Mohan	10/25/1996
KR10-0258672	KR	Multiple-bank memory architecture and systems and methods using the same	Rao, G. R. Mohan	10/25/1996
GB96307730.0	GB	Multiple-bank memory architecture and systems and methods using the same	Rao, G. R. Mohan	10/25/1996
DE69618319.6	DE	Multiple-bank memory architecture and systems and methods using the same	Rao, G. R. Mohan	10/25/1996
NL0771008	NL	Multiple-bank memory architecture and systems and methods using the same	Rao, G. R. Mohan	10/25/1996
FR96307730.0	FR	Multiple-bank memory architecture and systems and methods using the same	Rao, G. R. Mohan	10/25/1996
5,701,143	US	Circuits, systems and methods for improving row select speed in a row select memory device	Rao, G. R. Mohan	1/31/1995
PCT/US1996/001351	WO	Circuits, systems and methods for improving row select speed in a row select memory device	Rao, G. R. Mohan	1/31/1996

Patent No. / Application No.	Country	Title	Inventors	Filing Date
EP96906247.0	EP	Circuits, systems and methods for improving row select speed in a row select memory device	Rao, G. R. Mohan	1/31/1996
HK98104030.7	HK	Circuits, systems and methods for improving row select speed in a row select memory device	Rao, G. R. Mohan	1/31/1996
JP08-523716	JP	Circuits, systems and methods for improving row select speed in a row select memory device	Rao, G. R. Mohan	1/31/1996
KR10-1997-0705219	KR	Circuits, systems and methods for improving row select speed in a row select memory device	Rao, G. R. Mohan	1/31/1996
5,732,024	US	Circuits, systems and methods for modifying data stored in a memory using logic operations	Sharma, Sudhir; Runas, Michael E.; Nally, Robert M.	4/19/1995
5,914,900	US	Circuits, systems and methods for modifying data stored in a memory using logic operations	Sharma, Sudhir; Runas, Michael E.; Nally, Robert M.	7/30/1997
5,909,401	US	Sensing circuitry with boolean logic	Sharma, Sudhir; Runas, Michael E.; Nally, Robert M.	7/30/1997
5,910,919	US	Circuits, systems and methods for modifying data stored in a memory using logic operations	Sharma, Sudhir; Runas, Michael E.; Nally, Robert M.	7/30/1997
PCT/US1996/005523	WO	Circuits, systems and methods for modifying data stored in a memory using logic operations	Sharma, Sudhir; Runas, Michael E.; Nally, Robert M.	4/19/1996
EP0823116	EP	Circuits, systems and methods for modifying data stored in a memory using logic operations	Sharma, Sudhir; Runas, Michael E.; Nally, Robert M.	4/19/1996
DE69602742.9	DE	Circuits, systems and methods for modifying data stored in a memory using logic operations	Sharma, Sudhir; Runas, Michael E.; Nally, Robert M.	4/19/1996
FR0823116	FR	Circuits, systems and methods for modifying data stored in a memory using logic operations	Sharma, Sudhir; Runas, Michael E.; Nally, Robert M.	4/19/1996
GB0823116	GB	Circuits, systems and methods for modifying data stored in a memory using logic operations	Sharma, Sudhir; Runas, Michael E.; Nally, Robert M.	4/19/1996
HK1007912	HK	Circuits, systems and methods for modifying data stored in a memory using logic operations	Sharma, Sudhir; Runas, Michael E.; Nally, Robert M.	4/19/1996
IE0823116	IE	Circuits, systems and methods for modifying data stored in a memory using logic operations	Sharma, Sudhir; Runas, Michael E.; Nally, Robert M.	4/19/1996
NL0823116	NL	Circuits, systems and methods for modifying data stored in a memory using logic operations	Sharma, Sudhir; Runas, Michael E.; Nally, Robert M.	4/19/1996

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JP08-531977	JP	Circuits, systems and methods for modifying data stored in a memory using logic operations	Sharma, Sudhir; Runas, Michael E.; Nally, Robert M.	4/19/1996
KR10-1997-0707383	KR	Circuits, systems and methods for modifying data stored in a memory using logic operations	Sharma, Sudhir; Runas, Michael E.; Nally, Robert M.	4/19/1996
5,761,694	US	Multi-bank memory system and method having addresses switched between the row and column decoders in different banks	Rao, G. R. Mohan	11/30/1995
EP96308653.3	EP	A memory architecture using conserved addressing and systems and methods using the same	Rao, G. R. Mohan	11/29/1996
HK98110705.8	HK	A memory architecture using conserved addressing and systems and methods using the same	Rao, G. R. Mohan	9/18/1998
JP08-322039	JP	Ory sub-system, memory device, processing system and access method	Rao, G. R. Mohan	12/2/1996
JP2001-191969	JP	Memory sub-system, memory device, processing system and accessing method	Rao, G. R. Mohan	6/25/2001
KR10-0227133	KR	A memory architecture using conserved addressing and systems and methods using the same	Rao, G. R. Mohan	11/29/1996
TW086840	TW	A memory architecture using conserved addressing and systems and methods using the same	Rao, G. R. Mohan	11/21/1996
5,764,082	US	Circuits, systems and methods for transferring data across a conductive line	Taylor, Ronald T.	7/29/1996
5,815,456	US	Multibank -- multiport memories and systems and methods using the same	Rao, G.R. Mohan	6/19/1996
EP97304174.2	EP	Multibank -- multiport memories and systems and methods using the same	Rao, G.R. Mohan	6/13/1997
HK98104429.6	HK	Multibank -- multiport memories and systems and methods using the same	Rao, G.R. Mohan	6/13/1997
JP09-159006	JP	Multibank -- multiport memories and systems and methods using the same	Rao, G.R. Mohan	6/16/1997

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KR10-0533305	KR	Multibank -- multiport memories and systems and methods using the same	Rao, G.R. Mohan	6/13/1997
TWNI-096546	TW	Multibank -- multiport memories and systems and methods using the same	Rao, G.R. Mohan	3/19/1997
5,829,016	US	Memory system with multiplexed input-output port and systems and methods using the same	Sharma, Sudhir; Taylor, Ronald T.; Runas, Michael E.; Rao, G.R. Mohan	4/24/1996
5,835,965	US	Memory system with multiplexed input-output port and memory mapping capability	Taylor, Ronald T.; Sharma, Sudhir; Runas, Michael E.	4/24/1996
EP97301835.1	EP	A memory system with multiplexed input-output port and memory mapping capability and systems and methods using the same	Taylor, Ronald T.; Sharma, Sudhir; Runas, Michael E.	3/19/1997
HK98103145.1	HK	A memory system with multiplexed input-output port and memory mapping capability and systems and methods using the same	Taylor, Ronald T; Sharma, Sudhir; Runas, Michael E.	3/19/1997
JP09-100233	JP	Memory, memory system and method for mapping memory device	Taylor, Ronald T.; Sharma, Sudhir; Runas, Michael E.	4/17/1997
TW092144	TW	A memory system with multiplexed input-output port and memory mapping capability and systems and methods using the same	Taylor, Ronald T.; Sharma, Sudhir; Runas, Michael E.	3/17/1997
5,844,856	US	Dual port memories and systems and methods using the same	Taylor, Ronald T.	6/19/1996
EP97304204.7	EP	Dual port memories and systems and methods using the same	Taylor, Ronald T.	6/16/1997
HK98106432.6	HK	Dual port memories and systems and methods using the same	Taylor, Ronald T.	6/16/1997
JP09-161642	JP	Memory system, i/o subsystem device, and method for operating memory device	Taylor, Ronald T.	6/18/1997
KR10-0494201	KR	Dual port memories and systems and methods using the same	Taylor, Ronald T.	5/21/1997
TW095659	TW	Dual port memories and systems and methods using the same	Taylor, Ronald T.	4/16/1997
5,848,101	US	Circuits systems and methods for reducing power loss during transfer of data across an I/O bus	Taylor, Ronald T.	1/26/1996

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5,861,767	US	Digital step generators and circuits, systems and methods using the same	Patel, Kirit B.; Rao, G.R. Mohan	12/3/1996
PCT/US1997/022002	WO	Digital step generators and circuits, systems and methods using the same	Rao, G.R. Mohan; Patel, Kirit B.	12/3/1997
TW112490	TW	Digital step generators and circuits, systems and methods using the same	Rao, G.R. Mohan; Patel, Kirit B.	12/3/1997
5,906,003	US	Memory device with an externally selectable-width I/O port and systems and methods using the same	Runas, Michael E.	4/17/1996
5,950,219	US	Memory banks with pipelined addressing and priority acknowledging and systems and methods using the	Rao, G.R. Mohan	5/2/1996
5,920,886	US	Dynamic random access memory with a normal precharge mode and a priority precharge mode	Rao, G.R. Mohan	6/1/1998
6,282,603	US	Memory with pipelined accessed and priority precharge	Rao, G.R. Mohan	6/1/1998
5,945,974	US	Display controller with integrated half frame buffer and systems and methods using the same	Sharma, Sudhir; Rao, G.R. Mohan; Runas, Michael E.	5/15/1996
EP97301325.3	EP	Display controller with integrated half frame buffer and systems and methods using the same	Sharma, Sudhir; Rao, G.R. Mohan; Runas, Michael E.	2/27/1997
JP09-121139	JP	Display controller, integrated circuit, system and method displaying data on screen of display device	Sharma, Sudhir; Rao, G.R. Mohan; Runas, Michael E.	5/12/1997
HK98104029.0	HK	Display controller with integrated half frame buffer and systems and methods using the same	Sharma, Sudhir; Rao, G.R. Mohan; Runas, Michael E.	2/27/1997
KR10-1997-0007014	KR	Display controller with integrated half frame buffer and systems and methods using the same	Sharma, Sudhir; Rao, G.R. Mohan; Runas, Michael E.	3/4/1997
TW086103038	TW	Display controller with integrated half frame buffer and systems and methods using the same	Sharma, Sudhir; Rao, G.R. Mohan; Runas, Michael E.	3/12/1997
5,978,293	US	Circuitry and methods for dynamically sensing of data in a static random access memory cell	Taylor, Ronald T.	3/19/1998
5,982,696	US	Memories with programmable address decoding and systems and methods using the same	Rao, G.R. Mohan	6/6/1996

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6,025,840	US	Circuits, systems and methods for memory mapping and display control systems using the same	Taylor, Ronald T.	9/27/1995
6,058,464	US	Circuits, systems and method for address mapping	Taylor, Ronald T.	7/9/1996
6,118,461	US	Circuits, systems and methods for memory mapping and display control systems using the same	Taylor, Ronald T.	4/24/1998
PCT/US1996/015583	WO	Circuits, systems and methods for memory mapping and display control systems using the same	Taylor, Ronald T.	9/27/1996
JP09-515068	JP	Circuits, systems and method for address mapping	Taylor, Ronald T.	9/27/1996
KR10-1997-0703465	KR	Circuits, systems and methods for memory mapping and display control systems using the same	Taylor, Ronald T.	9/27/1996
EP96936043.7	EP	Circuits, systems and methods for memory mapping and display control systems using the same	Taylor, Ronald T.	9/27/1996
6,041,389	US	Memory architecture using content addressable memory, and systems and methods using the same	Rao, G. R. Mohan	11/16/1995
EP96308277.1	EP	Memory architecture using content addressable memory, and systems and methods using the same	Rao, G. R. Mohan	11/15/1996
JP2968486	JP	Memory architecture using content addressable memory, and systems and methods using the same	Rao, G. R. Mohan	11/18/1996
HK98110709.4	HK	Memory architecture using content addressable memory, and systems and methods using the same	Rao, G. R. Mohan	11/15/1996
KR10-1996-0054610	KR	Memory architecture using content addressable memory, and systems and methods using the same	Rao, G. R. Mohan	11/16/1996
TW085114065	TW	Memory architecture using content addressable memory, and systems and methods using the same	Rao, G. R. Mohan	11/11/1996
6,106,015	US	Circuits, systems and methods for interfacing processing circuitry with a memory	Cross, Randolph A.	11/2/1995
JP08-292717	JP	Circuits, systems and methods for interfacing processing circuitry with a memory	Cross, Randolph A.	11/5/1996

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EP96307888.6	EP	Methods and circuits for interfacing processing circuitry with memories	Cross, Randolph A.	10/31/1996
KR10-0255259	KR	Circuits, systems and methods for interfacing processing circuitry with a memory	Cross, Randolph A.	11/2/1996
08/349,894	US	Circuits, systems and methods for controlling the display of blocks of data on a display screen	Sharma, Sudhir	12/6/1994
6,157,366	US	Circuits, systems and methods for graphics and video window/display data block transfer via dedicated memory control	Sharma, Sudhir	5/23/1997
PCT/US1995/015847	WO	Circuits, systems and methods for controlling the display of blocks of data on a display screen	Sharma, Sudhir	12/6/1995
EP95944065.2	EP	Circuits, systems and methods for controlling the display of blocks of data on a display screen	Sharma, Sudhir	12/6/1995
JP08-519143	JP	Circuits, systems and methods for graphics and video window/display data block transfer via dedicated memory control	Sharma, Sudhir	12/6/1995
KR10-1997-0703709	KR	Circuits, systems and methods for controlling the display of blocks of data on a display screen	Sharma, Sudhir	6/3/1997
SG39578	SG	Circuits, systems and methods for controlling the display of blocks of data on a display screen	Sharma, Sudhir	12/6/1995
6,510,098	US	Method and apparatus for transferring data in a dual port memory	Taylor, Ronald T.	5/28/1997
08/340,163	US	Circuits, systems, and methods for accounting for defective cells in a memory device	Cross, Randolph A.	11/15/1994
08/725,274	US			10/2/1996
6,513,130	US	Circuits, systems, and methods for accounting for defective cells in a memory device	Cross, Randolph A.	10/4/1996
PCT/US1995/014307	WO	Circuits, systems, and methods for accounting for defective cells in a memory device	Cross, Randolph A.	11/6/1995
JP3647040	JP	Circuits, systems, and methods for accounting for defective cells in a memory device	Cross, Randolph A.	11/6/1995

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KR10-1997-0703246	KR	Circuits, systems, and methods for accounting for defective cells in a memory device	Cross, Randolph A.	11/6/1995
SG041004	SG	Circuits, systems, and methods for accounting for defective cells in a memory device	Cross, Randolph A.	11/6/1995
EP0792507	EP	Circuits, systems, and methods for accounting for defective cells in a memory device	Cross, Randolph A.	11/6/1995
DE69518163.7	DE	Circuits, systems, and methods for accounting for defective cells in a memory device	Cross, Randolph A.	11/6/1995
FR0792507	FR	Circuits, systems, and methods for accounting for defective cells in a memory device	Cross, Randolph A.	11/6/1995
GB0792507	GB	Circuits, systems, and methods for accounting for defective cells in a memory device	Cross, Randolph A.	11/6/1995
IE0792507	IE	Circuits, systems, and methods for accounting for defective cells in a memory device	Cross, Randolph A.	11/6/1995
NL95939746.4	NL	Circuits, systems, and methods for accounting for defective cells in a memory device	Cross, Randolph A.	11/6/1995
5,455,526	US	Digital voltage shifters and systems using the same	Runas, Michael E.	8/10/1994
DE69505752.9	DE	Digital voltage shifters and systems using the same	Runas, Michael E.	8/8/1995
EP0696850	EP	Digital voltage shifters and systems using the same	Runas, Michael E.	8/8/1995
EP0788235	EP	Digital voltage shifters and systems using the same	Runas, Michael E.	8/8/1995
FR0696850	FR	Digital voltage shifters and systems using the same	Runas, Michael E.	8/8/1995
GB0696850	GB	Digital voltage shifters and systems using the same	Runas, Michael E.	8/8/1995
JP07-203390	JP	Digital voltage shifters and systems using the same	Runas, Michael E.	8/9/1995
KR10-0247604	KR	Digital voltage shifters and systems using the same	Runas, Michael E.	8/9/1995
FR0788235	FR	Digital voltage shifters and systems using the same	Runas, Michael E.	8/8/1995
GB0788235	GB	Digital voltage shifters and systems using the same	Runas, Michael E.	8/8/1995
DE69519386.4	DE	Digital voltage shifters and systems using the same	Runas, Michael E.	8/8/1995

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08/519,992	US	Circuits and methods for controlling frame buffer refresh	Sharma, Sudhir K.	8/28/1995
EP96930661.2	EP	Circuits and methods for controlling frame buffer refresh	Sharma, Sudhir K.	8/28/1996
JP09-510625	JP	Circuits and methods for controlling frame buffer refresh	Sharma, Sudhir K.	8/28/1996
KR10-1998-0701432	KR	Circuits and methods for controlling frame buffer refresh	Sharma, Sudhir K.	8/28/1996
PCT/US1996/014062	WO	Circuits and methods for controlling frame buffer refresh	Sharma, Sudhir K.	8/28/1996
08/512,574	US	Unified system/frame buffer memories and systems and methods using the same	Rao, G.R.	8/8/1995
EP96931370.9	EP	Unified system/frame buffer memories and systems and methods using the same	Rao, G.R.	8/5/1996
HK98109048.6	HK	Unified system/frame buffer memories and systems and methods using the same	Rao, G.R.	8/5/1996
JP09-508627	JP	Unified system/frame buffer memories and systems and methods using the same	Rao, G.R.	8/5/1996
KR10-1998-0700938	KR	Unified system/frame buffer memories and systems and methods using the same	Rao, G.R.	2/7/1998
PCT/US1996/012829	WO	Unified system/frame buffer memories and systems and methods using the same	Rao, G.R.	8/5/1996
08/611,061	US	A Memory with optimized memory space and wide data input/output and systems and methods using the same	Rao, G.R.; Runas, Michael E.; Taylor, Ronald T.	3/5/1996
EP97301403.8	EP	A Memory with optimized memory space and wide data input/output and systems and methods using the same	Rao, G.R.; Runas, Michael E.; Taylor, Ronald T.	3/4/1997
HK98101985.8	HK	A Memory with optimized memory space and wide data input/output and systems and methods using the same	Rao, G.R.; Runas, Michael E.; Taylor, Ronald T.	3/4/1997
JP09-036524	JP	A Memory with optimized memory space and wide data input/output and systems and methods using the same	Rao, G.R.; Runas, Michael E.; Taylor, Ronald T.	2/20/1997
KR10-0490703	KR	A Memory with optimized memory space and wide data input/output and systems and methods using the same	Rao, G.R.; Runas, Michael E.; Taylor, Ronald T.	3/5/1997

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TW117176	TW	A Memory with optimized memory space and wide data input/output and systems and methods using the same	Rao, G.R.; Runas, Michael E.; Taylor, Ronald T.	2/27/1997
6,425,020	US	Systems and methods for passively transferring data across a selected single bus line independent of a control circuitry	Sharma, Sudhir K.	4/18/1997