PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Micron Technology Inc.	08/18/2010

RECEIVING PARTY DATA

Name:	MOSAID Technologies Incorporated
Street Address:	11 Hines Road, Suite 203
City:	Ottawa
State/Country:	CANADA
Postal Code:	K2K 2X1

PROPERTY NUMBERS Total: 2

Property Type	Number
Patent Number:	5257238
Patent Number:	5600602

CH $80.00 5257238

CORRESPONDENCE DATA

Fax Number: (613)591-8148
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ATTORNEY DOCKET NUMBER:	MICRON
NAME OF SUBMITTER:	Victoria Donnelly

Total Attachments: 11
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CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS

Definitions

"Assignor" is Micron Technology, Inc., a Delaware corporation with offices at 8000 South Federal Way, Boise, ID, USA.

"Assignee" is MOSAID Technologies Incorporated, a Canadian company, with an office located at 11 Hines Road, Suite 203, Ottawa, Ontario, Canada K2K 2X1.

"The Letters Patents" are the patents and patent applications identified in Schedules A and B, including, without limitation, all parents, divisionals, continuations, continuations-in-part, reissues, and reexaminations thereof and all pending applications therefore, and all foreign counterparts thereof and all pending applications therefor, and any patents resulting therefrom.

Covenants

Assignor, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, confirms having sold, assigned, and transferred to Assignee its entire right, title and interest in and to The Letters Patents on April 2, 2009.

Assignor confirms having sold, assigned, and transferred to Assignee all claims for damages and all remedies arising out of any violation of the rights that have been assigned and that may have accrued prior to the date of this Confirmatory Assignment, or may accrue hereafter, including, but not limited to, the right to bring suit and to collect and retain damages for past infringement of The Letters Patents.

Assignor hereby authorizes and requests the Commissioner of Patents of the United States, and any other official of the United States and any country foreign to the United States whose duty it is to issue or record patents, to issue The Letters Patents to Assignee and to record assignment of The Letters Patents to Assignee.

This Confirmatory Assignment shall be binding on the heirs, assigns, representatives, and successors of Assignor and shall extend to and inure to the benefit of the successors and assigns of the Assignee.

Agreed to by:

Assignor: Micron Technology, Inc.

Signed: Roderic W. Lewis

Name: Roderic W. Lewis

Position: VP Legal Affairs

Date: Aug 18, 2010

Notarization

State of Idaho

County of Ada

On August 18, 2010 before me, Jan Reimer, personally appeared the above-named, Roderic W. Lewis who executed this Assignment in my presence and acknowledged to me that he did so of his own free will and in his authorized capacity for the purposes set forth herein.

JAN REIMER NOTARY PUBLIC STATE OF IDAHO

Signed: Jan Reimer

My commission expires: 9/11/2013

Accepted by:

Assignee: MOSAID Technologies Incorporated

Signed: _____ September 22, 2010

Name: Phillip Shaer

Position: Vice President, General Counsel and Corporate Secretary

Witness: _____

Schedule A

Patents and Applications listed in Assignment of Patent Rights executed April 2, 2009

Patents

Country	Patent Number	Title
US	5831334	FIELD EFFECT TRANSISTOR COMPRISING ELECTRICALLY CONDUCTIVE PLUGS HAVING MONOCRYSTALLINE AND POLYCRYSTALLINE SILICON
US	5637518	METHOD OF MAKING A FIELD EFFECT TRANSISTOR HAVING AN ELEVATED SOURCE AND AN ELEVATED DRAIN
US	5677573	FIELD EFFECT TRANSISTOR
US	5998844	SEMICONDUCTOR CONSTRUCTIONS COMPRISING ELECTRICALLY CONDUCTIVE PLUGS HAVING MONOCRYSTALLINE AND POLYCRYSTALLINE SILICON
US	6057200	METHOD OF MAKING A FIELD EFFECT TRANSISTOR HAVING AN ELEVATED SOURCE AND AN ELEVATED DRAIN
US	5574697	MEMORY DEVICE WITH DISTRIBUTED VOLTAGE REGULATION SYSTEM
US	5818780	MEMORY DEVICE WITH DISTRIBUTED VOLTAGE REGULATION SYSTEM
US	6009034	MEMORY DEVICE WITH DISTRIBUTED VOLTAGE REGULATION SYSTEM
US	6307802	MEMORY DEVICE WITH DISTRIBUTED VOLTAGE REGULATION SYSTEM
US	5673224	SEGMENTED NON-VOLATILE MEMORY ARRAY WITH MULTIPLE SOURCES WITH IMPROVED WORD LINE CONTROL CIRCUITRY
US	5959884	SEGMENTED NON-VOLATILE MEMORY ARRAY WITH MULTIPLE SOURCES WITH IMPROVED WORD LINE CONTROL CIRCUITRY
US	5873112	SYSTEM AND METHOD FOR ENCODING DATA TO REDUCE POWER AND TIME REQUIRED TO WRITE THE ENCODED DATA TO A FLASH MEMORY

Country	Patent Number	Title
US	6292868	SYSTEM AND METHOD FOR ENCODING DATA TO REDUCE POWER AND TIME REQUIRED TO WRITE THE ENCODED DATA TO A FLASH MEMORY
US	6222770	METHOD FOR AN ERASE OPERATION OF FLASH MEMORY USING A SOURCE REGULATION CIRCUIT
US	6529417	SOURCE REGULATION CIRCUIT FOR FLASH MEMORY
US	6097632	SOURCE REGULATION CIRCUIT FOR AN ERASE OPERATION OF FLASH MEMORY
US	6256259	DELAY LOCKED LOOP WITH BINARY COUPLED CAPACITOR
US	6483757	DELAY LOCKED LOOP WITH BINARY COUPLED CAPACITOR
US	6490224	DELAY LOCKED LOOP WITH BINARY COUPLED CAPACITOR
US	6490207	DELAY LOCKED LOOP WITH BINARY COUPLED CAPACITOR
US	6400641	DELAY LOCKED LOOP WITH BINARY COUPLED CAPACITOR
US	6262921	DELAY LOCKED LOOP WITH BINARY COUPLED CAPACITOR
Japan	3778946	DELAY LOCKED LOOP WITH BINARY COUPLED CAPACITOR
US	5946244	DELAY LOCKED LOOP WITH BINARY COUPLED CAPACITOR
South Korea	662221	DELAY LOCKED LOOP WITH BINARY COUPLED CAPACITOR
US	6199177	DEVICE AND METHOD FOR REPAIRING A SEMICONDUCTOR MEMORY
US	6910152	DEVICE AND METHOD FOR REPAIRING A SEMICONDUCTOR MEMORY
US	6571352	DEVICE FOR REPAIRING A SEMICONDUCTOR MEMORY
US	6892318	METHOD FOR REPAIRING A SEMICONDUCTOR MEMORY
US	7467334	METHOD FOR REPAIRING A SEMICONDUCTOR MEMORY
US	7045834	MEMORY CELL ARRAYS
US	6410948	MEMORY CELL ARRAYS COMPRISING INTERSECTING SLANTED PORTIONS
US	6607944	METHOD OF MAKING MEMORY CELL ARRAYS
US	6790721	METAL LOCAL INTERCONNECT SELF-ALIGNED SOURCE FLASH CELL
China	ZL 01813103.4	SEMICONDUCTOR MEMORY HAVING SEGMENTED ROW REPAIR

Country	Patent Number	Title
South Korea	10-0595813	SEMICONDUCTOR MEMORY HAVING SEGMENTED ROW REPAIR
US	6314030	SEMICONDUCTOR MEMORY HAVING SEGMENTED ROW REPAIR
US	6442084	SEMICONDUCTOR MEMORY HAVING SEGMENTED ROW REPAIR
US	6724663	ERASABLE BLOCK ARCHITECTURE FOR NON-VOLATLE MEMORY
US	6587383	ERASE BLOCK ARCHITECTURE FOR NON-VOLATILE MEMORY
US	6895474	SYNCHRONOUS DRAM WITH SELECTABLE INTERNAL PREFETCH SIZE
US	6981100	SYNCHRONOUS DRAM WITH SELECTABLE INTERNAL PREFETCH SIZE
US	7120754	SYNCHRONOUS DRAM WITH SELECTABLE INTERNAL PREFETCH SIZE
US	7154781	CONTIGUOUS BLOCK ADDRESSING SCHEME
US	7154780	CONTIGUOUS BLOCK ADDRESSING SCHEME
US	7123512	CONTIGUOUS BLOCK ADDRESSING SCHEME
US	7154782	CONTIGUOUS BLOCK ADDRESSING SCHEME
US	7089438	CIRCUIT, SYSTEM AND METHOD FOR SELECTIVELY TURNING OFF INTERNAL CLOCK DRIVERS
US	7061817	DATA PATH HAVING GROUNDED PRECHARGE OPERATION AND TEST COMPRESSION CAPABILITY
US	7170806	DATA PATH HAVING GROUNDED PRECHARGE OPERATION AND TEST COMPRESSION CAPABILITY
US	7038945	FLASH MEMORY DEVICE WITH IMPROVED PROGRAMMING PERFORMANCE
US	7120055	FLASH MEMORY DEVICE WITH IMPROVED PROGRAMMING PERFORMANCE
US	7280403	FLASH MEMORY DEVICE WITH IMPROVED PROGRAMMING PERFORMANCE
US	5913128	METHOD FOR FORMING TEXTURIZED POLYSILICON
US	5838620	CIRCUIT FOR CANCELLING AND REPLACING REDUNDANT ELEMENTS
US	5677884	CIRCUIT FOR CANCELLING AND REPLACING REDUNDANT ELEMENTS

Country	Patent Number	Title
US	5912579	CIRCUIT FOR CANCELLING AND REPLACING REDUNDANT ELEMENTS
US	6208568	A CIRCUIT FOR CANCELLING AND REPLACING REDUNDANT ELEMENTS
US	5978287	INPUT/OUTPUT DEVICE HAVING SHARED ACTIVE AREA
US	6291289	METHOD OF FORMING DRAM TRENCH CAPACITOR WITH METAL LAYER OVER HEMISPHERICAL GRAIN POLYSILICON
US	6388284	CAPACITOR STRUCTURES
US	6167541	METHOD FOR DETECTING OR PREPARING INTERCELL DEFECTS IN MORE THAN ONE ARRAY OF A MEMORY DEVICE
US	6510533	METHOD FOR DETECTING OR REPAIRING INTERCELL DEFECTS IN MORE THAN ONE ARRAY OF A MEMORY DEVICE
US	6077211	CIRCUITS AND METHODS FOR SELECTIVELY COUPLING REDUNDANT ELEMENTS INTO AN INTEGRATED CIRCUIT
US	6333887	CIRCUITS AND METHODS FOR SELECTIVELY COUPLING REDUNDANT ELEMENTS INTO AN INTEGRATED CIRCUIT
US	6141276	APPARATUS AND METHOD FOR INCREASING TEST FLEXIBIITY OF A MEMORY DEVICE
US	6459635	APPARATUS AND METHOD FOR INCREASING TEST FLEXIBIITY OF A MEMORY DEVICE
US	5257238	DYNAMIC MEMORY HAVING ACCESS TRANSISTOR TURN-OFF STATE
US	5734620	HIERARCHICAL MEMORY ARRAY STRUCTURE WITH REDUNDANT COMPONENTS HAVING ELECTRICALLY ISOLATED BIT LINES
US	5600602	HIERARCHICAL MEMORY ARRAY STRUCTURE HAVING ELECTRICALLY ISOLATED BIT LINES FOR TEMPORARY DATA STORAGE
US	5724301	HIERARCHICAL MEMORY ARRAY STRUCTURE HAVING ELECTRICALLY ISOLATED BIT LINES FOR TEMPORARY DATA STORAGE
Germany	696 06 771.4 (0846325)	REDUCED AREA SENSE AMPLIFIER ISOLATION LAYOUT IN A DYNAMIC RAM ARCHITECTURE

Country	Patent Number	Title
EP	0846325	REDUCED AREA SENSE AMPLIFIER ISOLATION LAYOUT IN A DYNAMIC RAM ARCHITECTURE
France	0846325	REDUCED AREA SENSE AMPLIFIER ISOLATION LAYOUT IN A DYNAMIC RAM ARCHITECTURE
Great Britain	0846325	REDUCED AREA SENSE AMPLIFIER ISOLATION LAYOUT IN A DYNAMIC RAM ARCHITECTURE
Italy	0846325	REDUCED AREA SENSE AMPLIFIER ISOLATION LAYOUT IN A DYNAMIC RAM ARCHITECTURE
South Korea	397684	REDUCED AREA SENSE AMPLIFIER ISOLATION LAYOUT IN A DYNAMIC RAM ARCHITECTURE
Taiwan	NI 094557	REDUCED AREA SENSE AMPLIFIER ISOLATION LAYOUT IN A DYNAMIC RAM ARCHITECTURE
US	6480407	REDUCED AREA SENSE AMPLIFIER ISOLATION LAYOUT IN A DYNAMIC RAM ARCHITECTURE
US	6577523	REDUCED AREA SENSE AMPLIFIER ISOLATION LAYOUT IN A DYNAMIC RAM ARCHITECTURE
US	6600671	REDUCED AREA SENSE AMPLIFIER ISOLATION LAYOUT IN A DYNAMIC RAM ARCHITECTURE
US	5976917	INTEGRATED CIRCUITRY FUSE FORMING METHODS, INTEGRATED CIRCUITRY PROGRAMMING METHODS, AND RELATED INTEGRATED CIRCUITRY
US	6238955	INTERGRATED CIRCUITRY FUSE FORMING METHODS, INTERGRATED CIRCUITRY PROGRAMMING METHODS, AND RELATED INTERGRATED CIRCUITRY
US	6249037	INTEGRATED CIRCUITRY FUSE FORMING METHODS, INTEGRATED CIRCUITRY PROGRAMMING METHODS, AND RELATED INTEGRATED CIRCUITRY
US	6300170	INTEGRATED CIRCUITRY FUSE FORMING METHODS, INTEGRATED CIRCUITRY PROGRAMMING METHODS, AND RELATED INTEGRATED CIRCUITRY
US	6265299	INTEGRATED CIRCUITRY FUSE FORMING METHODS, INTEGRATED CIRCUITRY PROGRAMMING METHODS, AND RELATED INTEGRATED CIRCUITRY

Country	Patent Number	Title
US	6680519	INTEGRATED CIRCUITRY FUSE FORMING METHODS, INTEGRATED CIRCUITRY PROGRAMMING METHODS, AND RELATED INTEGRATED CIRCUITRY

Patent Applications

Country	Patent Appln Number	Title
US	11/581,887	NON-VOLATILE MEMORY DEVICES AND CONTROL AND OPERATION THEREOF
US	11/449,499	CIRCUIT, SYSTEM AND METHOD FOR SELECTIVELY TURNING OFF INTERNAL CLOCK DRIVERS
US	12/336,371	MEMORY DEVICE AND METHOD FOR REPAIRING A SEMICONDUCTOR MEMORY
EP	01942036.3	SEMICONDUCTOR MEMORY HAVING SEGMENTED ROW REPAIR
EP	09001943.1	SEMICONDUCTOR MEMORY HAVING SEGMENTED ROW REPAIR
Japan	2002-511339	SEMICONDUCTOR MEMORY HAVING SEGMENTED ROW REPAIR

Schedule B

Patents and Applications not listed in the Assignment of Patent Rights executed April 2, 2009

Patents

Country	Patent Number	Title
KR	292640	MEMORY CIRCUIT WITH HIERARCHICAL BIT LINE STRUCTURE
TW	119516	MEMORY CIRCUIT WITH HIERARCHICAL BIT LINE STRUCTURE

Patent Applications

Country	Patent Appln Number	Title
CN	200810176690.00	SEMICONDUCTOR MEMORY HAVING SEGMENTED ROW REPAIR
WO	PCT/US95/16071	MEMORY CIRCUIT WITH HIERARCHICAL BIT LINE STRUCTURE

Abandoned Patent Applications

Country	Patent Appln Number	Title
US	11/484,856	SYNCHRONOUS DRAM WITH SELECTABLE INTERNAL PREFETCH SIZE
US	11/434,303	MEMORY CELL ARRAYS
US	08/506,674	METHOD FOR FORMING TEXTURIZED POLYSILICON
US	08/417,007	CIRCUIT FOR CANCELLING AND REPLACING REDUNDANT ELEMENTS
US	08/417,208	HIERARCHICAL MEMORY ARRAY STRUCTURE WITH REDUNDANT COMPONENTS HAVING ELECTRICALLY ISOLATED BIT LINES

JP	1997-510470	REDUCED AREA SENSE AMPLIFIER ISOLATION LAYOUT IN A DYNAMIC RAM ARCHITECTURE
JP	08-530268	MEMORY CIRCUIT WITH HIERARCHICAL BIT LINE STRUCTURE