Electronic Version v1.1 Stylesheet Version v1.1

SUBMISSION TYPE:	CORRECTIVE ASSIGNMENT
NATURE OF CONVEYANCE:	Corrective Assignment to correct the Conveying Party and the Receiving Party previously recorded on Reel 009756 Frame 0085. Assignor(s) hereby confirms the Conveying Party is Ramtron International Corporation; and the Receiving Party is National Electrical Benefit Fund

CONVEYING PARTY DATA

Name	Execution Date
Ramtron International Corporation	01/15/1999

RECEIVING PARTY DATA

Name:	National Electrical Benefit Fund
Street Address:	1125 Fifteenth Street N.W.
City:	Washington
State/Country:	DISTRICT OF COLUMBIA
Postal Code:	20005

PROPERTY NUMBERS Total: 1

Property Type	Number
Patent Number:	5963481

CORRESPONDENCE DATA

Fax Number: (312)913-0002

Correspondence will be sent via US Mail when the fax attempt is unsuccessful.

Phone: 3129130001

Email: docketing@mbhb.com

Correspondent Name: McDonnell Boehnen Hulbert & Berghoff LLP

Address Line 1: 300 South Wacker Drive

Address Line 2: Suite 3200

Address Line 4: Chicago, ILLINOIS 60606

ATTORNEY DOCKET NUMBER: 07-397

NAME OF SUBMITTER: Thomas J. Loos

Total Attachments: 26

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PATENT REEL: 025446 FRAME: 0001

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> PATENT REEL: 025446 FRAME: 0002

(Hev. 5-93)	ORDATION FOR	02-26-1999	*RTMENT OF COMMERCE alent and Trademark Office
Омв № 0651-0011 (ехр. 4/94) Tab settings ▷ □ ▷ ▼	PATENTS		▼ ▼
To the Honorable Commissioner of Pate	nts and Trademarks: Pk	100975917	or copy thereof.
4. Name of conveying party/ies):	FEB 23 AH 101 57	2. Name and address of receiving p	arty(ies)
National Electrical Benefit	rund PMMAIIOE	Name: Ramtron Internation	nal Corporation
MRD 2-23 Additional name(s) of conveying party(ies) attached?	3-99	Internal Address:	
Nature of conveyance:			
☐ Assignment ☐) Merger	Street Address: 1850 Ramtrol	n Drive
☐ Security Agreement ☐	Change of Name		
5 Other First Amendment to Pa	tent Sec. Agmmt.	City: Colorado Spring State:	CO ZIP: <u>_80921</u> _
Execution Date: January 15, 1999		Additional name(s) & address(es) attache	ed? D. Yes 25 No
4. Application number(s) or patent number	r(s):		
if this document is being filed together to	with a new application, th	e execution date of the application i	s:
A. Patent Application No.(s)	1	B. Patent No.(s)	
SEE	ATTACHED	SCHEDULE A SUPPLEMENT	
	Additional numbers attache	ed? XXX Yes DINo	
Name and address of party to whom concerning document should be mailed:		6. Total number of applications and p	patents involved: 83
Name: Anthony F. Lo Cicero, E	aq	7. Total fee (37 CFR 3.41)\$	3,320.00
Internal Address:		☑ Enclosed	
AMSTER, ROTHSTEIN & EBENSTEI	<u> </u>	Authorized to be charged to d	eposit account
Street Address: 90 Park Avenue	{	3. Deposit account number:	
		01-1785	
City: New York State: NY	ZIP: <u>10016</u>	(Attach duplicate copy of this page if pay	ing by deposit eccount)
02/26/1999 DEDMTES 00000029 543A605	DO NOT USE TH	IIS SPACE	
9. Statement and signature.	1		
To the best of my knowledge and belief, the original document.	the foregoing internation	n is true and correct and any attach	ed copy is a true copy of
_Anthony F. Lo Cicero	100	,	02-22-99
Name of Person Signing		Tature	Date
. Total nu	imper of pages including cover	r sheet, attachments, and document:	<u>===</u>

SCHEDULE A SUPPLEMENT

PATENTS

RAM No.	Tech Type	fitte	P aten t No.	Issued !	Expires	inventor
RAM 398	FRAM	IRIOIUM OXIDE LOCAL INTERCONNECT	5.838.605	t1/17/98	3/20/16	BAILEY, RICHARD A.
RAM 393	EDRAM	EORAM WITH INTEGRATED GENERATION AND CONTROL OF WRITE ENABLE AND COLUMN LATCH SIGNALS AND METHOD OF MAKING SAME	5 535,442	11/10/98	3/ 22/16	JOSEPH, JAMES OEAN, ET
RAM 371 DIV	FRAM	A VOLTAGE REFERENCE FOR A FERROELECTRIC 1T/1C BASED MEMORY	5.822.237	10/13/98	9/1 5/14	WILSON, OENNIS R. ET AL
RAM 409	ORAM	SEMICOHOUCTOR MEMORY DEVICE	5.616.771	10/6/98	9/30/16	YASU, YOSHIKO, ET AL
RAM 384 DIV	FRAM	CIRCUIT AND METHOD FOR REDUCING COMPENSATION OF A FERROELECTRIC CAPACITOR BY MULTIPLE PULSING OF THE PLATE LINE FOLLOWING A WRITE OPERATION	5 815.430	9/ 29/9 8	41 0/1 5	VERHAEGHE, OONALD J
RAM 412	FRAM	LOW-POWER NON-RESETABLE TEST MODE	5,804,996	9/ 8/98	יועבויב	7 VERHAEGHE. OONALD J.,
RAM 410	FRAM ORAM	SYSTEM AND METHOD PROVIDING SELECTIVE WRITE PROTECTION FOR INDIVIDUAL BLOCKS OF MEMORY IN A NON-VOLATILE MEMORY		9/1/98	10/30/1	6 YE AGER, ET AL
RAM 390	EORA	OSVICE TO MEMORY SYSTEM	5,802.550	9/1/98	8/30/1	5 JOSEPH, JAMES D., ET A
RAM 396 OIV	FRAM		5. 500.683	9/1/98	3/1 5/ 1	16 Ka mmerdi ner, Lee, et
RAM 385	FRAM		5.789.323	6/4/98		15 TAYLOR, THOMAS C.
RAM 388	FRAN	BOOTSTRAPPING CIRCUIT UTILIZING A FERROELECTRIC CAPACITOR	5,774,392	6/30/98	3/ 25/	16 KRAUS. WILLIAM F. ET A
R AM 403	FRAN	A SYSTEM AND METHOD FOR MITIGATING IMPRINT EFFECT ::: FERROELECTRIC RANGO ACCESS MEMORIES UTILIZING A COMPLEMENTARY DATA PATH	5,745,403 M	4/28/98	2/28	M7 TAYLOR, CRAIG
RAM 343 CC	N EOR	AM ENHANCED DRAM WITH EMBEODED REGISTI	ERS 5.721.862	2/24/98	2/24	15 SARTORE, RONALD H.,
RAM 343 CIP	EDR	AM ENHANCED DRAMWITH EMBEDOEO REGISTI	ERS 5,699,317	12/16/97	1/22	V12 SARTORE, RONALO H.,
RAM 404		SAME STATE AND OPPOSITE STATE OIAGNOSTIC TEST FOR FERROELECTRIC MEMORIES	5.66 1.730	6/26/97	9/27	7/16 MITRA, SANJAY, ET AL
RAM 321	ORA	M PROCESS FOR FABRICATING TRANSISTORS USING COMPOSITE NITRIOE STRUCTURE	5.610.099	3/11/9	7 6,721	M14 LARSON, WILLIAM L
RAM 368 FV	VC FRA	M INTEGRATION OF HIGH VALUE CAPACITOR	5,608,246	3/4/9	7 3/	4/14 YEAGER, MICHAEL W.,
RAM 387	FRA		5.598.366	1/28/9		6/15 KRAUS, WILLIAM F., E?
RAM 384	FR	AM CIRCUIT AND METHOD FOR REDUCING COMPENSATION OF A FERROELECTRIC CAPACITOR BY MULTIPLE PULSING OF THE PLATE LINE FOLLOWING A WRITE OPERATION.		175	,	0/15 VERHAEGHE. OONALE
RAM 332 C	IV FR	AM STACKEO FERROELECTRIC MEMORY CELL METHOO	ANO 5.580.814	12/3/		29/11 LARSON, WILLIAM L.
RAM 379 D	DIV FR	AM PASSIVATION METHOD AND STRUCTURE USING HARD CERAMIC MATERIALS OR THE	5, 578.867 LIKE	11/26/	96 3/	11/14 ARGOS, GEORGE, ET
						12/2/08

12/2/95

PAAFUNT REEL: 9254467444511698604

RAM No.	Yech Typa		Patent No.	(ssued	Expires	Inventor WILSON, DENNIS R., ET AL
RAM 371	FRAM	VOLTAGE REFERENCE FOR A FERROELECTRIC	5.572,459	1112120		
RAM 381		1TMC BASED MEMORY CIRCUIT WITH A SINGLE ADDRESS REGISTER THAT AUGMENTS A MEMORY CONTROLLER BY ENABLING CACHE READS AND PAGE-MODE	5 5 66,318	10/15/96	3/2/14	O EBMAL H932OL
RAM 382	FRAM	WRITES FERROFI FOTRIC MEMORY SENSING METHOD	5 532,9 53	7/2/95	3/29/15	RUESCH, RODNEY A., ET A
RAM 370	FRAM	USING DISTINCT READ AND WRITE VOLTAGES FERROELECTRIC MEMORY SENSING SCHEME USING BIT LINES PRECHARGED TO A LOGIC	5,530,668	6/25/96	±12/15	CheRN, WEN-FOO, ET AL.
RAM 374	FRAM	ONE VOLTAGE FERROELECTRIC CAPACITOR REMEWAL	5,525,528	6/11/96	5/ 5/1 /	4 PERINO, STANLEY, ET AL.
PAM 352 FWC	FRAM	METHOD SEMICONDUCTOR DEVICE HAVING A	5,523,595	67 4/96	4:411	3 TAKENAKA, KAZUHIRO, E
RAM 377 CON	FRAM		5.519.566	5/21/96		4 PERINO, STANLEY C ET
RAM 378	FRAN	LAYERED OXIDES LAYERED LOCAL INTERCONNECT COMPATIBLE WITH INTEGRATED CIRCUIT FERROELECTRIC	E 5.496.569	3/12/96	6/22/	14 EASTEP, BRIAN
RAM 332 FW	CZ FRAM	CAPACITORS A STACKED FERROELECTRIC MEMORY CELL AN		2/27/99	-	13 LARSON, WILLIAM L
RAM 376	FRAI	METHOD MOISE AND GLITCH SUPPRESSING FILTER	5,479,132	12/25/9	5 6/6	114 VERHAEGHE, DONALO. (
RAM 358 FW	CZ FRA	WITH FEEDBACK	5,475,248	12/12/9	5 12/12	VIZ TAN ENAKA , K.

PAATUNT REEL: 8259458748471698705

PATENT APPLICATIONS

Ramtron No.	Patent Application	Serial No.	Filing Oate Assignee	Tech	Inventor
RAM 343 DIV	ENHANCEO ORAM WITH EMBEDDED REGISTERS	06/888 371	7/3/97 EMS	EORAM	SARTORE, RONALD H , ET AL
RAM 343 DIV/CD	ENHANCED DRAM WITH EMBEDDED REGISTERS	09/182 994	IO/30/96 EMS	EDRAM	SARTORE RONALOH,
RAM 368 DIV	INTEGRATION OF HIGH VALUE CAPACITOR 08/544,470	08/544,470	10/18/95 R I C	FRAM	YEAGER MICHAELW, ET AL
RA::389	COMPUTER HYBRID MEMORY INCLUDING DRAM AND EDRAM MEMORY COMPONENTS, WITH SECONDARY CACHE IN EDRAM FOR DRAM	08/615 392	SM3 96 FMS	EORAM	JOSEPH JAMES DEAN
RAM 391	PROGRAMMABLE OUTPUT DEVICES FOR CONTROLLING SIGNAL LEVELS IN AN RF/ID TRANSPONDER	08/521 251	6/30/95 R 1C	RFIO	DOWNS JEFFREYE, ET
RAM 392 DIV	METHOD OF MANUFACTURING IRIDIUM ELECTRODE FOR STRONTIUM BISMUTH TANTALATE FERROELECTRIC CAPACITORS	08/896, 329	7/17/97 RIC	FRAM	PERINO. STANLEY, ET AL

PAAFUNT REEL: 925448AWWW1299906

TAYLOR, CRAIG	FRAM	2/28/97 R I C	08/810,607	SERIAL FRAM ARCHITECTURE TO EQUALIZE COLUMN ACCESS	RAM 402
VERHAEGHE DONALD J. ET AL	FRAM	6/7/96 R I C	08/663.032	LOW VOLTAGE BOOTSTRAPPING CIRCUIT	RAM 400
ARGOS, GEORGE JR. ET AL	FRAM	10/8/96 R I C	08/728.256	YIELD ENHANCEMENT TECHNIQUE FOR INTEGRATED CIRCUIT PROCESSING TO REDUCE EFFECTS OF UNDESIRED DIELECTRIC MOISTURE RETENTION AND SUBSEQUENT HYDROGEN OUT DIFFUSION	RAM 399
BAILEY, RICHARD A	FRAM	10/29/98 R I C	09/183.545	IRIDIUM OXIDE LOCAL INTERCONNECT	RAM 398 DIV
TRAYNOR STEVEN	FRAM	3/15/96 R I C	08/616.913	A METHOD OF MEASURING RETENTION PERFORMANCE AND IMPRINT DEGRADATION OF FERROELECTRIC FILMS	RAM 397
KAMMERDINER LEE ET AL	FRAM	3/15/96 R I C	08/6 6. 856	THE USE OF CALCIUM AND STRONTIUM DOPANTS TO IMPROVE RETENTION PERFORMANCE IN A PZT FERROELECTRIC FILM	RAM 396
HEISLER DOYLE JAMES ET AL	EDRAM	4/10/96 EMS	08/630 489	DYNAMIC CACHE SIZING MEMORY	RAM 394
Inventor	Type	Filing Assignee	Serial No.	Patent Application	Ramiron No.

EASTEP, BRIAN, ET AL	EAST	FRAM	5/27/98 R1C	09/065,280	COMPLETELY ENCAPSULATED TOP ELECTRODE OF A FERROELECTRIC CAPACITOR USING A LEAO-ENHANCEO FACAPSULATION LAYER	RAM 407 CIP3
EVANS, THOMAS A, ET	AL EVAN	FRAM	3/27/97 R I C	08/828,1 57	PARTIALLY OR COMPLETELY ENCAPSULATEO TOP ELECTRODE OF FERROELECTRIC CAPACITOR	RAM 407 CIP2
EVANS THOMAS A. ET	AL EVAN	FRAM	10/11/96 R I C	08/728 740	PARTIALLY OR COMPLETELY ENCAPSULATEO TOP ELECTRODE OF A FERROELECTRIC CAPACITOR	RAM 407 CIP
EVANS, THOMAS A. ET AL	AL AL	FRAM	8/20/96 R I C	08/700.076	PARTIALLY OR COMPLETELY ENCAPSULATED TOP ELECTRODE OF A FERROELECTRIC CAPACITOR	RAM 407
DOWNS HIFERYE	DOWI	FRAM	10/21/96 RTC	08/734 802	DATA PROCESSOR INCORPORATING A FERROELECTRIC MEMORY ARRAY SELECTABLY CONFIGURABLE AS READAWRITE AND READ ONLY MEMORY	RAM 406
- KRAUSE WILLIAM F	KRAU	FRAM	2/3/98 RIC	09/017 577	BANOGAP REFERENCED BASED POWER ON OETECT CIRCUIT	RAM 405 CON
ARAGO VAREDON	2	FRAM	8/2\)96 R I C	08/702 363	BANDGAP REFERENCE BASED POWER-ON DETECT CIRCUIT NCLUDING A SUPPRESSION CIRCUIT	RAM 405
PLOVIETIANTE	Inventor	Type	Pale Assignee	Serial No.	Palent Application	Ramiron No.

MOBLEY, KENNETH J. ET AL.	EDRAM	2998 EMS	09/023,656	SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY DEVICE INCORPORATING A STATIC RAM CACHE	RAM 420
TAYLOR, CRAIG	EDRAM	41/97 EMS	05/840,115	FIRST-IN, FIRST-OUT INTEGRATED CIRCUIT MEMORY DEVICE UTILIZING A DYNAMIC RANDOM ACCESS MEMORY ARRAY FOR DATA STORAGE IMPLEMENTED IN CONJUNCTION WITH AN ASSOCIATED STATIC RANDOM ACCESS MEMORY CACHE	RAM 418
ALWAIS, MICHAEL, ET AL	EDRAM	5/2/97 EMS	08/650,802	ENHANCED SIGNAL PROCESSING RANDOM ACCESS MEMORY DEVICE UTILIZING A DRAM MEMORY ARRAY INTEGRATED WITH AN ASSOCIATED SRAM CACHE AND INTERNAL REFRESH CONTROL	RAM 417
ARGOS, GEORGE, ET AL	FRAM	5/9/97 R I C Fupisu	08/853.527	DUAL-LEVEL METALIZATION METHOD FOR INTEGRATED CIRCUIT FERROELECTRIC DEVICES	RAM 415
WILSON D. ET AL	FRAM	11/14/97 R1 C	08/970,453	SENSING METHODOLOGY FOR A 1TH C FERROELECTRIC MEMORY	RAM 414
J. ET AL	FRAM	2/19/97 R I C Haach	08/602.630	SYSTEM AND METHOD FOR CONTROLLING INTERNAL TEST MODES IN A NON-VOLATILE MEMORY THROUGH NORMAL ACCESSES	RAM 413
Inventor	Type	Filing Date Assignee	Serial No.	Patent Application	Ramtron No.

	RAM 427 SENSE AMPLIFIER UTRIZING A BALANCING RESISTOR	RAM 425 PLASTIC PACKAGE ASSEMBLY METHOD FOR A FERROELECTRIC BASED INTEGRATED CIRCUIT	RAM 424 VOLTAGE BOOST CIRCUIT AND OPERATION THEREOF AT LOW POWER SUPPLY VOLTAGES	RAM 422 INTEGRATED CIRCUIT MEMORY OF VICE INCORPORATING A NON-VOLATILE MEMORY ARRAY AND A RELATIVELY FASTER ACCESS TIME MEMORY CACHE	RAM 421 CIP MULTI- LAYER APPROACH FOR OPTIMIZING FERROELECTRIC FILM PERFORMANCE		Ramfron No. Patent Application
TECHNIQUE FOR REDUCING ELEMENT 09/069 468 DISABLE FUSE PITCH REQUIREMENTS IN	ICING 09/022,106	DD 09/090.575	08/915,054	 CE 09/021.132	MZING 09/064 465	IIZING 08/896,584 :E	Serial No.
4/29/96 EMS	2/11/98 RIC	6/4/98 R†C	8/20/97 R I C	2/10/98 RIC	4/22/98 R I C	7/18/97 RIC	Filing Date Assignee
EDRAM	FRAM	FRAM	FRAM	EDRAM, FRAM	FRAM	FRAM	Tech
MOBLEY, KENNETH J.	KRAUS, WILLIAM F	SANJAY MITRA, ET AL	MOSCALUK, GARYP	TAYLOR CRAIG ET AL	EASTEP BRIANL	EASTEP: BRIAN LEE	inventor

ALLEN, J., ET AL.	FRAM	11/14/97 R I C	08/970,454	COLUMN OF COOF CONFIGURATION FOR A 1TH C FERROFLECTRIC MEMORY	RAM 437
ALLEN, J. ET AL	FRAM	11/14/97 R I C	08/970,519	SENSE AMPLIFIER CONFIGURATION FOR A	RAM 436
ALLEN J ETAL	FRAM	11/14/97 R I C	08/970.518	REFERENCE CELL CONFIGURATION FOR A	RAM 435
ALLEN, J. ET AL	FRAM	11/1497 RIC	06/970,520	MEMORY CELL CONFIGURATION FOR A	RAM 434
WILSON D. ET AL	FRAM	11/14/97 R1C	08/970,452	REFERENCE CELL FOR A 11/1C FERROELECTRIC MEMORY	RAM 433
EORAM MOBLEY KENNETH J	EORAM	7/8/98 EMS	09/111.822	BLOCK-TO-BLOCK SHARING OF WRITE OECODER	RAM 432
EORAM MOBLEY KENNETH J	EORAM	7/8/98 EMS	09/112,223	MEMORY DEVICE, AND ASSOCIATED METHOD, HAVING DEDICATED BURST ADDRESS BUS	
MOBLEY, KENNETH J	EORAM	9/3/98 EMS	09/146,726	OYNAMIC RANDOM ACCESS MEMORY WORD LINE BOOST TECHNIQUE EMPLOYING A BOOST-ON-WRITES POLICY	RAM 430
Inventor	Туре	Dale Assignee	Serial No.	Patent Application	Ramiron No.

Ramiron No.	Palent Application	Serial No.	Filing Date Assignee	ī ech	Inventor
RAM 438	SENSE AMPLIFIER LATCH DRIVER CIRCUIT FOR A 11/1C FERROELECTRIC MEMORY		11/14/97 R + C	FRAM	WILSON D
RAM 439	PLATE LINE ORIVER CIRCUIT FOR A 17/1C FERROELECTRIC MEMORY	08/970 522	11/14/97 R 1 C	FRAM	KRAUS W ETAL
:: RAM 440	PLATE LINE SEGMENTATION IN A 17/1C FERROELECTRIC MEMORY	08/970,448	11/14/97 R1C	FRAM	KRAUS W ET AL
RAM 441	-WINOOW OF UNCERTAINTY MINIMIZER FOR A MULTIPLE-INPUT LOGIC CIRCUIT	09/027,881	2/23/98 R I C	FRAM	MOSCALUK GARYP, ET
RAM 442	FERROELECTRIC THIN FILMS AND SOLUTIONS COMPOSITIONS AND PROCESSING	09/061,362	4/15/98 R I C Mitsubish FRAM	h FRAM	SUN, SHAN, ET AL
RAM 443	CMOS RC EQUIVALENT DELAY CIRCUIT	09/087,726	5/29/98 R I C	FRAM	MOSCALUK, GARY
RAM 444	FERROELECTRIC MEMORY DEVICE STRUCTURE USEFUL FOR PREVENTING HYDROGENLINE DEGRADATION	09/177,392	10/23/98 R I C	FRAM	EVANS, THOMAS A

RAM 448	RAM 447	RAM 446	<u>;</u>
MEMORY DEVICE HAVING MULTI-BANK SRAM REGISTERS	EMBEDDED ENHANCED DRAM, AND ASSOCIATED METHOD	HYDROGEN BARRIER ENCAPSULATION TECHNIQUES FOR THE CONTROL OF THYDROGEN INDUCED DEGRADATION OF FERROELECTRIC CAPACITORS IN CONJUNCTION WITH MULTIHE VEL METAL PROCESSING FOR NON-VOLATILE PROCESSING FOR CONTROL THE INTEGRATED CIRCUIT MEMORY DEVICES	Basast Application
09/178,298	640 801/60	D9/164 952	Serial No.
10/23/98	SW3 66/0C/9	10/1/98 R1C	Flung Dale Assignee
EDRAM	EORAM	FRAM	Tech
EDRAM PETERS, MICHAEL	EDRAM ALWAIS MICHAEL ET AL 6/30/99	BAILEY RICHARD A. ET 101799 AL	Invenior
10/23/99	T AL 6/30/99		

FIRST AMENDMENT TO PATENT SECURITY AGREEMENT

THIS FIRST AMENDMENT TO PATENT SECURITY AGREEMENT (this "Amendment") is dated as of January /5, 1999 by and between RAMTRON
INTERNATIONAL CORPORATION (the "Debtor"), having a mailing address of 1850 Ramtron Drive, Colorado Springs, Colorado 80921, and NATIONAL ELECTRICAL BENEFIT FUND, having a mailing address of 1125 Fifteenth Street, N.W., Washington, D.C. 20005 (the "Secured Party" or "Lender").

W I T N E S S E T H

WHEREAS, in connection with that certain Loan Agreement dated as of August 31, 1995 between the Debtor and the Secured Party (as amended, the "Loan Agreement"), the Debtor executed in favor of the Secured Party that certain Patent Security Agreement dated as of August 31, 1995 (the "Patent Security Agreement"; terms being used herein shall have the meanings given them in such Patent Security Agreement);

WHEREAS, the Patent Security Agreement provides that the Debtor will, from time to time, execute such additional documents and instruments to assure the Secured Party of the full benefit intended to be created thereby, and

WHEREAS, the Secured Party has requested that Debtor execute this Amendment in order to reflect the Debtor's acquisition of rights in patents and patent applications subsequent to the execution of the Patent Security Agreement.

NOW THEREFORE, Debtor and Secured Party hereby agree as follows:

- 1. Supplement to Schedule A. In order to reflect the Debtor's acquisition of additional patents and patent applications since the date of the Patent Security Agreement, from and after the date hereof, the Schedule "A" attached thereto shall be deemed supplemented and modified by the "Schedule A Supplement" attached hereto. Each of the patents and patent applications reflected on the Schedule A Supplement shall be covered by the Patent Security Agreement and be deemed "Collateral" thereunder. For the avoidance of doubt, Debtor acknowledges that it has granted to the Secured Party a first priority security interest in and has conditionally assigned to Secured Party all of its right, title and interest in and to the patents and patent applications set forth on Schedule A to the Patent Security agreement (as supplemented as provided herein), including, without limitation, with respect to the patents and patent applications set forth on the Schedule A Supplement attached hereto.
- 2. Warranties and Representation. Debtor hereby warrants and represents to the Secured

PAATENT REEL: 025448**PA**AN**£**9**30**14

Party the following:

- (a) Schedule A to the Patent Security Agreement (as supplemented by this Amendment) is a true and complete schedule setting forth all patents and patent applications owned or controlled by Debtor, or licensed to Debtor, together with a summary description and full information in respect of the filing or issuance thereof and expiration dates therefor;
- (b) To the Knowledge of Debtor, each of such patents is valid and enforceable, and Debtor is not presently aware of any past, present or prospective claim by a third party that any of the patents are invalid or unenforceable, or that the use of any patents violates the rights of any third person, or of any basis for any such claims;
- (c) To the Knowledge of Debtor, Debtor is the sole and exclusive owner (or co-owner, as the case may be) of the entire and unencumbered right, title and interest in and to each of such patents and patent applications, free and clear of any liens, charges and encumbrances, including, without limitation, piedges, assignments, licenses, shop rights and covenants by Debtor not to sue third persons;
- (d) Debtor has used and will continue to use its best efforts to use proper statutory notice in connection with its use of each of the patents; and
- (e) Except for the filings with the United States Patent and Trademark Office necessary to perfect the security interests created hereunder with respect to those patents and patent licenses listed on the Schedule A Supplement to this Amendment, no authorization, approval or other action by, and no notice to or filing with, any governmental authority or regulatory body is required either for the grant by Debtor of the security interest hereunder or for the execution, delivery or performance of this agreement by Debtor or for the perfection of or the exercise by Secured Party of its rights hereunder to the Collateral in the United States.

It is acknowledged and agreed that it shall be an Event of Default under the Patent Security Agreement and the Loan Agreement if any representation or warranty set forth above is incorrect as of the time made.

- 3. No Other Amendments. Other than as expressly provided for herein, the Patent Security Agreement shall remain unamended and in full force and effect.
- 4. Governing Law. All acts and transactions hereunder and the rights and obligations of the parties hereto shall be governed, construed and interpreted in accordance with the laws of the State of Colorado.
- 5. <u>Counterparts</u>. This Amendment may be executed by the parties in counterpart, each of which shall be deemed an original, and, when taken together, one and the same document.

PAATENT REEL: 925448PAATME99015 IN WITNESS WHEREOF, the Debtor and the Secured Party have executed this Amendment by their duly authorized officers as of the date first above written.

By:

RAMTRON INTERNATIONAL CORPORATION

Name: Richard L. Mohr

Title: Executive Vice President and CFO

NATIONAL ELECTRICAL BENEFIT FUND

Edwin D. Hill, Trustee

STATE OF COLORADO)
) ss.
COUNTY OF EL PASO)
The foregoing instru	ments was acknowledged before me this مريح day of المعسمة 1999, by
Kichard L. Mohr, President of R	tamtron International Corporation.
EXECUTIVE	VP CFO
My commission expi	res 7ebmay 7, 2002 Witness my hand and official seal
	a Kill Sen C
	Tathleen III. Gan
	Notary Public

PAAFINT REEL: 925448814481699917

DISTRICT OF COLUMBIA)
) ss.
CITY OF WASHINGTON)
I, RISHA L. DAVIS_, a Notary Public in and for the aforesaid jurisdiction, do hereby
certify that / Edwin D. Hill , as Trustee of the National Electrical Benefit Fund, who subscribed
to the foregoing and annexed instrument dated as of JANUARY 15, 1999, is personally known to me,
and appeared before me this day in person and acknowledged that he signed and delivered said
instrument on behalf of the National Electrical Benefit Fund, for the purposes therein set forth.
Given under my hand and notarial seal this 4th day of Leveny, 1999.
Last I. On
Alaran Bublic
Notary Public
Cinglish L. Destiles Wordery Publish Policies of Orderstate My commission expires: http://doi.org/10.1002
My commission expires:

SCHEDULE A SUPPLEMENT

PATENTS

RAM No.	Tech Type	Title	Patent No.	issued	Expires	Inventor
RAM 398	FRAM	IRIDIUM OXIDE LOCAL INTERCONNECT	5.838.605	11/17/98	3/20/16	BAILEY. RICHARD A.
26C MAS	EDRAM	EDRAM WITH INTEGRATED GENERATION AND CONTROL OF WRITE ENABLE AND COLUMN LATCH SIGNALS AND METHOD OF MAKING SAME	5 935,442	11/1 0/98	3:22/18	JOS EPH, JAMES DEAN, ET.
RAM 371 DIV	FRAM	A VOLTAGE REFERENCE FOR A FERROELECTRIC 17/10 BASED MEMORY	5.822,237	10/13/98	9/1 6/14	WILSON, GENNIS R. ET AL.
RAM 409	MARC	SEMICONDUCTOR MEMORY DEVICE	5,818.771	10/6/98	9/30/16	YASU, YOSHIKO, ET AL.
RAM 384 DIV	FRAM	CIRCUIT AND METHOD FOR REDUCING COMPENSATION OF A FERROELECTRIC CAPACITOR BY MULTIPLE PULSING OF THE PLATE LINE FOLLOWING A WRITE OPERATION	5 815.430	9/ 29/98	₩1 0/ 15	VERHAEGHE. DONALD J!
RAM 412	FRAM	LOW-POWER NON-RESETABLE TEST MODE CIRCUIT	5.804,995	9/8/98	2:13/17	VERHAEGHE, DONALD J.,
RAM 410	FRAM DRAM	SYSTEM AND METHOD PROVIDING SELECTIVE WRITE PROTECTION FOR INDIVIDUAL SUCKS OF MEMORY IN A NON-VOLATILE MEMORY DÉVICE		9/1/98	10/30/1	S YE AGER. E TAL
RAM 390	EORA	M MULTIBUS CACHED MEMORY SYSTEM	5.802.560	9/1/98	8/ 30 /1	5 JOSEPH, JAMES C., ET A:
RAM 396 DIV	FRAM	USE OF CALCIUM AND STRONTIUM DOPANTS TO IMPROVE RETENTION PERFORMANCE IN A PZT FERROELECTRIC FILM	5. 600.683	9/1/96	3/1 5/ 1	6 KAMMERDINER, LEE, ET
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RAM 388	FRAN		5,774,392	6/30/98	3/ 28/	16 KRAUS, WILLIAM F, ET A
RAM 403	FRAN	A SYSTEM AND METHOD FOR MITIGATING IMPRINT EFFECT IN FERR DELECTRIC RANDO ACCESS MEMORIES UTILIZING A COMPLEMENTARY DATA PATH	5,7 45 ,403 M	4/28/98	2/24/	17 TAYLOR, CRAIG
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RAM 343 CIF	? EDR	AM ENHANCED DRAM WITH EMBEDDED REGISTE	ERS 5,699,317	12/16/97	1/22	/12 SARTORE, RONALD H
RAM 404	FRA	M SAME STATE AND OPPOSITE STATE DIAGNOSTIC TEST FOR FERRDELECTRIC MEMORIES	5,661.730	8/26/97	9/27	/16 MITRA. SANJAY, ET AL,
RAM 321	0RA	.M PROCESS FOR FABRICATING TRANSISTORS USING COMPOSITE NITRIDE STRUCTURE	5,610.099	3/11/9:	7 6/ 28	114 LARSON, WILLIAM L.
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R AM 3 67	FRA	M FERROELECTRIC NONVOLATILE RANDOM ACCESS MEMORY UTILIZING SELF-BOOTSTRAPPING PLATE LINE SEGMENT DRIVERS	5, 598 ,366	1/28/9	7 8/10	8/15 KRAUS, WILLIAM F., ET
RAM 384	FR.	AM CIRCUIT AND METHOD FOR REDUCING COMPENSATION OF A FERROELECTRIC CAPACITOR BY MULTIPLE PULSING OF THE PLATE LINE FOLLOWING A WRITE OPERATION.	5,592,410 ON	1 <i>/7/</i> 5	1 7 41	OV15 VERHAEGHE, DONALC
G 200 MAP	(V = R	AM STACKED FERROELECTRIC MEMORY CELL. METHOD		12/3/5	96 5·2	9/11 LARSON, WILLIAM L.
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RAM 371	FRAM	VOLTAGE REFERENCE FOR A FERROELECTRIC	5.572.459	11/5/96	9/16/14	WILSON, DENNIS R., ET AL
RAM 381	EDRAM	CIRCUIT WITH A SINGLE ADDRESS REGISTER THAT AUGMENTS A MEMORY CONTROLLER BY ENABLING CACHE READS AND PAGE-MODE WRITES	5 566,318	10/15/96	3/2/14	JOSEPH, JAMES D.
RAM 382	FRAM	FERROELECTRIC MEMORY SENSING METHOD USING DISTINCT READ AND WRITE VOLTAGES	5 532.953	7/2/96	3:29/15	RUESCH, ROONEY A., ET A
RAM 370	FRAM	FERROELECTRIC MEMORY SENSING SCHEME USING BIT LINES PRECHARGED TO A LOGIC ONE VOLTAGE	S 530.668	6/25/96	₩12/15	CISERN, WEN-FOO, ET AL.
9AM 374	FRAM	FERROELECTRIC CAPACITOR RENEWAL	5.525.529	6/ 11/96	5/ 5/1 4	PERINO, STANLEY, ET AL.
PAM 352 FWC	FRAM	SEMICONDUCTOR DEVICE HAVING A TRANSISTOR A FERROELECTRIC CAPACITOR AND A HYDROGEN BARRIER FILM	5,523,595	6/ 4/95	÷4/13	TAKENAKA, KAZUHIRO, E
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RAM 332 FW0	2 FRAM		D 5,495,117	2/27/96	2/ 27/ 1	3 LARSON, WILLIAM L
RAM 376	FRAM	· · · · · · · · · · · · · · · · · · ·	5,479,132	12/26/95		4 VERHAEGHE, DONALO, I
RAM 358 FW0	CZ FRAM		5,475,248	12/12/95	12/ 12/	12 TAN ENAKA , K.

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PATENT APPLICATIONS

RAM 343 DIV/CD RAM 343 DIV/CD	Palent Application ENHANCED DRAM WITH EMBEDDED REGISTERS ENHANCED DRAM WITH EMBEDDED REGISTERS INTEGRATION OF HIGH VALUE CAPACITOR	Serial No. 08/888 371 09/182 994	Filing Assi Date Assi 7/3/97 EMS 10/30/98 EMS	Assignee VIS	Tech gnee Type Inventor EDRAM SARTORE RONALD H ET AL EDRAM SARTORE RONALD H ET AL FRAM YEAGER MICHAEL W RF/10 ET AL
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RA:: 389	COMPUTER HYBRID MEMORY INCLUDING DRAM AND EDRAM MEMORY COMPONENTS, WITH SECONDARY CACHE IN EDRAM FOR DRAM	08/615.392		3/14/98 EMS	3/1496 EMS EORAM
RAM 391	PROGRAMMABLE OUTPUT DEVICES FOR CONTROLLING SIGNAL LEVELS IN AN RF/ID TRANSPONDER	08/521 251		8/30/95 R I C	8/30/95 RIC RFID
RAM 392 DIV	METHOD OF MANUFACTURING IRIDIUM ELECTRODE FOR STRONTIUM BISMUTH TANTALATE FERROELECTRIC CAPACITORS	08/896, 329		7117/97 RIC	7/17/97 RIC FRAM

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,		2/28/97 RIC	08/810,607	SERIAL FRAM ARCHITECTURE TO EQUALIZE COLUMN ACCESS	RAM 402
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EASTEP, BRIAN, C YE	FRAM	5/27/98 R I C	09/085,280	COMPLETELY ENCAPSULATED TOP ELECTRODE OF A FERROELECTRIC CAPACITOR USING A LEAD-ENHANCED ENCAPSULATION LAYER	RAM 407 CIP3
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AL THOMAS A ET	FRAM	10/11/96 R I C	08/728 740	PARTIALLY OR COMPLETELY ENCAPSULATED TOP ELECTRODE OF A FERROELECTRIC CAPACITOR	RAM 407 CIP
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MOBLEY, KENNETH J. ET AL	EDRAM	2998 EMS	09/023,656	SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY DEVICE INCORPORATING A STATIC RAM CACHE	RAM 420
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ALWAIS MICHAEL ET AL	EDRAM	5/2/97 EMS	08/850,802	ENHANCED SIGNAL PROCESSING RANDOM ACCESS MEMORY DEVICE UTILIZING A DRAM MEMORY ARRAY INTEGRATED WITH AN ASSOCIATED SRAM CACHE AND INTERNAL REFRESH CONTROL	RAM 417
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EASTEP, BRIAN LEE	FRAM	7/18/97 RIC	08/896 684	MULTI-LAYER APPROACH FOR OPTIMIZING FERROELECTRIC FILM PERFORMANCE	RAM 421
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Damiron No.	Palent Application	Serial No.	Filing Date Assignee	Tech	inventor
RAM 430	DYNAMIC RANDOM ACCESS MEMORY WORD LINE BOOST TECHNIQUE EMPLOYING A BOOST ON WRITES POLICY	09/146,726	SW3 BEAZIG	EDRAM	MOBLEY, KENNETH J
RAM 431	MEMORY DEVICE, AND ASSOCIATED METHOD, HAVING DEDICATED BURST ADDRESS BUS	09/112.223	7/8/98 EMS	EDRAM	EDRAM MOBLEY KENNETH J
RAM 432	BLOCK TO BLOCK SHARING OF WRITE DECODER	09/111.822	7/8/98 EMS	EDRAM	MOBLEY KENNETH J
RAM 433	REFERENCE CELL FOR A 1T/IC FERROELECTRIC MEMORY	08/970,452	(1/14/97 R I C	FRAM	WILSON D ETAL
RAM 434	MEMORY CELL CONFIGURATION FOR A 17/1C FERROELECTRIC MEMORY	08/970.520	11/14/97 R I C	FRAM	ALLEN J ETAL
RAM 435	REFERENCE CELL CONFIGURATION FOR A	08/970.518	11/14/97 R I C	FRAM	ALLEN. J. ET AL
RAM 436	SENSE AMPLIFIER CONFIGURATION FOR A 11/1C FERROELECTRIC MEMORY	08/970.519	11/14/97 R I C	FRAM	ALLEN, J. ETAL
RAM 437	COLUMN DECODER CONFIGURATION FOR A 1711C FERROELECTRIC MEMORY	08/970,454	15/14/97 R 1 C	FRAM	ALLEN, J., ET AL.

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RAM 448	RAM 447	RAM 446	Ramiron No.
MEMORY DEVICE HAVING MULTI-BANK SRAM REGISTERS	EMBEOGEO ENHANCEO DRAM, ANO ASSOCIATEO METHOD	HYDROGEN BARRIER ENCAPSULATION TECHNIQUES FOR THE CONTROL OF HYDROGEN INDUCEO DEGRADATION OF FERROELECTRIC CAPACITORS IN CONJUNCTION WITH MULTILEVEL METAL PROCESSING FOR NON-VOLATILE MATEGRATED CIRCUIT MEMORY DEVICES	Pateni Application
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EDRAM	EORAM	FRAM	Tech
EDRAM PETERS, MICHAEL	EORAM ALWAIS MICHAEL ET AL 8/30/99	AL	Inventor
1/23/99	6/30/99	Q. S	3