PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	CORRECTIVE ASSIGNMENT
NATURE OF CONVEYANCE:	Corrective Assignment to correct the Conveying Party and the Receiving Party previously recorded on Reel 009756 Frame 0085. Assignor(s) hereby confirms the Conveying Party is Ramtron International Corporation; and the Receiving Party is National Electrical Benefit Fund..

CONVEYING PARTY DATA

Name	Execution Date
Ramtron International Corporation	01/15/1999

RECEIVING PARTY DATA

Name:	National Electrical Benefit Fund
Street Address:	1125 Fifteenth Street N.W.
City:	Washington
State/Country:	DISTRICT OF COLUMBIA
Postal Code:	20005

PROPERTY NUMBERS Total: 1

Property Type	Number
Patent Number:	5963481

CH $40.00 5963481

CORRESPONDENCE DATA

Fax Number: (312)913-0002
Correspondence will be sent via US Mail when the fax attempt is unsuccessful.
Phone: 3129130001
Email: docketing@mbhb.com
Correspondent Name: McDonnell Boehnen Hulbert & Berghoff LLP
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Address Line 4: Chicago, ILLINOIS 60606

ATTORNEY DOCKET NUMBER:	07-397
NAME OF SUBMITTER:	Thomas J. Loos

Total Attachments: 26
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(Rev. 6-93)
OMB No. 0651-0011 (exp. 4/94)

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RECORDATION FOR PATENTS

02-26-1999

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or copy thereof.

To the Honorable Commissioner of Patents and Trademarks: Pl

1999 FEB 23 AM 10:57

1. Name of conveying party(ies):

National Electrical Benefit Fund

MRD 2-23-99

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies)

Name: Ramtron International Corporation

Internal Address:

Street Address: 1850 Ramtron Drive

City: Colorado Springs State: CO ZIP: 80921

Additional name(s) & address(es) attached? ☐ Yes ☒ No

3. Nature of conveyance:

☐ Assignment ☐ Merger

☐ Security Agreement ☐ Change of Name

☒ Other First Amendment to Patent Sec. Agmnt.

Execution Date: January 15, 1999

4. Application number(s) or patent number(s):

If this document is being filed together with a new application, the execution date of the application is:

A. Patent Application No.(s)	B. Patent No.(s)
SEE ATTACHED	SCHEDULE A SUPPLEMENT

Additional numbers attached? ☒ Yes ☐ No

5. Name and address of party to whom correspondence concerning document should be mailed:

Name: Anthony F. Lo Cicero, Esq.

Internal Address:

AMSTER, ROTHSTEIN & EBENSTEIN

Street Address: 90 Park Avenue

City: New York State: NY ZIP: 10016

6. Total number of applications and patents involved: 83

7. Total fee (37 CFR 3.41).....$ 3,320.00

☒ Enclosed

☐ Authorized to be charged to deposit account

8. Deposit account number:

01-1785

(Attach duplicate copy of this page if paying by deposit account)

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9. Statement and signature.

To the best of my knowledge and belief, the foregoing information is true and correct and any attached copy is a true copy of the original document.

Anthony F. Lo Cicero — Name of Person Signing

Signature

02-22-99 — Date

Total number of pages including cover sheet, attachments, and document:

Mail documents to be recorded with required cover sheet information to:
Commissioner of Patents & Trademarks, Box Assignments
Washington, D.C. 20231

SCHEDULE A SUPPLEMENT

PATENTS

RAM No.	Tech Type	Title	Patent No.	Issued	Expires	Inventor
RAM 398	FRAM	IRIDIUM OXIDE LOCAL INTERCONNECT	5,838,605	11/17/98	3/20/16	BAILEY, RICHARD A.
RAM 393	EDRAM	EDRAM WITH INTEGRATED GENERATION AND CONTROL OF WRITE ENABLE AND COLUMN LATCH SIGNALS AND METHOD OF MAKING SAME	5,835,442	11/10/98	3/22/16	JOSEPH, JAMES DEAN, ET
RAM 371 DIV	FRAM	A VOLTAGE REFERENCE FOR A FERROELECTRIC 1T/1C BASED MEMORY	5,822,237	10/13/98	9/16/14	WILSON, DENNIS R. ET AL
RAM 409	DRAM	SEMICONDUCTOR MEMORY DEVICE	5,818,771	10/6/98	9/30/16	YASU, YOSHIKO, ET AL
RAM 384 DIV	FRAM	CIRCUIT AND METHOD FOR REDUCING COMPENSATION OF A FERROELECTRIC CAPACITOR BY MULTIPLE PULSING OF THE PLATE LINE FOLLOWING A WRITE OPERATION	5,815,430	9/29/98	4/10/15	VERHAEGHE, DONALD J..
RAM 412	FRAM	LOW-POWER NON-RESETABLE TEST MODE CIRCUIT	5,804,996	9/8/98	2/13/17	VERHAEGHE, DONALD J..
RAM 410	FRAM DRAM	SYSTEM AND METHOD PROVIDING SELECTIVE WRITE PROTECTION FOR INDIVIDUAL BLOCKS OF MEMORY IN A NON-VOLATILE MEMORY DEVICE	5,802,583	9/1/98	10/30/16	YEAGER, ET AL.
RAM 390	EDRAM	MULTIBUS CACHED MEMORY SYSTEM	5,802,560	9/1/98	8/30/15	JOSEPH, JAMES D., ET AL
RAM 396 DIV	FRAM	USE OF CALCIUM AND STRONTIUM DOPANTS TO IMPROVE RETENTION PERFORMANCE IN A PZT FERROELECTRIC FILM	5,800,683	9/1/98	3/15/16	KAMMERDINER, LEE, ET
RAM 385	FRAM	FABRICATION OF METAL-FERROELECTRIC-METAL CAPACITORS WITH A TWO-STEP PATTERNING SEQUENCE	5,789,323	8/4/98	4/25/15	TAYLOR, THOMAS C.
RAM 388	FRAM	BOOTSTRAPPING CIRCUIT UTILIZING A FERROELECTRIC CAPACITOR	5,774,392	6/30/98	3/28/16	KRAUS, WILLIAM F. ET A
RAM 403	FRAM	SYSTEM AND METHOD FOR MITIGATING IMPRINT EFFECT IN FERROELECTRIC RANDOM ACCESS MEMORIES UTILIZING A COMPLEMENTARY DATA PATH	5,745,403	4/28/98	2/28/17	TAYLOR, CRAIG
RAM 343 CCN	EDRAM	ENHANCED DRAM WITH EMBEDDED REGISTERS	5,721,862	2/24/98	2/24/15	SARTORE, RONALD H..
RAM 343 CIP	EDRAM	ENHANCED DRAM WITH EMBEDDED REGISTERS	5,699,317	12/16/97	1/22/12	SARTORE, RONALD H..
RAM 404	FRAM	SAME STATE AND OPPOSITE STATE DIAGNOSTIC TEST FOR FERROELECTRIC MEMORIES	5,661,730	8/26/97	9/27/16	MITRA, SANJAY, ET AL.
RAM 321	DRAM	PROCESS FOR FABRICATING TRANSISTORS USING COMPOSITE NITRIDE STRUCTURE	5,610,099	3/11/97	6/28/14	LARSON, WILLIAM L.
RAM 368 FWC	FRAM RF/ID	INTEGRATION OF HIGH VALUE CAPACITOR WITH FERROELECTRIC MEMORY	5,608,246	3/4/97	3/4/14	YEAGER, MICHAEL W..
RAM 387	FRAM	FERROELECTRIC NONVOLATILE RANDOM ACCESS MEMORY UTILIZING SELF-BOOTSTRAPPING PLATE LINE SEGMENT DRIVERS	5,598,366	1/28/97	8/16/15	KRAUS, WILLIAM F., ET
RAM 384	FRAM	CIRCUIT AND METHOD FOR REDUCING COMPENSATION OF A FERROELECTRIC CAPACITOR BY MULTIPLE PULSING OF THE PLATE LINE FOLLOWING A WRITE OPERATION	5,592,410	1/7/97	4/10/15	VERHAEGHE, DONALD
RAM 332 DIV	FRAM	STACKED FERROELECTRIC MEMORY CELL AND METHOD	5,580,814	12/3/96	5/29/11	LARSON, WILLIAM L.
RAM 379 DIV	FRAM	PASSIVATION METHOD AND STRUCTURE USING HARD CERAMIC MATERIALS OR THE LIKE	5,578,867	11/26/96	3/11/14	ARGOS, GEORGE, ET

12/2/98

RAM No.	Tech Type	Title	Patent No.	Issued	Expires	Inventor
RAM 371	FRAM	VOLTAGE REFERENCE FOR A FERROELECTRIC 1T/1C BASED MEMORY	5,572,459	11/5/96	9/16/14	WILSON, DENNIS R., ET AL.
RAM 381	EDRAM	CIRCUIT WITH A SINGLE ADDRESS REGISTER THAT AUGMENTS A MEMORY CONTROLLER BY ENABLING CACHE READS AND PAGE-MODE WRITES	5,566,318	10/15/96	3/2/14	JOSEPH, JAMES D.
RAM 382	FRAM	FERROELECTRIC MEMORY SENSING METHOD USING DISTINCT READ AND WRITE VOLTAGES	5,532,953	7/2/96	3/29/15	RUESCH, RODNEY A., ET A
RAM 370	FRAM	FERROELECTRIC MEMORY SENSING SCHEME USING BIT LINES PRECHARGED TO A LOGIC ONE VOLTAGE	5,530,668	6/25/96	4/12/15	CHERN, WEN-FOO, ET AL.
RAM 374	FRAM	FERROELECTRIC CAPACITOR RENEWAL METHOD	5,525,528	6/11/96	5/6/14	PERINO, STANLEY, ET AL.
RAM 352 FWC	FRAM	SEMICONDUCTOR DEVICE HAVING A TRANSISTOR A FERROELECTRIC CAPACITOR AND A HYDROGEN BARRIER FILM	5,523,595	6/4/96	4/4/13	TAKENAKA, KAZUHIRO, E
RAM 377 CON	FRAM	FILM HAVING FERROELECTRIC BISMUTH LAYERED OXIDES	5,519,566	5/21/96	6/15/14	PERINO, STANLEY C., ET
RAM 378	FRAM	LAYERED LOCAL INTERCONNECT COMPATIBLE WITH INTEGRATED CIRCUIT FERROELECTRIC CAPACITORS	5,498,569	3/12/96	8/22/14	EASTEP, BRIAN
RAM 332 FWC2	FRAM	STACKED FERROELECTRIC MEMORY CELL AND METHOD	5,495,117	2/27/96	2/27/13	LARSON, WILLIAM L.
RAM 376	FRAM	NOISE AND GLITCH SUPPRESSING FILTER WITH FEEDBACK	5,479,132	12/26/95	6/6/14	VERHAEGHE, DONALD, E
RAM 358 FWC2	FRAM	SEMICONDUCTOR DEVICE WITH A CONDUCTIVE REACTION-PREVENTING FILM	5,475,248	12/12/95	12/12/12	TANENAKA, K.

PATENT APPLICATIONS

Ramtron No.	Patent Application	Serial No.	Filing Date	Assignee	Tech Type	Inventor
RAM 343 DIV	ENHANCED DRAM WITH EMBEDDED REGISTERS	08/888,371	7/3/97	EMS	EDRAM	SARTORE, RONALD H., ET AL
RAM 343 DIV/CD	ENHANCED DRAM WITH EMBEDDED REGISTERS	09/182,994	10/30/98	EMS	EDRAM	SARTORE, RONALD H., ET AL
RAM 368 DIV	INTEGRATION OF HIGH VALUE CAPACITOR	08/544,470	10/18/95	R I C	FRAM RFID	YEAGER, MICHAEL W., ET AL
RAM 389	COMPUTER HYBRID MEMORY INCLUDING DRAM AND EDRAM MEMORY COMPONENTS, WITH SECONDARY CACHE IN EDRAM FOR DRAM	08/615,392	3/14/96	EMS	EDRAM	JOSEPH, JAMES DEAN
RAM 391	PROGRAMMABLE OUTPUT DEVICES FOR CONTROLLING SIGNAL LEVELS IN AN RF/ID TRANSPONDER	08/521,251	8/30/95	R I C	RFID	DOWNS, JEFFREY E., ET AL
RAM 392 DIV	METHOD OF MANUFACTURING IRIDIUM ELECTRODE FOR STRONTIUM BISMUTH TANTALATE FERROELECTRIC CAPACITORS	08/896,329	7/17/97	RIC	FRAM	PERINO, STANLEY, ET AL

Ramtron No.	Patent Application	Serial No.	Filing Date	Assignee	Tech Type	Inventor
RAM 394	DYNAMIC CACHE SIZING MEMORY	08/630,489	4/10/96	EMS	EDRAM	HEISLER, DOYLE JAMES, ET AL
RAM 396	THE USE OF CALCIUM AND STRONTIUM DOPANTS TO IMPROVE RETENTION PERFORMANCE IN A PZT FERROELECTRIC FILM	08/616,856	3/15/96	R I C	FRAM	KAMMERDINER, LEE ET AL
RAM 397	A METHOD OF MEASURING RETENTION PERFORMANCE AND IMPRINT DEGRADATION OF FERROELECTRIC FILMS	08/616,913	3/15/96	R I C	FRAM	TRAYNOR, STEVEN
RAM 398 DIV	IRIDIUM OXIDE LOCAL INTERCONNECT	09/183,545	10/29/98	R I C	FRAM	BAILEY, RICHARD A
RAM 399	YIELD ENHANCEMENT TECHNIQUE FOR INTEGRATED CIRCUIT PROCESSING TO REDUCE EFFECTS OF UNDESIRED DIELECTRIC MOISTURE RETENTION AND SUBSEQUENT HYDROGEN OUT-DIFFUSION	08/728,256	10/8/96	R I C	FRAM	ARGOS, GEORGE JR., ET AL
RAM 400	LOW VOLTAGE BOOTSTRAPPING CIRCUIT	08/663,032	6/7/96	R I C	FRAM DRAM	VERHAEGHE, DONALD J., ET AL
RAM 402	SERIAL FRAM ARCHITECTURE TO EQUALIZE COLUMN ACCESS	08/810,607	2/28/97	R I C	FRAM	TAYLOR, CRAIG

Ramtron No.	Patent Application	Serial No.	Filing Date	Assignee	Tech Type	Inventor
RAM 405	BANDGAP REFERENCE BASED POWER-ON OETECT CIRCUIT INCLUDING A SUPPRESSION CIRCUIT	08/702,363	8/23/96	R I C	FRAM	KRAUS, WILLIAM F
RAM 405 CON	BANDGAP REFERENCED BASED POWER-ON OETECT CIRCUIT	09/017,577	2/3/98	RIC	FRAM	KRAUSE, WILLIAM F
RAM 406	DATA PROCESSOR INCORPORATING A FERROELECTRIC MEMORY ARRAY SELECTABLY CONFIGURABLE AS READ/WRITE AND READ ONLY MEMORY	08/734,802	10/21/96	R I C	FRAM	DOWNS, JEFFERY E
RAM 407	PARTIALLY OR COMPLETELY ENCAPSULATED TOP ELECTRODE OF A FERROELECTRIC CAPACITOR	08/700,076	8/20/96	R I C	FRAM	EVANS, THOMAS A., ET AL
RAM 407 CIP	PARTIALLY OR COMPLETELY ENCAPSULATED TOP ELECTRODE OF A FERROELECTRIC CAPACITOR	08/728,740	10/11/96	R I C	FRAM	EVANS, THOMAS A., ET AL
RAM 407 CIP2	PARTIALLY OR COMPLETELY ENCAPSULATED TOP ELECTRODE OF FERROELECTRIC CAPACITOR	08/828,157	3/27/97	R I C	FRAM	EVANS, THOMAS A., ET AL
RAM 407 CIP3	COMPLETELY ENCAPSULATED TOP ELECTRODE OF A FERROELECTRIC CAPACITOR USING A LEAD-ENHANCED ENCAPSULATION LAYER	09/065,280	5/27/98	R I C	FRAM	EASTEP, BRIAN, ET AL

Ramtron No.	Patent Application	Serial No.	Filing Date	Assignee	Tech Type	Inventor
RAM 413	SYSTEM AND METHOD FOR CONTROLLING INTERNAL TEST MODES IN A NON-VOLATILE MEMORY THROUGH NORMAL ACCESSES	08/802,630	2/19/97	R I C Hitachi	FRAM	VERHAEGHE, DONALD J., ET AL
RAM 414	SENSING METHODOLOGY FOR A 1T/1C FERROELECTRIC MEMORY	08/970,453	11/14/97	R I C	FRAM	WILSON D., ET AL
RAM 415	DUAL-LEVEL METALIZATION METHOD FOR INTEGRATED CIRCUIT FERROELECTRIC DEVICES	08/853,527	5/9/97	R I C Fujitsu	FRAM	ARGOS, GEORGE, ET AL
RAM 417	ENHANCED SIGNAL PROCESSING RANDOM ACCESS MEMORY DEVICE UTILIZING A DRAM MEMORY ARRAY INTEGRATED WITH AN ASSOCIATED SRAM CACHE AND INTERNAL REFRESH CONTROL	08/850,802	5/2/97	EMS	EDRAM	ALWAIS, MICHAEL, ET AL
RAM 418	FIRST-IN, FIRST-OUT INTEGRATED CIRCUIT MEMORY DEVICE UTILIZING A DYNAMIC RANDOM ACCESS MEMORY ARRAY FOR DATA STORAGE IMPLEMENTED IN CONJUNCTION WITH AN ASSOCIATED STATIC RANDOM ACCESS MEMORY CACHE	08/840,118	4/1/97	EMS	EDRAM DRAM	TAYLOR, CRAIG
RAM 420	SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY DEVICE INCORPORATING A STATIC RAM CACHE	09/023,656	2/9/98	EMS	EDRAM	MOBLEY, KENNETH J., ET AL.

Ramtron No.	Patent Application	Serial No.	Filing Date	Assignee	Tech Type	Inventor
RAM 421	MULTI-LAYER APPROACH FOR OPTIMIZING FERROELECTRIC FILM PERFORMANCE	08/896,684	7/18/97	RIC	FRAM	EASTEP, BRIAN LEE
RAM 421 CIP	MULTI- LAYER APPROACH FOR OPTIMIZING FERROELECTRIC FILM PERFORMANCE	09/064,465	4/22/98	RIC	FRAM	EASTEP, BRIAN L
RAM 422	INTEGRATED CIRCUIT MEMORY OEVICE INCORPORATING A NON-VOLATILE MEMORY ARRAY AND A RELATIVELY FASTER ACCESS TIME MEMORY CACHE	09/021,132	2/10/98	RIC	EDRAM, FRAM	TAYLOR, CRAIG, ET AL
RAM 424	VOLTAGE BOOST CIRCUIT AND OPERATION THEREOF AT LOW POWER SUPPLY VOLTAGES	08/915,054	8/20/97	RIC	FRAM	MOSCALUK, GARY P
RAM 425	PLASTIC PACKAGE ASSEMBLY METHOD FOR A FERROELECTRIC-BASED INTEGRATED CIRCUIT	09/090,575	6/4/98	RIC	FRAM	SANJAY MITRA, ET AL
RAM 427	SENSE AMPLIFIER UTILIZING A BALANCING RESISTOR	09/022,106	2/11/98	RIC	FRAM	KRAUS, WILLIAM F
RAM 429	TECHNIQUE FOR REDUCING ELEMENT DISABLE FUSE PITCH REQUIREMENTS IN AN INTEGRATED CIRCUIT DEVICE INCORPORATING REPLACEABLE CIRCUIT ELEMENTS	09/069,468	4/29/98	EMS	EDRAM	MOBLEY, KENNETH J., ET AL.

Ramtron No.	Patent Application	Serial No.	Filing Date	Assignee	Tech Type	Inventor
RAM 430	OYNAMIC RANOOM ACCESS MEMORY WORO LINE BOOST TECHNIQUE EMPLOYING A BOOST-ON-WRITES POLICY	09/146,726	9/3/98	EMS	EORAM	MOBLEY, KENNETH J
RAM 431	MEMORY OEVICE, ANO ASSOCIATEO METHOO, HAVING OEOICATEO BURST AOORESS BUS	09/112,223	7/8/98	EMS	EORAM	MOBLEY KENNETH J
RAM 432	BLOCK-TO-BLOCK SHARING OF WRITE OECOOER	09/111,822	7/8/98	EMS	EORAM	MOBLEY, KENNETH J
RAM 433	REFERENCE CELL FOR A 1T/1C FERROELECTRIC MEMORY	08/970,452	11/14/97	RIC	FRAM	WILSON, D., ET AL
RAM 434	MEMORY CELL CONFIGURATION FOR A 1T/1C FERROELECTRIC MEMORY	08/970,520	11/14/97	RIC	FRAM	ALLEN, J., ET AL
RAM 435	REFERENCE CELL CONFIGURATION FOR A 1T/1C FERROELECTRIC MEMORY	08/970,518	11/14/97	RIC	FRAM	ALLEN, J., ET AL
RAM 436	SENSE AMPLIFIER CONFIGURATION FOR A 1T/1C FERROELECTRIC MEMORY	08/970,519	11/14/97	RIC	FRAM	ALLEN, J., ET AL
RAM 437	COLUMN OECOOER CONFIGURATION FOR A 1T/1C FERROELECTRIC MEMORY	08/970,454	11/14/97	RIC	FRAM	ALLEN, J., ET AL

Ramtron No.	Patent Application	Serial No.	Filing Date	Assignee	Tech Type	Inventor
RAM 438	SENSE AMPLIFIER LATCH DRIVER CIRCUIT FOR A 1T/1C FERROELECTRIC MEMORY	08/970,521	11/14/97	R I C	FRAM	WILSON D
RAM 439	PLATE LINE ORIVER CIRCUIT FOR A 1T/1C FERROELECTRIC MEMORY	08/970,522	11/14/97	R I C	FRAM	KRAUS W. ET AL
RAM 440	PLATE LINE SEGMENTATION IN A 1T/1C FERROELECTRIC MEMORY	08/970,448	11/14/97	R I C	FRAM	KRAUS W. ET AL
RAM 441	"WINOOW OF UNCERTAINTY" MINIMIZER FOR A MULTIPLE-INPUT LOGIC CIRCUIT	09/027,881	2/23/98	R I C	FRAM DRAM	MOSCALUK, GARY P., ET AL
RAM 442	FERROELECTRIC THIN FILMS AND SOLUTIONS COMPOSITIONS AND PROCESSING	09/061,362	4/15/98	R I C Mitsubish	FRAM	SUN, SHAN, ET AL
RAM 443	CMOS RC EOUIVALENT DELAY CIRCUIT	09/087,726	5/29/98	R I C	FRAM	MOSCALUK, GARY
RAM 444	FERROELECTRIC MEMORY DEVICE STRUCTURE USEFUL FOR PREVENTING HYDROGEN LINE DEGRADATION	09/177,392	10/23/98	R I C	FRAM	EVANS, THOMAS A

Ramtron No.	Patent Application	Serial No.	Filing Date	Assignee	Tech Type	Inventor	
RAM 446	HYDROGEN BARRIER ENCAPSULATION TECHNIQUES FOR THE CONTROL OF HYDROGEN INDUCED DEGRADATION OF FERROELECTRIC CAPACITORS IN CONJUNCTION WITH MULTILEVEL METAL PROCESSING FOR NON-VOLATILE INTEGRATED CIRCUIT MEMORY DEVICES	09/164,952	10/1/98	R I C	FRAM	BAILEY, RICHARD A., ET AL	10/1/99
RAM 447	EMBEDDED ENHANCED DRAM, AND ASSOCIATED METHOD	09/108,089	6/30/98	EMS	EDRAM	ALWAIS, MICHAEL, ET AL	6/30/99
RAM 448	MEMORY DEVICE HAVING MULTI-BANK SRAM REGISTERS	09/178,298	10/23/98		EDRAM	PETERS, MICHAEL	1/23/99 10/23/99

FIRST AMENDMENT TO PATENT SECURITY AGREEMENT

THIS FIRST AMENDMENT TO PATENT SECURITY AGREEMENT (this "Amendment") is dated as of January 15, 1999 by and between **RAMTRON INTERNATIONAL CORPORATION** (the "Debtor"), having a mailing address of 1850 Ramtron Drive, Colorado Springs, Colorado 80921, and **NATIONAL ELECTRICAL BENEFIT FUND**, having a mailing address of 1125 Fifteenth Street, N.W., Washington, D.C. 20005 (the "Secured Party" or "Lender").

W I T N E S S E T H

WHEREAS, in connection with that certain Loan Agreement dated as of August 31, 1995 between the Debtor and the Secured Party (as amended, the "Loan Agreement"), the Debtor executed in favor of the Secured Party that certain Patent Security Agreement dated as of August 31, 1995 (the "Patent Security Agreement"; terms being used herein shall have the meanings given them in such Patent Security Agreement);

WHEREAS, the Patent Security Agreement provides that the Debtor will, from time to time, execute such additional documents and instruments to assure the Secured Party of the full benefit intended to be created thereby; and

WHEREAS, the Secured Party has requested that Debtor execute this Amendment in order to reflect the Debtor's acquisition of rights in patents and patent applications subsequent to the execution of the Patent Security Agreement.

NOW THEREFORE, Debtor and Secured Party hereby agree as follows:

1. **Supplement to Schedule A**. In order to reflect the Debtor's acquisition of additional patents and patent applications since the date of the Patent Security Agreement, from and after the date hereof, the Schedule "A" attached thereto shall be deemed supplemented and modified by the "Schedule A Supplement" attached hereto. Each of the patents and patent applications reflected on the Schedule A Supplement shall be covered by the Patent Security Agreement and be deemed "Collateral" thereunder. For the avoidance of doubt, Debtor acknowledges that it has granted to the Secured Party a first priority security interest in and has conditionally assigned to Secured Party all of its right, title and interest in and to the patents and patent applications set forth on Schedule A to the Patent Security agreement (as supplemented as provided herein), including, without limitation, with respect to the patents and patent applications set forth on the Schedule A Supplement attached hereto.

2. **Warranties and Representation**. Debtor hereby warrants and represents to the Secured

Party the following:

(a) Schedule A to the Patent Security Agreement (as supplemented by this Amendment) is a true and complete schedule setting forth all patents and patent applications owned or controlled by Debtor, or licensed to Debtor, together with a summary description and full information in respect of the filing or issuance thereof and expiration dates therefor;

(b) To the Knowledge of Debtor, each of such patents is valid and enforceable, and Debtor is not presently aware of any past, present or prospective claim by a third party that any of the patents are invalid or unenforceable, or that the use of any patents violates the rights of any third person, or of any basis for any such claims;

(c) To the Knowledge of Debtor, Debtor is the sole and exclusive owner (or co-owner, as the case may be) of the entire and unencumbered right, title and interest in and to each of such patents and patent applications, free and clear of any liens, charges and encumbrances, including, without limitation, pledges, assignments, licenses, shop rights and covenants by Debtor not to sue third persons;

(d) Debtor has used and will continue to use its best efforts to use proper statutory notice in connection with its use of each of the patents; and

(e) Except for the filings with the United States Patent and Trademark Office necessary to perfect the security interests created hereunder with respect to those patents and patent licenses listed on the Schedule A Supplement to this Amendment, no authorization, approval or other action by, and no notice to or filing with, any governmental authority or regulatory body is required either for the grant by Debtor of the security interest hereunder or for the execution, delivery or performance of this agreement by Debtor or for the perfection of or the exercise by Secured Party of its rights hereunder to the Collateral in the United States.

It is acknowledged and agreed that it shall be an Event of Default under the Patent Security Agreement and the Loan Agreement if any representation or warranty set forth above is incorrect as of the time made.

3. **No Other Amendments**. Other than as expressly provided for herein, the Patent Security Agreement shall remain unamended and in full force and effect.

4. **Governing Law**. All acts and transactions hereunder and the rights and obligations of the parties hereto shall be governed, construed and interpreted in accordance with the laws of the State of Colorado.

5. **Counterparts**. This Amendment may be executed by the parties in counterpart, each of which shall be deemed an original, and, when taken together, one and the same document.

IN WITNESS WHEREOF, the Debtor and the Secured Party have executed this Amendment by their duly authorized officers as of the date first above written.

RAMTRON INTERNATIONAL CORPORATION

By: _____

Name: Richard L. Mohr

Title: Executive Vice President and CFO

NATIONAL ELECTRICAL BENEFIT FUND

By: _____

Edwin D. Hill, Trustee

STATE OF COLORADO)
) ss.
COUNTY OF EL PASO)

The foregoing instruments was acknowledged before me this 25 day of January 1999, by Richard L. Mohr, ~~President~~ EXECUTIVE VP & CFO of Ramtron International Corporation.

My commission expires February 7, 2002 Witness my hand and official seal.

Kathleen M. Egan
Notary Public

DISTRICT OF COLUMBIA)
) ss.
CITY OF WASHINGTON)

I, Crystal L. Davis, a Notary Public in and for the aforesaid jurisdiction, do hereby certify that Edwin D. Hill, as Trustee of the National Electrical Benefit Fund, who subscribed to the foregoing and annexed instrument dated as of January 15, 1999, is personally known to me, and appeared before me this day in person and acknowledged that he signed and delivered said instrument on behalf of the National Electrical Benefit Fund, for the purposes therein set forth.

Given under my hand and notarial seal this 4th day of February, 1999.

Crystal L. Davis
Notary Public

Crystal L Davis
Notary Public District of Columbia
My commission expires: My commission expires July 14, 2002

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SCHEDULE A SUPPLEMENT

PATENTS

RAM No.	Tech Type	Title	Patent No.	Issued	Expires	Inventor
RAM 398	FRAM	IRIDIUM OXIDE LOCAL INTERCONNECT	5,838,605	11/17/98	3/20/16	BAILEY, RICHARD A.
RAM 393	EDRAM	EDRAM WITH INTEGRATED GENERATION AND CONTROL OF WRITE ENABLE AND COLUMN LATCH SIGNALS AND METHOD OF MAKING SAME	5,835,442	11/10/98	3/22/18	JOSEPH, JAMES DEAN, ET A
RAM 371 DIV	FRAM	A VOLTAGE REFERENCE FOR A FERROELECTRIC 1T/1C BASED MEMORY	5,822,237	10/13/98	9/16/14	WILSON, DENNIS R. ET AL.
RAM 409	DRAM	SEMICONDUCTOR MEMORY DEVICE	5,818,771	10/6/98	9/30/16	YASU, YOSHIKO, ET AL.
RAM 384 DIV	FRAM	CIRCUIT AND METHOD FOR REDUCING COMPENSATION OF A FERROELECTRIC CAPACITOR BY MULTIPLE PULSING OF THE PLATE LINE FOLLOWING A WRITE OPERATION	5,815,430	9/29/98	4/10/15	VERHAEGHE, DONALD J..
RAM 412	FRAM	LOW-POWER NON-RESETABLE TEST MODE CIRCUIT	5,804,996	9/8/98	2/13/17	VERHAEGHE, DONALD J..
RAM 410	FRAM DRAM	SYSTEM AND METHOD PROVIDING SELECTIVE WRITE PROTECTION FOR INDIVIDUAL BLOCKS OF MEMORY IN A NON-VOLATILE MEMORY DEVICE	5,802,583	9/1/98	10/30/16	YEAGER, ET AL.
RAM 390	EDRAM	MULTIBUS CACHED MEMORY SYSTEM	5,802,560	9/1/98	8/30/15	JOSEPH, JAMES O., ET AL
RAM 396 DIV	FRAM	USE OF CALCIUM AND STRONTIUM DOPANTS TO IMPROVE RETENTION PERFORMANCE IN A PZT FERROELECTRIC FILM	5,800,683	9/1/98	3/15/16	KAMMERDINER, LEE, ET
RAM 385	FRAM	FABRICATION OF METAL-FERROELECTRIC-METAL CAPACITORS WITH A TWO-STEP PATTERNING SEQUENCE	5,789,323	8/4/98	4/25/15	TAYLOR, THOMAS C.
RAM 388	FRAM	BOOTSTRAPPING CIRCUIT UTILIZING A FERROELECTRIC CAPACITOR	5,774,392	6/30/98	3/28/16	KRAUS, WILLIAM F, ET A
RAM 403	FRAM	SYSTEM AND METHOD FOR MITIGATING IMPRINT EFFECT IN FERRDELECTRIC RANDOM ACCESS MEMORIES UTILIZING A COMPLEMENTARY DATA PATH	5,745,403	4/28/98	2/28/17	TAYLOR, CRAIG
RAM 343 CON	EDRAM	ENHANCED DRAM WITH EMBEDDED REGISTERS	5,721,862	2/24/98	2/24/15	SARTORE, RONALD H..
RAM 343 CIP	EDRAM	ENHANCED DRAM WITH EMBEDDED REGISTERS	5,699,317	12/16/97	1/22/12	SARTORE, RONALD H..
RAM 404	FRAM	SAME STATE AND OPPOSITE STATE DIAGNOSTIC TEST FOR FERRDELECTRIC MEMORIES	5,661,730	8/26/97	9/27/16	MITRA, SANJAY, ET AL.
RAM 321	DRAM	PROCESS FOR FABRICATING TRANSISTORS USING COMPOSITE NITRIDE STRUCTURE	5,610,099	3/11/97	6/28/14	LARSON, WILLIAM L.
RAM 368 FWC	FRAM RFID	INTEGRATION OF HIGH VALUE CAPACITOR WITH FERROELECTRIC MEMORY	5,608,246	3/4/97	3/4/14	YEAGER, MICHAEL W..
RAM 367	FRAM	FERROELECTRIC NONVOLATILE RANDOM ACCESS MEMORY UTILIZING SELF-BOOTSTRAPPING PLATE LINE SEGMENT DRIVERS	5,598,366	1/28/97	8/16/15	KRAUS, WILLIAM F., ET
RAM 384	FRAM	CIRCUIT AND METHOD FOR REDUCING COMPENSATION OF A FERROELECTRIC CAPACITOR BY MULTIPLE PULSING OF THE PLATE LINE FOLLOWING A WRITE OPERATION	5,592,410	1/7/97	4/10/15	VERHAEGHE, DONALD
RAM 332 DIV	FRAM	STACKED FERROELECTRIC MEMORY CELL AND METHOD	5,580,814	12/3/96	5/29/11	LARSON, WILLIAM L.
RAM 379 DIV	FRAM	PASSIVATION METHOD AND STRUCTURE USING HARD CERAMIC MATERIALS OR THE LIKE	5,578,867	11/26/96	3/11/14	ARGOS, GEORGE, ET

RAM No.	Tech Type	Title	Patent No.	Issued	Expires	Inventor
RAM 371	FRAM	VOLTAGE REFERENCE FOR A FERROELECTRIC 1T/1C BASED MEMORY	5,572,459	11/5/96	9/16/14	WILSON, DENNIS R., ET AL.
RAM 381	EDRAM	CIRCUIT WITH A SINGLE ADDRESS REGISTER THAT AUGMENTS A MEMORY CONTROLLER BY ENABLING CACHE READS AND PAGE-MODE WRITES	5,566,318	10/15/96	3/2/14	JOSEPH, JAMES D.
RAM 382	FRAM	FERROELECTRIC MEMORY SENSING METHOD USING DISTINCT READ AND WRITE VOLTAGES	5,532,953	7/2/96	3/29/15	RUESCH, RODNEY A., ET A
RAM 370	FRAM	FERROELECTRIC MEMORY SENSING SCHEME USING BIT LINES PRECHARGED TO A LOGIC ONE VOLTAGE	5,530,668	6/25/96	4/12/15	CHERN, WEN-FOO, ET AL.
RAM 374	FRAM	FERROELECTRIC CAPACITOR RENEWAL METHOD	5,525,528	6/11/96	5/6/14	PERINO, STANLEY, ET AL.
RAM 352 FWC	FRAM	SEMICONDUCTOR DEVICE HAVING A TRANSISTOR, A FERROELECTRIC CAPACITOR AND A HYDROGEN BARRIER FILM	5,523,595	6/4/96	5/4/13	TAKENAKA, KAZUHIRO, E
RAM 377 CON	FRAM	FILM HAVING FERROELECTRIC BISMUTH LAYERED OXIDES	5,519,566	5/21/96	5/15/14	PERINO, STANLEY C., ET
RAM 378	FRAM	LAYERED LOCAL INTERCONNECT COMPATIBLE WITH INTEGRATED CIRCUIT FERROELECTRIC CAPACITORS	5,496,569	3/12/96	8/22/14	EASTEP, BRIAN
RAM 332 FWC2	FRAM	STACKED FERROELECTRIC MEMORY CELL AND METHOD	5,495,117	2/27/96	2/27/13	LARSON, WILLIAM L.
RAM 376	FRAM	NOISE AND GLITCH SUPPRESSING FILTER WITH FEEDBACK	5,479,132	12/26/95	6/6/14	VERHAEGHE, DONALD, I
RAM 358 FWC2	FRAM	SEMICONDUCTOR DEVICE WITH A CONDUCTIVE REACTION-PREVENTING FILM	5,475,248	12/12/95	12/12/12	TANENAKA, K.

PATENT APPLICATIONS

Ramtron No.	Patent Application	Serial No.	Filing Date	Assignee	Tech Type	Inventor
RAM 343 DIV	ENHANCED DRAM WITH EMBEDDED REGISTERS	08/888,371	7/3/97	EMS	EDRAM	SARTORE, RONALD H., ET AL
RAM 343 DIV/CD	ENHANCED DRAM WITH EMBEDDED REGISTERS	09/182,994	10/30/98	EMS	EDRAM	SARTORE, RONALD H., ET AL
RAM 368 DIV	INTEGRATION OF HIGH VALUE CAPACITOR	08/544,470	10/18/95	RIC	FRAM RFID	YEAGER, MICHAEL W., ET AL
RAM 389	COMPUTER HYBRID MEMORY INCLUDING DRAM AND EDRAM MEMORY COMPONENTS, WITH SECONDARY CACHE IN EDRAM FOR DRAM	08/615,392	3/14/96	EMS	EDRAM	JOSEPH, JAMES DEAN
RAM 391	PROGRAMMABLE OUTPUT DEVICES FOR CONTROLLING SIGNAL LEVELS IN AN RF/ID TRANSPONDER	08/521,251	8/30/95	RIC	RFID	DOWNS, JEFFREY E., ET AL
RAM 392 DIV	METHOD OF MANUFACTURING IRIDIUM ELECTRODE FOR STRONTIUM BISMUTH TANTALATE FERROELECTRIC CAPACITORS	08/896,329	7/17/97	RIC	FRAM	PERINO, STANLEY, ET AL

Ramtron No.	Patent Application	Serial No.	Filing Date	Assignee	Tech Type	Inventor
RAM 394	DYNAMIC CACHE SIZING MEMORY	08/630,489	4/10/96	EMS	EDRAM	HEISLER, DOYLE JAMES, ET AL
RAM 396	THE USE OF CALCIUM AND STRONTIUM DOPANTS TO IMPROVE RETENTION PERFORMANCE IN A PZT FERROELECTRIC FILM	08/616,856	3/15/96	RIC	FRAM	KAMMERDINER, LEE ET AL
RAM 397	A METHOD OF MEASURING RETENTION PERFORMANCE AND IMPRINT DEGRADATION OF FERROELECTRIC FILMS	08/616,913	3/15/96	RIC	FRAM	TRAYNOR, STEVEN
RAM 398 DIV	IRIDIUM OXIDE LOCAL INTERCONNECT	09/183,545	10/29/98	RIC	FRAM	BAILEY, RICHARD A
RAM 399	YIELD ENHANCEMENT TECHNIQUE FOR INTEGRATED CIRCUIT PROCESSING TO REDUCE EFFECTS OF UNDESIRED DIELECTRIC MOISTURE RETENTION AND SUBSEQUENT HYDROGEN OUT-DIFFUSION	08/728,256	10/8/96	RIC	FRAM	ARGOS, GEORGE JR., ET AL
RAM 400	LOW VOLTAGE BOOTSTRAPPING CIRCUIT	08/663,032	6/7/96	RIC	FRAM DRAM	VERHAEGHE, DONALD J., ET AL
RAM 402	SERIAL FRAM ARCHITECTURE TO EQUALIZE COLUMN ACCESS	08/810,607	2/28/97	RIC	FRAM	TAYLOR, CRAIG

Ramtron No.	Patent Application	Serial No.	Filing Date	Assignee	Tech Type	Inventor
RAM 405	BANDGAP REFERENCE BASED POWER-ON DETECT CIRCUIT INCLUDING A SUPPRESSION CIRCUIT	08/702 363	8/23/96	R I C	FRAM	KRAUS WILLIAM F
RAM 405 CON	BANDGAP REFERENCED BASED POWER-ON DETECT CIRCUIT	09/017 577	2/3/98	RIC	FRAM	KRAUSE WILLIAM F
RAM 406	DATA PROCESSOR INCORPORATING A FERROELECTRIC MEMORY ARRAY SELECTABLY CONFIGURABLE AS READ/WRITE AND READ ONLY MEMORY	08/734 802	10/21/96	R I C	FRAM	DOWNS JEFFERY E
RAM 407	PARTIALLY OR COMPLETELY ENCAPSULATEO TOP ELECTRODE OF A FERROELECTRIC CAPACITOR	08/700 076	8/20/96	R I C	FRAM	EVANS, THOMAS A , ET AL
RAM 407 CIP	PARTIALLY OR COMPLETELY ENCAPSULATED TOP ELECTRODE OF A FERROELECTRIC CAPACITOR	08/728 740	10/11/96	R I C	FRAM	EVANS, THOMAS A , ET AL
RAM 407 CIP2	PARTIALLY OR COMPLETELY ENCAPSULATEO TOP ELECTRODE OF FERROELECTRIC CAPACITOR	08/828,157	3/27/97	R I C	FRAM	EVANS, THOMAS A , ET AL
RAM 407 CIP3	COMPLETELY ENCAPSULATED TOP ELECTRODE OF A FERROELECTRIC CAPACITOR USING A LEAD-ENHANCED ENCAPSULATION LAYER	09/085,280	5/27/98	R I C	FRAM	EASTEP, BRIAN, ET AL

Ramtron No.	Patent Application	Serial No.	Filing Date	Assignee	Tech Type	Inventor
RAM 413	SYSTEM AND METHOD FOR CONTROLLING INTERNAL TEST MODES IN A NON-VOLATILE MEMORY THROUGH NORMAL ACCESSES	08/802,630	2/19/97	R I C Hitachi	FRAM	VERHAEGHE, DONALD J., ET AL
RAM 414	SENSING METHODOLOGY FOR A 1T/1C FERROELECTRIC MEMORY	08/970,453	11/14/97	R I C	FRAM	WILSON, D., ET AL
RAM 415	DUAL-LEVEL METALIZATION METHOD FOR INTEGRATED CIRCUIT FERROELECTRIC DEVICES	08/853,527	5/9/97	R I C Fujitsu	FRAM	ARGOS, GEORGE, ET AL
RAM 417	ENHANCED SIGNAL PROCESSING RANDOM ACCESS MEMORY DEVICE UTILIZING A DRAM MEMORY ARRAY INTEGRATED WITH AN ASSOCIATED SRAM CACHE AND INTERNAL REFRESH CONTROL	08/850,802	5/2/97	EMS	EDRAM	ALWAIS, MICHAEL, ET AL
RAM 418	FIRST-IN, FIRST-OUT INTEGRATED CIRCUIT MEMORY DEVICE UTILIZING A DYNAMIC RANDOM ACCESS MEMORY ARRAY FOR DATA STORAGE IMPLEMENTED IN CONJUNCTION WITH AN ASSOCIATED STATIC RANDOM ACCESS MEMORY CACHE	08/840,118	4/1/97	EMS	EDRAM DRAM	TAYLOR, CRAIG
RAM 420	SYNCHRONOUS DYNAMIC RANDOM ACCESS MEMORY DEVICE INCORPORATING A STATIC RAM CACHE	09/023,656	2/9/98	EMS	EDRAM	MOBLEY, KENNETH J., ET AL

Ramtron No.	Patent Application	Serial No.	Filing Date	Assignee	Tech Type	Inventor
RAM 421	MULTI-LAYER APPROACH FOR OPTIMIZING FERROELECTRIC FILM PERFORMANCE	08/896,684	7/18/97 RIC	FRAM	EASTEP, BRIAN LEE	
RAM 421 CIP	MULTI-LAYER APPROACH FOR OPTIMIZING FERROELECTRIC FILM PERFORMANCE	09/064,465	4/22/98 R I C	FRAM	EASTEP BRIAN L	
RAM 422	INTEGRATED CIRCUIT MEMORY DEVICE INCORPORATING A NON-VOLATILE MEMORY ARRAY AND A RELATIVELY FASTER ACCESS TIME MEMORY CACHE	09/021,132	2/10/98 RIC	EDRAM, FRAM	TAYLOR CRAIG, ET AL	
RAM 424	VOLTAGE BOOST CIRCUIT AND OPERATION THEREOF AT LOW POWER SUPPLY VOLTAGES	08/915,054	8/20/97 R I C	FRAM	MOSCALUK, GARY P	
RAM 425	PLASTIC PACKAGE ASSEMBLY METHOD FOR A FERROELECTRIC-BASED INTEGRATED CIRCUIT	09/090,575	6/4/98 R I C	FRAM	SANJAY MITRA, ET AL	
RAM 427	SENSE AMPLIFIER UTILIZING A BALANCING RESISTOR	09/022,106	2/11/98 RIC	FRAM	KRAUS, WILLIAM F	
RAM 429	TECHNIQUE FOR REDUCING ELEMENT DISABLE FUSE PITCH REQUIREMENTS IN AN INTEGRATED CIRCUIT DEVICE INCORPORATING REPLACEABLE CIRCUIT ELEMENTS	09/069,468	4/29/98 EMS	EDRAM	MOBLEY, KENNETH J., ET AL.	

Ramtron No.	Patent Application	Serial No.	Filing Date	Assignee	Tech Type	Inventor
RAM 430	DYNAMIC RANDOM ACCESS MEMORY WORD LINE BOOST TECHNIQUE EMPLOYING A BOOST-ON-WRITES POLICY	09/146,726	9/3/98	EMS	EDRAM	MOBLEY, KENNETH J
RAM 431	MEMORY DEVICE, AND ASSOCIATED METHOD, HAVING DEDICATED BURST ADDRESS BUS	09/112,223	7/8/98	EMS	EDRAM	MOBLEY, KENNETH J
RAM 432	BLOCK-TO-BLOCK SHARING OF WRITE DECODER	09/111,822	7/8/98	EMS	EDRAM	MOBLEY, KENNETH J
RAM 433	REFERENCE CELL FOR A 1T/1C FERROELECTRIC MEMORY	08/970,452	11/14/97	R I C	FRAM	WILSON, D., ET AL
RAM 434	MEMORY CELL CONFIGURATION FOR A 1T/1C FERROELECTRIC MEMORY	08/970,520	11/14/97	R I C	FRAM	ALLEN, J., ET AL
RAM 435	REFERENCE CELL CONFIGURATION FOR A 1T/1C FERROELECTRIC MEMORY	08/970,518	11/14/97	R I C	FRAM	ALLEN, J., ET AL
RAM 436	SENSE AMPLIFIER CONFIGURATION FOR A 1T/1C FERROELECTRIC MEMORY	08/970,519	11/14/97	R I C	FRAM	ALLEN, J., ET AL
RAM 437	COLUMN DECODER CONFIGURATION FOR A 1T/1C FERROELECTRIC MEMORY	08/970,454	11/14/97	R I C	FRAM	ALLEN, J., ET AL

Ramtron No.	Patent Application	Serial No.	Filing Date	Assignee	Tech Type	Inventor
RAM 438	SENSE AMPLIFIER LATCH DRIVER CIRCUIT FOR A IT/1C FERROELECTRIC MEMORY	08/970,521	11/14/97	R I C	FRAM	WILSON D
RAM 439	PLATE LINE DRIVER CIRCUIT FOR A IT/1C FERROELECTRIC MEMORY	08/970,522	11/14/97	R I C	FRAM	KRAUS W ET AL
RAM 440	PLATE LINE SEGMENTATION IN A IT/1C FERROELECTRIC MEMORY	08/970,448	11/14/97	R I C	FRAM	KRAUS W ET AL
RAM 441	"WINDOW OF UNCERTAINTY" MINIMIZER FOR A MULTIPLE-INPUT LOGIC CIRCUIT	09/027,881	2/23/98	R I C	FRAM ORAM	MOSCALUK GARY P. ET AL
RAM 442	FERROELECTRIC THIN FILMS AND SOLUTIONS COMPOSITIONS AND PROCESSING	09/061,362	4/15/98	R I C Mitsubishi	FRAM	SUN, SHAN, ET AL
RAM 443	CMOS RC EQUIVALENT DELAY CIRCUIT	09/087,726	5/29/98	R I C	FRAM	MOSCALUK, GARY
RAM 444	FERROELECTRIC MEMORY DEVICE STRUCTURE USEFUL FOR PREVENTING HYDROGEN LINE DEGRADATION	09/177,392	10/23/98	R I C	FRAM	EVANS, THOMAS A

Ramtron No.	Patent Application	Serial No.	Filing Date	Assignee	Tech Type	Inventor	
RAM 446	HYDROGEN BARRIER ENCAPSULATION TECHNIQUES FOR THE CONTROL OF HYDROGEN INDUCED DEGRADATION OF FERROELECTRIC CAPACITORS IN CONJUNCTION WITH MULTILEVEL METAL PROCESSING FOR NON-VOLATILE INTEGRATED CIRCUIT MEMORY DEVICES	09/164,952	10/1/98	R I C	FRAM	BAILEY, RICHARD A., ET AL	10/1/99
RAM 447	EMBEDDED ENHANCED DRAM, AND ASSOCIATED METHOD	09/108,089	6/30/98	EMS	EDRAM	ALWAIS, MICHAEL ET AL	6/30/99
RAM 448	MEMORY DEVICE HAVING MULTI-BANK SRAM REGISTERS	09/178,298	10/23/98		EDRAM	PETERS, MICHAEL	1/23/99 10/23/99