PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	RELEASE BY SECURED PARTY

CONVEYING PARTY DATA

Name	Execution Date
Morgan Stanley & Co. Incorporated, as Facility Collateral Agent	02/13/2004

RECEIVING PARTY DATA

Name:	Legerity, Inc.
Street Address:	Bldg. 3, M/S 310
Internal Address:	4509 Freidrich Lane
City:	Austin
State/Country:	TEXAS
Postal Code:	78744

Name:	Legerity Holdings, Inc.
Street Address:	Bldg. 3, M/S 310
Internal Address:	4509 Freidrich Lane
City:	Austin
State/Country:	TEXAS
Postal Code:	78744

Name:	Legerity International, Inc.
Street Address:	Bldg. 3, M/S 310
Internal Address:	4509 Freidrich Lane
City:	Austin
State/Country:	TEXAS
Postal Code:	78744

OP $1320.00 5247626

PROPERTY NUMBERS Total: 33

Property Type	Number
Patent Number:	5247626
Patent Number:	5305321

Patent Number:	5627536
Patent Number:	5633888
Patent Number:	5646621
Patent Number:	5675808
Patent Number:	5721945
Patent Number:	5892934
Patent Number:	5740420
Patent Number:	5754878
Patent Number:	5768553
Patent Number:	5768613
Patent Number:	5781792
Patent Number:	5784640
Patent Number:	5790824
Patent Number:	5802463
Patent Number:	5918073
Patent Number:	5937374
Patent Number:	6026130
Patent Number:	6032247
Patent Number:	6035434
Patent Number:	6061410
Patent Number:	6067515
Patent Number:	6085314
Patent Number:	6128307
Patent Number:	6151366
Patent Number:	6246754
Patent Number:	6263311
Patent Number:	6272465
Patent Number:	6320943
Patent Number:	6356765
Patent Number:	6377666
Patent Number:	5442354

CORRESPONDENCE DATA

Fax Number: (801)328-1707

Correspondence will be sent via US Mail when the fax attempt is unsuccessful.

Phone:	8015339800
Email:	bgonzalez@wnlaw.com
Correspondent Name:	ERIC L. MASCHOFF / Workman Nydegger
Address Line 1:	60 East South Temple
Address Line 2:	1000 Eagle Gate Tower
Address Line 4:	Salt Lake City, UTAH 84111

ATTORNEY DOCKET NUMBER:	17286.0
NAME OF SUBMITTER:	ERIC L. MASCHOFF

Total Attachments: 4
source=release secy interest #1#page1.tif
source=release secy interest #1#page2.tif
source=release secy interest #1#page3.tif
source=release secy interest #1#page4.tif

RELEASE OF LIEN ON PATENTS

WHEREAS, by a certain Intellectual Property Security Agreement dated as of September 30, 2002 (the "**Agreement**") by Legerity, Inc., a Delaware corporation, Legerity Holdings, Inc., a Delaware corporation, and the Legerity International, Inc., a Delaware corporation (together, the "**Assignors**"), in favor of Morgan Stanley & Co. Incorporated, as Facility Collateral Agent (the "**Assignee**"), which Agreement was recorded with the United States Patent and Trademark Office on October 21, 2002 on reel 013372 frame 63, Assignors granted to Assignee a security interest in and lien on those patents and patent applications owned by Assignors and set forth on Schedule A hereto;

WHEREAS, Assignee desires to release its security interest in and lien on the patents and patent applications set forth on Schedule A hereto;

NOW, THEREFORE, Assignee does hereby release its security interest in and lien on patents and patent applications set forth on Schedule A hereto.

Dated: February 13, 2004

MORGAN STANLEY & CO. INCORPORATED,
as Facility Collateral Agent

By: _____
Name: DEBORAH DESANTIS
Title: **AUTHORIZED SIGNATORY**

Schedule A

Patent No.	Inventor(s)	Title	Patent Date
5,247,626	Farzin Firoozmand	FDDI controller having flexible buffer management	Sep. 21, 1993
5,305,321	Ian Crayford	Ethernet media access controller with external address detection interface and associated method	Apr. 19, 1994
5,627,536	Sergio R. Ramirez	Multiplexed delta-sigma modulator	May. 06, 1997
5,633,888	Brett B. Stewart	Method of using an access point adjacency matrix to establish handoff in a wireless LAN	May. 27, 1997
5,646,621	Carlin Dru Cabler; Alfredo R. Linz	Delta-sigma ADC with multi-stage decimation filter and gain compensation filter	Jul. 08, 1997
5,675,808	Dele E. Gulick; Larry D. Hewitt; Michael Hogan; David Norris	Power control of circuit modules within an integrated circuit	Oct. 07, 1997
5,721,945	Andrew Mills; Mark A. Ireton; Thomas W. Lynch	Microprocessor configured to detect a DSP call instruction and to direct a DSP to execute a routine corresponding to the DSP call instruction	Feb. 24, 1998
5,892,934	Christopher J. Yard	Microprocessor configured to detect a branch to a DSP routine and to direct a DSP to execute said routine	Apr. 06, 1999
5,740,420	Krishnan Palaniswami	System and method for compiling and executing sequences of macro and micro instructions	Apr. 14, 1998
5,754,878	Saf Asghar; Mark Ireton; John G. Bartkowiak	CPU with DSP function preprocessor having pattern recognition detector that uses table for translating instruction sequences intended to perform DSP function into DSP macros	May. 19, 1998
5,768,553	Thang M. Tran	Microprocessor using an instruction field to define DSP instructions	Jun. 16, 1998
5,768,613	Safdar M. Asghar	Computing apparatus configured for partitioned processing	Jun. 16, 1998
5,781,792	Saf Asghar; Mark Ireton; John Bartkowiak	CPU with DSP having decoder that detects and converts instruction sequences intended to perform DSP function into DSP function identifier	Jul. 14, 1998
5,784,640	Saf Asghar; Mark Ireton; John G. Bartkowiak	CPU with DSP function preprocessor having look-up table for translating instruction sequences intended to perform DSP function into DSP macros	Jul. 21, 1998
5,790,824	Saf Asghar; Mark Ireton; John Bartkowiak	Central processing unit including a DSP function preprocessor which scans instruction sequences for DSP functions	Aug. 04, 1998

Patent No.	Inventor(s)	Title	Patent Date
5,802,463	Lawrence H. Zuckerman	Apparatus and method for receiving a modulated radio frequency signal by converting the radio frequency signal to a very low intermediate frequency signal	Sep. 01, 1998
5,918,073	Larry D. Hewitt	System and method for equalizing data buffer storage and fetch rates of peripheral devices	Jun. 29, 1999
5,937,374	John G. Bartkowiak; Mark A. Ireton	System and method for improved pitch estimation which performs first formant energy removal for a frame using coefficients from a prior frame	Aug. 10, 1999
6,026,130	Muhammad M. Rahmatullah; Philip Yip; Saf Asghar	System and method for estimating a set of parameters for a transmission channel in a communication system	Feb. 15, 2000
6,032,247	Saf Asghar; Andrew Mills	Central processing unit including APX and DSP cores which receives and processes APX and DSP instructions	Feb. 29, 2000
6,035,434	Sharif M. Sazzad; Jagannathan Bharath	System and method for bit interleaving of half-rate speech data	Mar. 07, 2000
6,061,410	Alfredo R. Linz	Frequency ratio estimation arrangement and method thereof	May. 09, 2000
6,067,515	Lin Cong; Safdar M. Asghar	Split matrix quantization with split vector quantization error compensation and selective enhanced processing for robust speech recognition	May. 23, 2000
6,085,314	Saf Asghar; Andrew Mills	Central processing unit including APX and DSP cores and including selectable APX and DSP execution modes	Jul. 04, 2000
6,128,307	Glen W. Brown	Programmable data flow processor for performing data transfers	Oct. 03, 2000
6,151,366	Philip Chu Wah Yip	Method and apparatus for modulating signals	Nov. 21, 2000
6,246,754	Terry Lynn Cole; Charles Ray Boswell, Jr.	Mechanism for changing a modem's connection rate within a family of interoperable modems	Jun. 12, 2001
6,263,311	Robert Dildy	Method and system for providing security using voice recognition	Jul. 17, 2001
6,272,465	Larry D. Hewitt; Jeffrey M. Blumenthal; Geoffrey E. Brehmer; Glen W. Brown; Carlin Dru Cabler; Ryan Feemster; David Guercio; Dale E. Gulick; Michael Hogan; Alfredo R. Linz; David Norris; Paul G. Schnizlein; Martin P. Soques; Michael E. Spak; David N. Suggs; Alan T. Torok	Monolithic PC audio circuit	Aug. 07, 2001

Patent No.	Inventor(s)	Title	Patent Date
6,320,943	David James Borland	Electronic directory system and method	Nov. 20, 2001
6,356,765	Christopher L. McCrank; Javier V. Magana	Method and apparatus for tracking signals	Mar. 12, 2002
6,377,666	Yi Cheng; Zhenhua Liu	Apparatus and method for a PHY transmitter with programmable power mode control in CMOS	Apr. 23, 2002
5,442,354	Carlin D. Cabler	Fourth-order cascaded sigma-delta modulator	Aug. 15, 1995