PATENT ASSIGNMENT

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Hewlett-Packard Development Company, L.P.	06/25/2010
Hewlett-Packard Company	06/25/2010

RECEIVING PARTY DATA

Name:	Samsung Electronics Co., Ltd.
Street Address:	416 Maetan-dong, Yeongtong-gu
Internal Address:	Suwon-si
City:	Gyeonggi-do
State/Country:	REPUBLIC OF KOREA

PROPERTY NUMBERS Total: 2

Property Type	Number
Application Number:	11146790
Application Number:	11540480

CH $80.00 11146790

CORRESPONDENCE DATA

Fax Number: (919)854-1401
Correspondence will be sent via US Mail when the fax attempt is unsuccessful.
Phone: 919-854-1400
Email: kcarlos@myersbigel.com
Correspondent Name: Myers Bigel Sibley & Sajovec, P.A./ksc
Address Line 1: 4140 Parklake Avenue
Address Line 2: Suite 600
Address Line 4: Raleigh, NORTH CAROLINA 27612

ATTORNEY DOCKET NUMBER:	5649-3123
NAME OF SUBMITTER:	Kirsten S. Carlos

Total Attachments: 11
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Exhibit B

ASSIGNMENT OF PATENTS AND PATENT APPLICATIONS

WHEREAS, Hewlett-Packard Development Company, L.P., a limited partnership established and existing under the laws of the State of Texas and having its registered place of business at 20555 S.H. 249 Houston, Texas 77070, U.S.A. and Hewlett-Packard Company, a corporation organized and existing under the laws of the State of Delaware and having its principal place of business at 3000 Hanover Street, Palo Alto, California 94304, U.S.A. (collectively "HP") are the owners of record, either individually or collectively, of the Assigned Patents (as defined below);

WHEREAS, Samsung Electronics Co., Ltd. ("Samsung"), a corporation duly organized and existing under and by virtue of the laws of the Republic of Korea, and having a place of business at 416 Maetan-dong, Yeongtong-gu, Suwon-si, Gyeonggi-do, Republic of Korea, is desirous of acquiring the entire interest in and to the Assigned Patents (as defined below);

WHEREAS, HP and Samsung have entered into a Patent Purchase and Sale Agreement for certain patents and patent applications dated June 25, 2010 ("Purchase and Sale Agreement") wherein HP has agreed to sell and Samsung has agreed to purchase the Assigned Patents subject to all prior encumbrances and licenses;

WHEREAS, Samsung has agreed and covenanted in said Purchase and Sale Agreement to license back to HP certain rights under the Assigned Patents as a condition of and as part of the consideration for the Parties entering into the Purchase and Sale Agreement;

WHEREAS, for the purpose of this Assignment, the following terms, whether in singular or in plural form, when used with a capital initial letter shall have the respective meanings as follows.

"**Affiliate**" means with respect to any person, any other Person that directly, or indirectly through one or more intermediaries, controls, is controlled by, or is under the common control of the Person in question; provided, however, that in any country where the local law or regulation does not permit foreign equity participation of more than fifty percent (50%), an "Affiliate" shall include any Person in which the Person in question owns or controls, directly or indirectly, the maximum percentage of such outstanding stock or voting rights permitted by such local law or regulation. For purposes of the foregoing, "control," including the terms "controlling," "controlled by" and "under common control with," means the possession, direct or indirect, of the power to direct or cause the direction of the management and policies of a Person, whether through the ownership of voting securities, by contract or otherwise.

"**Assigned Patents**" means the issued patents and patent applications listed in Appendix A of this Assignment. SamsungSemi acknowledges that, as of the Effective Date of the Purchase and Sale Agreement, HP has not completed due diligence on the foreign-filed

patents and patent applications listed under the heading 'Foreign Patents and Applications Pending Diligence Review' in Appendix A (collectively "Unconfirmed Foreign Patents") and accordingly, has not confirmed that such Unconfirmed Foreign Patents are available for sale or, similarly, are Assigned Patents. Each patent or patent application for which it is determined that the patent or patent application has not been abandoned, HP is the legal and beneficial owner of and to which HP has good marketable title free from liens and which HP has the authority and capacity to transfer HP's entire legal and beneficial title to SamsungSemi will be included as an Assigned Patent. HP will complete the due diligence on the Unconfirmed Foreign Patents on or before July 20, 2010 and, upon completion of such diligence, HP will provide SamsungSemi a final list by email addressed to Dr. Won Deuk Song at wdsong@samsung.com of all Unconfirmed Foreign Patents confirmed as Assigned Patents. The Parties acknowledge that the Purchase Price shall not be affected by the final determination of whether any of such Unconfirmed Foreign Patents is or is not an Assigned Patent.

"**Encumbrances**" means any commitments, licenses or other rights relating to any of the Assigned Patents, whether express, implied or otherwise, that are made, entered into or granted by, or that arise from the actions taken by, HP, any current or former Affiliate of HP, or any Person, prior to the Effective Date including, but not limited to, the commitments, licenses and rights described in Sections 5 and 6.1 of the Purchase and Sale Agreement.

"**Person**" means any natural person, corporation, company, partnership, association, sole proprietorship, trust, joint venture, non-profit entity, institute, governmental authority, trust association or other form of entity not specifically listed herein including, without limitation, HP or any of its Affiliates, or Samsung or any of its Affiliates.

NOW, THEREFORE, to all whom it may concern, be it known that for good and valuable consideration to HP in hand paid, the receipt of which is hereby acknowledged, HP has sold, assigned, transferred, and set over, and by these presents does sell, assign, transfer, and set over unto said Samsung, subject to all Encumbrances, its whole right, title, and interest in and to all of the Assigned Patents, said whole right, title, and interest in and to said Assigned Patents including all past, present, and future causes of action and claims for damages derived by reason of patent infringement thereof (to the extent such damages are not already paid, awarded or contractually owed to HP, its Affiliates or any predecessor of HP or HP's Affiliates), for said Samsung's own use and for the use of its assigns, successors, and legal representatives to the full end of the term of each of the Assigned Patents. For clarity, the foregoing assignment does not include (i) any trademarks, trade dress, trade names, or other indicia of origin; (ii) except for inventions of the Assigned Patents, any inventions or discoveries, whether patentable or not, and registrations, invention disclosures, patents and applications therefor; (iii) any trade secrets, confidential information or know-how; (iv) any works of authorship, whether copyrightable or not; and (v) any other intellectual property or proprietary rights of HP, its Affiliates or any predecessor of HP or HP's Affiliates.

HP, for itself, and its heirs, assigns, and legal representatives hereby further covenants to

and with Samsung, its assigns, successors, and legal representatives to fully cooperate therewith in perfecting this assignment in the United States and in any and all foreign jurisdictions, said cooperation extending to the Assigned Patents, and including the execution of additional assignments or other formal documents as may be required in connection therewith.

In Testimony Whereof, HP by its fully authorized representatives has executed this Assignment as of the dates indicated below.

HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.

By: HPQ Holdings, LLC, its General Partner

By: _____ Date: June 25, 2010

Kevin P. Light, Manager
HPQ Holdings, LLC

HEWLETT-PACKARD COMPANY

By: _____ Date: 6/25/10

Bruce H. Watrous, Jr.
VP & AGC, Intellectual Property Licensing
Hewlett-Packard Company

(Execution Copy June 25, 2010)

Appendix A of Exhibit B: List of Assigned Patents

CN	GRANTED	1121893	Collapsible Hub Assembly
CN	GRANTED	200410044759.6	Systems And Methods For Storing Data On Computer Systems
CN	GRANTED	ZL01124741.X	AFM Version Of Diode- And Cathodoconductivity-and Cathodoluminescence-Based Data Storage Media
CN	GRANTED	ZL01139500.1	Electron Source Having Planar Emission Region And Focusing Structure
CN	GRANTED	ZL02120303.2	Device Isolation Process Flow For ARS System
CN	GRANTED	ZL02126529.1	A Circuit And A Method For Writing A Memory Cell (as Amended)
CN	GRANTED	ZL02126953.X	A Method Of Fabricating A Solid State Memory Device (as Amended)
CN	GRANTED	ZL02127285.9	Write Pulse Limiting For Worm Storage Device
DE	GRANTED	1093562	An Architectural Mechanism For Fast Evaluation Of Boolean Reductions
DE	GRANTED	1167266	Collapsible Hub Assembly
DE	GRANTED	1278203	Pulse Train Writing Of Worm Storage Device
DE	GRANTED	1286357	Thin Film Transistor Memory Device
DE	GRANTED	1303044	DIODE-BASED MULTIPLEXER
DE	GRANTED	1388048	Storage System For Use In Custom Loop Accelerators And The Like
DE	GRANTED	1398781	Luminescence-based Data Storage
EP	NATIONAL	0379768	Read-modify-write operation
EP	NATIONAL	0399761	Sequential parity correction
EP	NATIONAL	0407053	Small, fast, look-aside data cache memory
EP	NATIONAL	461923	True least recently used replacement method and apparatus
EP	NATIONAL	461924	Memory address space determination using programmable limit registers with single-ended comparators
EP	NATIONAL	0528538	Mirrored memory multi processor system
EP	NATIONAL	0565855	Data integrity assurance in a disk drive upon a power failure
EP	NATIONAL	0617367	System management interrupt address bit correction circuit
EP	NATIONAL	0621539	Burst SRAMs for use with a high speed clock
EP	NATIONAL	0649140	Electrical interconnect for a head/arm assembly of computer disk drives
EP	NATIONAL	0760501	Data handling system with circular queue formed in paged memory
EP	NATIONAL	0851425	Method and apparatus for using EDO memory devices in a memory syste designed for FPM memory devices
EP	NATIONAL	1167266	Collapsible hub assembly
EP	NATIONAL	1241580	Memory manager for a common memory
EP	NATIONAL	1278203	Method and apparatus for writing a memory device
EP	NATIONAL	1282136	Method and apparatus for writing memory cells
EP	NATIONAL	1286357	Thin film transistor memory device
EP	NATIONAL	1303044	Diode-based multiplexer
EP	NATIONAL	1388048	STORAGE SYSTEM FOR USE IN CUSTOM LOOP ACCELLERATORS AND THE LIKE
EP	NATIONAL	1398781	Luminescence-based data storage
EP	PENDING	1769500	SEMICONDUCTOR STORAGE DEVICE
EP	NATIONAL	69433155.4	Programmable error-checking matrix for digital communication system
FR	GRANTED	461923	TRUE SIX-BIT LEAST RECENTLY USED (LRU) AL- GORITHM

FR	GRANTED	1278203	Pulse Train Writing Of Worm Storage Device
FR	GRANTED	1286357	Thin Film Transistor Memory Device
FR	GRANTED	1398781	Luminescence-based Data Storage
GB	GRANTED	461924	MEMORY ADDRESS SPACE DETERMINATION USING PROGRAMMABLE LIMIT REGISTERS WITH SINGLE- ENDED COMPARATORS
GB	GRANTED	1093562	Computer System And Method For Evaluating Predicates And Boolean Expressions
GB	GRANTED	1167266	Collapsible Hub Assembly
GB	GRANTED	1278203	Pulse Train Writing Of Worm Storage Device
GB	GRANTED	1282136	Write Pulse Limiting For Worm Storage Device
GB	GRANTED	1286357	Thin Film Transistor Memory Device
GB	GRANTED	1303044	DIODE-BASED MULTIPLEXER
GB	GRANTED	1398781	Luminescence-based Data Storage
GB	GRANTED	2411802	System For Error Correction Coding And Decoding
GB	GRANTED	10990959	A Preemptive Replacement Strategy For A Caching Dynamic Translator
HK	GRANTED	HK1048712	AFM Version Of Diode- And Cathodoconductivity-and Cathodoluminescence-Based Data Storage Media
IT	GRANTED	1398781	Luminescence-based Data Storage
JP	GRANTED	3471088	IMPROVED PROGRAMMABLE LOGIC CELL ARRAY ARCHITECTURE
JP	GRANTED	3573506	COMPUTER SYSTEM AND METHOD FOR SOLVING PREDICATE AND BOOLEAN EXPRESSION
JP	GRANTED	3638156	NETWORK
JP	GRANTED	3825443	Multiple Function Unit Processor Using Distributed Variable Length Instruction Words
JP	GRANTED	3896136	System And Method For Executing Branch Instructions In A VLIW Processc (as Amended)
JP	GRANTED	3961392	DIODE-BASED MULTIPLEXER
JP	GRANTED	3977880	OPERATING METHOD FOR PROGRAMMABLE GATE ARRAY
JP	GRANTED	4034135	PULSE TRAIN WRITING OF WORM STORAGE DEVICE
JP	GRANTED	4034969	Memory Manager For A Common Memory
JP	GRANTED	4083847	MEMORY REFRESHING METHOD AND SYSTEM
JP	GRANTED	4150748	Graph Partitioning Engine Based On Programmable Gate Arrays
JP	GRANTED	4386661	High Density Data Storage Module
NL	GRANTED	1167266	Collapsible Hub Assembly
SG	GRANTED	38849	PADDLELESS MOLDED PLASTIC SEMICONDUCTOR CHIP PACKAGE
TW	GRANTED	188749	Fault-Tolerant Solid State Memory
TW	GRANTED	203166	Method For Automatically Disabling Cell Phone Ringing (As Revised)
TW	GRANTED	223269	Write Pulse Limiting For Worm Storage Device
TW	GRANTED	10006168	Data Storage Device
TW	GRANTED	I240273	Thin Film Transistor Memory Device
TW	GRANTED	I240281	DIODE-BASED MULTIPLEXER
TW	GRANTED	I277097	Pulse Train Writing Of Worm Storage Device
US	GRANTED	5224263	Gentle package extraction tool and method
US	GRANTED	5235211	Semiconductor package having wraparound metallization
US	GRANTED	5235693	Method and apparatus for reducing buffer storage in a read-modify-write operation
US	GRANTED	5315178	IC which can be used as a programmable logic cell array or as a register fil
US	GRANTED	5325511	True least recently used replacement method and apparatus

US	GRANTED	5359728	Data integrity assurance in a disk drive upon a power failure
US	GRANTED	5396505	Programmable error-checking matrix for digital communication system
US	GRANTED	5404484	Cache system for reducing memory latency times
US	GRANTED	5422764	Electrical interconnect for a head/arm assembly of computer disk drives
US	GRANTED	5475823	Memory processor that prevents errors when load instructions are move in the execution sequence
US	GRANTED	5495570	Mirrored memory multi-processor system
US	GRANTED	5509139	Circuit for disabling an address masking control signal using OR gate wher a microprocessor is in a system management mode
US	GRANTED	5513363	Scalable register file organization for a computer architecture having multiple functional units or a large register file
US	GRANTED	5515381	Sequential parity correction for error-correcting RAM array
US	GRANTED	5519629	Tileable gate array cell for programmable logic devices and gate array having tiled gate array cells
US	GRANTED	5535354	Method for addressing a block addressable memory using a gray code
US	GRANTED	5537541	System independent interface for performance counters
US	GRANTED	5537575	System for handling cache memory victim data which transfers data from cache to the interface while CPU performs a cache lookup using cache status information
US	GRANTED	5544344	Apparatus for caching smram in an intel processor based computer syster employing system management mode
US	GRANTED	5553270	Apparatus for providing improved memory access in page mode access systems with pipelined cache access and main memory address replay
US	GRANTED	5557622	Method and apparatus for parity generation
US	GRANTED	5566325	Method and apparatus for adaptive memory access
US	GRANTED	5590087	Multi-ported data storage device with improved cell stability
US	GRANTED	5604376	Paddleless molded plastic semiconductor chip package
US	GRANTED	5604884	Burst SRAMS for use with a high speed clock
US	GRANTED	5615386	Computer architecture for reducing delays due to branch instructions
US	GRANTED	5617557	Using an address pin as a snoop invalidate signal during snoop cycles
US	GRANTED	5621883	Circuit for testing microprocessor memories
US	GRANTED	5628027	Method of determining the configuration of devices installed on a computer bus
US	GRANTED	5664135	Apparatus and method for reducing delays due to branches
US	GRANTED	5664225	Circuit for disabling an address masking control signal when a microprocessor is in a system management mode
US	GRANTED	5692154	Circuit for masking a dirty status indication provided by a cache dirty memory under certain conditions so that a cache memory controller properly controls a cache tag memory
US	GRANTED	5692169	Method and system for deferring exceptions generated during speculativ execution
US	GRANTED	5724550	Using an address pin as a snoop invalidate signal during snoop cycles
US	GRANTED	5729752	Network connection scheme
US	GRANTED	5754557	Method for refreshing a memory, controlled by a memory controller in a computer system, in a self-refresh mode while scanning the memory controller
US	GRANTED	5761077	Graph partitioning engine based on programmable gate arrays
US	GRANTED	5774714	Zone bit recording enhanced video data layout
US	GRANTED	5776800	Paddleless molded plastic semiconductor chip package

US	GRANTED	5778219	Method and system for propagating exception status in data registers and for detecting exceptions from speculative operations with non-speculative operations
US	GRANTED	5790771	Apparatus and method for configuring a reconfigurable electronic system having defective resources
US	GRANTED	5809549	Burst SRAMs for use with a high speed clock
US	GRANTED	5857116	Circuit for disabling an address masking control signal when a microprocessor is in a system management mode
US	GRANTED	5873089	Data handling system with circular queue formed in paged memory
US	GRANTED	5885853	Hollow chip package and method of manufacture
US	GRANTED	5933850	Instruction unit having a partitioned cache
US	GRANTED	5933857	Accessing multiple independent microkernels existing in a globally shared memory system
US	GRANTED	5951685	Computer system with system ROM including serial-access PROM coupled to an auto-configuring memory controller and method of shadowing BIOS code from PROM
US	GRANTED	5974501	Method and apparatus for detecting memory device types
US	GRANTED	5974514	Controlling SDRAM memory by using truncated burst read-modify-write memory operations
US	GRANTED	6023751	Computer system and method for evaluating predicates and Boolean expressions
US	GRANTED	6034919	Method and apparatus for using extended-data output memory devices in a system designed for fast page mode memory devices
US	GRANTED	6067649	Method and apparatus for a low power self test of a memory subsystem
US	GRANTED	6069573	Match and match address signal prioritization in a content addressable memory encoder
US	GRANTED	6070227	Main memory bank indexing scheme that optimizes consecutive page hits by linking main memory bank address organization to cache memory address organization
US	GRANTED	6081876	Memory error containment in network cache environment via restricted access
US	GRANTED	6112303	Computer system with system ROM including serial-access PROM coupled to an auto-configuring memory controller and method of shadowing BIOS code from PROM
US	GRANTED	6131150	Scaled memory allocation system
US	GRANTED	6134629	Determining thresholds and wrap-around conditions in a first-in-first-out memory supporting a variety of read and write transaction sizes
US	GRANTED	6144930	Method for providing a memory model of a memory device for use in simulation
US	GRANTED	6145061	Method of management of a circular queue for asynchronous access
US	GRANTED	6192423	Sharing a single serial port between system remote access software and a remote management microcontroller
US	GRANTED	6192447	Method and apparatus for resetting a random access memory
US	GRANTED	6208513	Independently mounted cooling fins for a low-stress semiconductor package
US	GRANTED	6209061	Integrated hierarchical memory overlay having invariant address space span that inactivates a same address space span in main memory
US	GRANTED	6226755	Apparatus and method for enhancing data transfer to or from a SDRAM system

US	GRANTED	6237065	Preemptive replacement strategy for a caching dynamic translator
US	GRANTED	6249465	Redundancy programming using addressable scan paths to reduce the number of required fuses
US	GRANTED	6275410	Data recording systems and methods for facilitating data recovery with emitter failure
US	GRANTED	6295582	System and method for managing data in an asynchronous I/O cache memory to maintain a predetermined amount of storage space that is readily available
US	GRANTED	6298411	Method and apparatus to share instruction images in a virtual cache
US	GRANTED	6298453	Method of determining signal delay of a resource in a reconfigurable system having multiple resources
US	GRANTED	6301140	Content addressable memory cell with a bootstrap improved compare
US	GRANTED	6317857	System and method for utilizing checksums to recover data
US	GRANTED	6321247	System and method for multiplication modulo (2N+1)
US	GRANTED	6374344	Methods and apparatus for processing load instructions in the presence c RAM array and data bus conflicts
US	GRANTED	6402692	Apparatus and method for detecting and storing information relating to a animal
US	GRANTED	6434048	Pulse train writing of worm storage device
US	GRANTED	6434060	Write pulse limiting for worm storage device
US	GRANTED	6438747	Programmatic iteration scheduling for parallel processors
US	GRANTED	6446157	Cache bank conflict avoidance and cache collision avoidance
US	GRANTED	6507552	AFM version of diode-and cathodoconductivity-and cathodoluminescence based data storage media
US	GRANTED	6508433	Collapsible hub assembly
US	GRANTED	6567301	One-time programmable unit memory cell based on vertically oriented fuse and diode and one-time programmable memory using the same
US	GRANTED	6614697	Diode-based multiplexer
US	GRANTED	6621096	Device isolation process flow for ARS system
US	GRANTED	6636943	Method for detecting continuity modules in a direct Rambus DRAM subsystem
US	GRANTED	6643248	Data storage device
US	GRANTED	6664193	Device isolation process flow for ARS system
US	GRANTED	6665201	Direct connect solid-state storage device
US	GRANTED	6678790	Microprocessor chip having a memory that is reconfigurable to function a on-chip main memory or an on-chip cache
US	GRANTED	6691252	Cache test sequence for single-ported row repair CAM
US	GRANTED	6697971	System and method for detecting attempts to access data residing outsid of allocated memory
US	GRANTED	6744681	Fault-tolerant solid state memory
US	GRANTED	6745263	Automated multiple data unit transfers between a host device and a storage medium
US	GRANTED	6754130	Memory having multiple write ports and write insert unit, and method of operation
US	GRANTED	6766445	Storage system for use in custom loop accelerators and the like
US	GRANTED	6766480	Using task description blocks to maintain information regarding operatior
US	GRANTED	6775034	Portable scanning apparatus having high storage capacity
US	GRANTED	6795907	Relocation table for use in memory management

US	GRANTED	6799254	Memory manager for a common memory
US	GRANTED	6804798	System and method for setting new values for configuration parameters on a device
US	GRANTED	6807609	Interleaving read and write operations on a bus and minimizing buffering on a memory module in a computer system
US	GRANTED	6810489	Checkpoint computer system utilizing a FIFO buffer to re-synchronize and recover the system on the detection of an error
US	GRANTED	6813627	Method and apparatus for performing integer multiply operations using primitive multi-media operations that operate on smaller operands
US	GRANTED	6815875	Electron source having planar emission region and focusing structure
US	GRANTED	6826653	Block data mover adapted to contain faults in a partitioned multiprocessc system
US	GRANTED	6839263	Memory array with continuous current path through multiple lines
US	GRANTED	6848033	Method of memory management in a multi-threaded environment and program storage device
US	GRANTED	6851018	Exchanging operation parameters between a data storage device and a controller
US	GRANTED	6864529	Thin film transistor memory device
US	GRANTED	6872964	Data storage device
US	GRANTED	6873840	Resource access/return system
US	GRANTED	6880067	Retiring instructions that meet the early-retirement criteria to improve computer operation throughput
US	GRANTED	6889305	Device identification using a memory profile
US	GRANTED	6889342	Preventing floppy disk data corruption
US	GRANTED	6892290	Linked-list early race resolution mechanism
US	GRANTED	6892319	Method for verifying abstract memory models of shared memory multiprocessors
US	GRANTED	6895476	Retry-based late race resolution mechanism for a computer system
US	GRANTED	6896134	Armored peripheral case
US	GRANTED	6897506	Systems and methods using non-volatile memory cells
US	GRANTED	6906964	Multiple buffer memory interface
US	GRANTED	6925047	High density data storage module
US	GRANTED	6928522	Unbalanced inclusive tags
US	GRANTED	6940770	Method for precharging word and bit lines for selecting memory cells within a memory array
US	GRANTED	6948112	System and method for performing backward error recovery in a comput
US	GRANTED	6950906	System for and method of operating a cache
US	GRANTED	6950912	Memory manager for a common memory
US	GRANTED	6952821	Method and system for memory management optimization
US	GRANTED	6961674	System and method for analysis of cache array test data
US	GRANTED	6968428	Microprocessor cache design initialization
US	GRANTED	6970724	Apparatus and method for automatically disabling cell phone ringing
US	GRANTED	6976143	Systems and methods for controlling communication with nonvolatile memory devices
US	GRANTED	6977979	Enhanced clock forwarding data recovery
US	GRANTED	6980507	Luminescence-phase change based data storage
US	GRANTED	6986005	Low latency lock for multiprocessor computer system
US	GRANTED	6989827	System and method for transferring data through a video interface

US	GRANTED	7000080	Channel-based late race resolution mechanism for a computer system
US	GRANTED	7000091	System and method for independent branching in systems with plural processing elements
US	GRANTED	7002820	Semiconductor storage device
US	GRANTED	7007184	DIMM connector accomodating sideband signals for battery status and/o control
US	GRANTED	7020757	Providing an arrangement of memory devices to enable high-speed data access
US	GRANTED	7024509	Passive release avoidance technique
US	GRANTED	7024520	System and method enabling efficient cache line reuse in a computer system
US	GRANTED	7024538	Processor multiple function units executing cycle specifying variable lengt instruction block and using common target block address updated pointe
US	GRANTED	7024550	Method and apparatus for recovering from corrupted system firmware in a computer system
US	GRANTED	7027380	Atomic resolution storage device
US	GRANTED	7055013	SPARE DATA SITE ALLOCATION
US	GRANTED	7057928	System and method for erasing high-density non-volatile fast memory
US	GRANTED	7085151	Storage device having a resistance measurement system
US	GRANTED	7093089	Systems and methods for storing data on computer systems
US	GRANTED	7120777	Device identification using a memory profile
US	GRANTED	7147108	Method and apparatus for the separation and collection of particles
US	GRANTED	7149155	Channeled dielectric re-recordable data storage medium
US	GRANTED	7161838	Thin film transistor memory device
US	GRANTED	7171594	Pausing a transfer of data
US	GRANTED	7178068	Memory image verification system and method
US	GRANTED	7188226	Defective data site information storage
US	GRANTED	7191189	Organizing data objects in a storage device
US	GRANTED	7194609	Branch reconfigurable systems and methods
US	GRANTED	7208867	Focusing structure for electron source
US	GRANTED	7213086	System having a storage controller that modifies operation of a storage system based on the status of a data transfer
US	GRANTED	7248518	Self-timed memory device providing adequate charging time for selected heaviest loading row
US	GRANTED	7281100	Data processing system and method
US	GRANTED	7342817	System and method for writing data using an electron beam
US	GRANTED	7383392	Performing read-ahead operation for a direct input/output request
US	GRANTED	7386333	Test subject monitoring device
US	GRANTED	7391635	Method and apparatus for variable-resolution memory
US	GRANTED	7418381	Device for automatically translating and presenting voice messages as tex messages
US	GRANTED	7418644	System for error correction coding and decoding
US	GRANTED	7421459	Buffer management for data transfers between a host device and a storage medium
US	GRANTED	7454221	Electron tube amplification
US	GRANTED	7467264	Methods and apparatuses for determining the state of a memory elemen
US	GRANTED	7484079	Pipeline stage initialization via task frame accessed by a memory pointer propagated among the pipeline stages

US	GRANTED	7496216	Fingerprint capture
US	GRANTED	7742045	System and method for an enhanced analog video interface
US	GRANTED	20060274629	Data storage device
US	GRANTED	20070027977	System and method for self configuration of reconfigurable systems
WO	NATIONAL		METHOD OF ASYNCHRONOUS MANAGEMENT OF A CIRCULAR QUEUE IN A MULTIPROCESS ENVIRONMENT
WO	NATIONAL	02/077794	STORAGE SYSTEM FOR USE IN CUSTOM LOOP ACCELERATORS AND THE LIKE
WO	NATIONAL	03/058433	MULTIPLE FUNCTION UNIT PROCESSOR USING DISTRIBUTED VARIABLE LENGTH INSTRUCTION WORDS
WO	NATIONAL	04/015562	SYSTEM AND METHOD USING DIFFERENTIAL BRANCH LATENCY PROCESSING ELEMENTS
WO	NATIONAL	04/17207	METHOD AND SYSTEM FOR MEMORY MANAGEMENT OPTIMIZATION
WO	NATIONAL	WO2006/002115	RECORD LOW PROGRAMMING CURRENT FOR NONVOLATILE MEMORY DEVICE FROM TIP-PHASE CHANGE MATERIAL (PCM) INTERACTION

Foreign Patents and Applications Pending Diligence Review

[illegible]	[illegible]	[illegible]	[illegible]		
CN	checking status			CN1490805A	Luminescence-based Data Storage
DE	checking status			DE60218945D1	Memory Array
EP	checking status	02255084.2	1288968		Atomic Resolution Storage Device
FR	checking status	02255052.9	1282136	1282136	Write Pulse Limiting For Worm Storage Device
HK	checking status	04105736.4	1062953A		Solid state memory
IN	checking status	626/CHE/2006			Performing Read-ahead Operation For A Direc Input/output Request
JP	checking status	PH10-000153		3930629	Performing Read-ahead Operation For A Direc Input/output Request
JP	checking status			JP2002222930A	AFM version of diode-and cathodoconductivit cathodoluminescence-based data storage mec
JP	checking status	P2003-126349		P2003-126349	Write Pulse Limiting For Worm Storage Device
JP	checking status	P2003-415025			Systems And Methods For Storing Data On Co Systems
TW	checking status	92125343			System For And Method Of Operating A Cache
TW	checking status	93104967			METHOD AND DEVICE FOR USING EDO MEMO MEMORY SYSTEM DESIGNED FOR FPM MEMO