PATENT ASSIGNMENT

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Cypress Semiconductor Corporation	12/21/2010

RECEIVING PARTY DATA

Name:	Rambus Inc.
Street Address:	1050 Enterprise Way
Internal Address:	Suite 700
City:	Sunnyvale
State/Country:	CALIFORNIA
Postal Code:	94089

PROPERTY NUMBERS Total: 10

Property Type	Number
Patent Number:	5424991
Patent Number:	5530675
Patent Number:	5835401
Patent Number:	5978868
Patent Number:	6430718
Patent Number:	7269772
Patent Number:	7345946
Patent Number:	7394716
Application Number:	60613174
Application Number:	60667412

CH $400.00 5424991

CORRESPONDENCE DATA

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Total Attachments: 2
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EXHIBIT D

PATENT ASSIGNMENT

This Patent Assignment ("Patent Assignment") dated as of December 21, 2010 ("Effective Date"), is made by and between Cypress Semiconductor Corporation, a Delaware corporation having a principal place of business at 198 Champion Court, San Jose, CA 95134-1709 ("Assignor") and Rambus Inc., a Delaware corporation having a principal place of business at 1050 Enterprise Way, Suite 700, Sunnyvale, CA 94089 ("Assignee").

WHEREAS, Assignor is sole and exclusive owner of all right, title and interest in and to the "Patents" defined as each and all of: (a) the patents and patent applications listed below, (b) any and all reexaminations, extensions and reissues thereof; and (c) any and all patents and patent applications that directly or indirectly claim priority thereto, including, without limitation, any and all divisionals, substitutions, continuations, and continuations-in-part thereof, and any and all foreign applications or patents, or certificates of invention corresponding thereto.

WHEREAS, Assignee wishes to acquire the Patents.

Patent Title	Inventor(s)	Patent No.	Date Issued	Appl. Serial No.	Appl. Filing Date
Floating Gate Nonvolatile Memory with Uniformly Erased Threshold Voltage	Hu, Genda J.	5,424,991	June 13, 1995	08/030,458	April 1, 1993
Floating Gate Nonvolatile Memory with Uniformly Erased Threshold Voltage	Hu, Genda J.	5,530,675	June 25, 1996	08/442,682	May 17, 1995
DRAM with Hidden Refresh	Green, Gary W.; Torode, John Q.; Rodgers, T.J.; Shah, Shailesh	5,835,401	November 10, 1998	08/760,823	December 5, 1996
System for Generating Buffer Status Flags by Comparing Read and Write Pointers and Determining Direction of Progression of Read Pointer with Respect to Write Pointer	Maas, Michael F.	5,978,868	November 2, 1999	08/919,653	August 28, 1997
Architecture, Circuitry and Method for Testing One or More Integrated Circuits and/or Receiving Test Information Therefrom	Nayak, Anup K.	6,430,718	August 6, 2002	09/385,189	August 30, 1999
Method and Apparatus for Built-In Self-Test (BIST) of Integrated Circuit Device	Li, Jun; Tzou, Joseph; Tran, Thinh	7,269,772	September 11, 2007	10/785,826	February 23, 2004
Dual-Voltage Wordline Drive Circuit With Two Stage Discharge	Chapman, David; Arora, Anupam; Ma, Lin; Parent, Richard	7,345,946	March 18, 2008	11/234,028	September 23, 2005
Bank Availability Indications for Memory Device and Method Therefor	Chakrapani, Anuj; Manapat, Rajesh	7,394,716	July 1, 2008	11/395,416	March 31, 2006
Dual-Voltage Level Wordline Drive Circuit with Two Stage Discharge	Chapman, David E.; Arora, Anupam; Ma, Lin	N/A	N/A	60/613,174	September 24, 2004
Bank Selection on Synchronous DRAMs	Chakrapani, Anuj; Manapat, Rajesh	N/A	N/A	60/667,412	April 1, 2005

Now, for good and valuable consideration, Assignor, on behalf of itself and its Subsidiaries, hereby irrevocably sells, assigns, transfers and conveys to Assignee the entire worldwide right, title and interest in and to (a) the Patents; (b) all inventions, discoveries and disclosures that are disclosed in the Patents; and (c) any and all other common law or statutory rights, claims and privileges pertaining to, arising out of, or associated with the Patents, including, without limitation, the right to file, prosecute and maintain such Patents and patent applications, and the right to seek equitable relief, sue and recover damages for all past, present and future infringement of such patents.

Assignor further assigns to and empowers Assignee, its successors, assigns or nominees, all rights to make applications for patents or other forms of protection for said inventions and to prosecute such applications and the Patents, as well as to claim and receive the benefit of the right of priority provided by the International Convention for the Protection of Industrial Property, as amended, or by any convention which may henceforth be substituted for it, and the right to invoke and claim such right of priority without further written or oral authorization.

IN WITNESS WHEREOF, the parties have caused this Patent Assignment to be executed as of the Effective Date.

ASSIGNOR:

CYPRESS SEMICONDUCTOR CORPORATION

By: Cathal G. Phelan

Name: CATHAL G. PHELAN

Title: CHIEF TECHNICAL OFFICER

ASSIGNEE:

RAMBUS INC.

By: Laura S Stark

Name: LAURA STARK

Title: SVP