PATENT ASSIGNMENT

Electronic Version v1.1
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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Vanguard International Semiconductor Corporation	10/26/2010

RECEIVING PARTY DATA

Name:	Taiwan Semiconductor Manufacturing Co., Ltd.
Street Address:	No. 8, Li-Hsin Rd. 6, Science-Based Industrial Park
City:	Hsin-Chu
State/Country:	TAIWAN
Postal Code:	300-77

PROPERTY NUMBERS Total: 75

Property Type	Number
Patent Number:	6008513
Patent Number:	5858831
Patent Number:	5869861
Patent Number:	5870343
Patent Number:	5977558
Patent Number:	5872018
Patent Number:	5998820
Patent Number:	5872032
Patent Number:	5874336
Patent Number:	5877052
Patent Number:	5879986
Patent Number:	5888863
Patent Number:	5893734
Patent Number:	5895239
Patent Number:	5895250

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Patent Number:	5897352
Patent Number:	5899716
Patent Number:	5904521
Patent Number:	6018177
Patent Number:	5909619
Patent Number:	5913119
Patent Number:	5917748
Patent Number:	5920775
Patent Number:	6184548
Patent Number:	5920785
Patent Number:	5923973
Patent Number:	5926710
Patent Number:	5926719
Patent Number:	5930625
Patent Number:	6057573
Patent Number:	5933725
Patent Number:	5936898
Patent Number:	5943581
Patent Number:	5956587
Patent Number:	5956594
Patent Number:	6171923
Patent Number:	5976945
Patent Number:	5976981
Patent Number:	6001717
Patent Number:	6004853
Patent Number:	6008084
Patent Number:	6133599
Patent Number:	6008085
Patent Number:	6010933
Patent Number:	6010942
Patent Number:	6016279
Patent Number:	6137130
Patent Number:	6025227
Patent Number:	6037216
Patent Number:	6037219

Patent Number:	6037220
Patent Number:	6046083
Patent Number:	6046084
Patent Number:	6054347
Patent Number:	6060353
Patent Number:	6077742
Patent Number:	6077743
Patent Number:	6080620
Patent Number:	6100137
Patent Number:	6114198
Patent Number:	6114202
Patent Number:	6124165
Patent Number:	6130127
Patent Number:	6136643
Patent Number:	6136661
Patent Number:	6141285
Patent Number:	6150213
Patent Number:	6165830
Patent Number:	6168987
Patent Number:	6373090
Patent Number:	6174767
Patent Number:	6174815
Patent Number:	6413813
Patent Number:	6177695
Patent Number:	6180453

CORRESPONDENCE DATA

Fax Number: (770)951-0933

Correspondence will be sent via US Mail when the fax attempt is unsuccessful.

Phone: 770-933-9500

Email: dan.mcclure@tkhr.com

Correspondent Name: THOMAS, KAYDEN, HORSTEMEYER & RISLEY

Address Line 1: 600 GALLERIA PKWY

Address Line 2: SUITE 1500

Address Line 4: ATLANTA, GEORGIA 30339

ATTORNEY DOCKET NUMBER:	252106-9000 (#2)

NAME OF SUBMITTER:	Daniel R. McClure

Total Attachments: 14
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EXHIBIT B

PATENT ASSIGNMENT

THIS ASSIGNMENT (the "Assignment"), effective as of October 26, 2010 is made by and between by and between Taiwan Semiconductor Manufacturing Company, Ltd., a Taiwan, Republic of China corporation ("Assignee"), and Vanguard International Semiconductor Corporation, a Taiwan, Republic of China corporation (the "Assignor"). Assignee and Assignor are referred to herein as the "Parties" and each individually as a "Party."

WITNESSETH:

WHEREAS, the Parties entered into that certain Asset Purchase Agreement, dated as of October 26, 2010, by and among, Assignor and Assignee (the "Purchase Agreement");

WHEREAS, pursuant to the Purchase Agreement, Assignor agreed to transfer to Assignee all of the right, title and interest of Assignor in and to certain assets, properties, rights and interests, including without limitation, certain Patent Rights (as defined in the Purchase Agreement);

WHEREAS, Assignee is desirous of acquiring (and Assignor is desirous of assigning to Assignee) the entire right, title and interest in and to the Patent Rights and the inventions disclosed and/or claimed in the Patent Rights, and in and to any and all Letters Patents worldwide which may be obtained therefor;

NOW, THEREFORE, for good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged:

1. Assignor does hereby sell, assign, transfer, and convey to Assignee free and clear of all liens or other encumbrances, except for those Encumbrances (as such term is defined in the Purchase Agreement) listed in Exhibit D to the Purchase Agreement, and to the maximum extent provided under law, all of Assignor's entire worldwide right, title and interest in, to, and under the Patent Rights, the same to be held and enjoyed by Assignee for its own use and enjoyment and the use and enjoyment of its successors, assigns or other legal representatives, as fully and entirely as the same would have been held and enjoyed by Assignor if this assignment and sale had not been made, as assignee of its entire right, title and interest therein and in and to all income, royalties, damages and payments now or hereafter due or payable with respect thereto in and to all causes of action (either in law or in equity) and the right to sue, counterclaim, and recover for past, present and future infringement of the rights assigned or to be assigned under this Assignment.

2. Assignor hereby covenants and agrees that Assignor will not execute any writing or do any act whatsoever conflicting with this Assignment, and that Assignor will, at any time upon request, without further or additional consideration but at the expense of Assignee, execute such additional assignments and other writings and do such additional acts as Assignee

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may deem necessary or desirable to perfect Assignee's enjoyment of this grant, and render all necessary or desirable assistance in making application for and obtaining original, divisional, continuations, continuation-in-part, reexamined, reissued, or extended letters patent or of any and all foreign countries on said inventions, and in enforcing any rights or causes of action accruing as a result of such applications or patents, by giving testimony in any proceedings or transactions involving such applications or patents, and/or by executing preliminary statements and other affidavits.

3. The Parties authorize and request that the Commissioner of Patents and Trademarks of the United States, and the corresponding entities or agencies in any applicable foreign countries, record Assignee as the owner of record for the Patent Rights and issue the patent for the pending Patent Rights to the Assignee upon issuance.

4. All disputes, claims or controversies arising out of this Assignment, or the negotiation, validity or performance of this Assignment, or the transactions contemplated hereby shall be governed by and construed in accordance with the laws of the Republic of China without regard to its rules of conflict of laws.

5. This Assignment shall be binding upon and inure to the benefit of the Parties and their respective successors and assigns.

6. If any provision of this Assignment or the application of any such provision to any person or circumstance shall be held invalid, illegal or unenforceable in any respect by a court of competent jurisdiction, such invalidity, illegality or unenforceability shall not affect any other provision hereof.

7. This Assignment may be executed in two (2) counterparts, each of which when so executed and delivered shall be deemed an original, and such counterparts together shall constitute one and the same instrument.

IN WITNESS WHEREOF, Assignor and Assignee have caused this Assignment to be duly executed in duplicate originals by their duly authorized representative as of the day and year first above written.

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VANGUARD INTERNATIONAL SEMICONDUCTOR CORPORATION
(as Assignor)

By: ______________________
Name: Ching-Chu Chang
Title: Chairman

TAIWAN SEMICONDUCTOR MANUFACTURING COMPANY, LTD.
(as Assignee)

By: ______________________
Name: Richard L. Thurston
Title: Sr. Vice President and General Counsel

LEGAL

5 Sworn to and subscribed before me
this _____ day of October, 2010.

____
Notary Public
10 My Commission Expires: ______________

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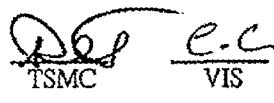
Exhibit A

Patent Rights

Item No.	Patent No.	Country	Title	File Date
D009-01	5583070	USA	Process to form rugged polycrystalline silicon surfaces	07/07/1995
D039-01	5712202	USA	Method for fabricating a multiple walled crown capacitor of a semiconductor device	12/27/1995
D043-01	5780338	USA	Method for manufacturing crown-shaped capacitors for . dynamic random access memory integrated circuits	04/11/1997
D044-01	5780339	USA	Method for fabricating a semiconductor memory cell in a DRAM	05/02/1997
D044-02	099650	Taiwan	在一動態隨機存取記憶體中製作一半導體記憶胞之方法	04/29/1997
D044-03	144361	China	在一動態隨機存取記憶體中製作一半導體記憶胞之方法	05/06/1998
D045-01	5789289	USA	Method for fabricating vertical fin capacitor structures	06/18/1996
D045-02	090852	Taiwan	垂直鰭型電容器結構的製造方法	12/05/1996
D046-01	5789291	USA	Dram cell capacitor fabrication method	08/07/1995
D063-01	5837581	USA	Method for forming a capacitor using a hemispherical-grain structure	04/04/1997
D063-02	099232	Taiwan	以半球形顆粒結構形成隨機存取記憶體之電容的方法	04/01/1997
D074-01	5874336	USA	Method to improve yield for capacitors formed using etchback of polysilicon hemispherical grains	06/23/1997
D074-02	103345	Taiwan	利用複晶矽半球的晶粒回蝕刻以形成電容器來改善良率的方法	11/25/1997
D074-03	130088	China	利用複晶矽半球的晶粒回蝕刻以形成電容器來改善良率的方法	03/19/1998
D075-01	5877052	USA	Resolution of hemispherical grained silicon peeling and row-disturb problems for dynamic random access memory, stacked capacitor structures	06/11/1998
D075-02	117929	Taiwan	解決半球狀顆粒矽層脫落以及陣列擾動問題的動態隨機存取記憶體以及柱狀電容器結構	06/16/1998
D076-01	5879986	USA	Method for fabrication of a one gigabit capacitor over bit line DRAM cell with an area equal to eight times the used minimum feature	02/27/1998
D076-02	114153	Taiwan	半導體基底上高密度ＤＲＡＭ胞的製造方法	04/17/1998
D078-01	5893734	USA	Method for fabricating capacitor-under-bit line (CUB) dynamic random access memory (DRAM) using tungsten landing plug contacts	09/14/1998
D079-01	5895239	USA	Method for fabricating dynamic random access memory (DRAM) by simultaneous formation of tungsten bit lines and tungsten landing plug contacts	09/14/1998
D079-02	119432	Taiwan	製造動態隨機存取記憶（ＤＲＡＭ）之方法	12/31/1998
D080-01	5895250	USA	Method of forming semicrown-shaped stacked capacitors for dynamic random access memory	06/11/1998
D081-01	5897352	USA	Method of manufacturing hemispherical grained polysilicon with improved adhesion and reduced capacitance depletion	03/25/1998
D081-02	132383	Taiwan	增進附著力及降低電容缺乏之半球顆粒複晶矽	05/22/1998
D085-01	5913119	USA	Method of selective growth of a hemispherical grain silicon layer on the outer sides of a crown shaped DRAM capacitor structure	06/26/1998

TSMC VIS

Item No.	Patent No.	Country	Title	File Date
D085-02	114769	Taiwan	一種動態隨機存取記憶體之電容器結構的製造方法	08/14/1998
D092-01	5930625	USA	Method for fabricating a stacked, or crown shaped, capacitor structure	04/24/1998
D095-01	5943581	USA	Method of fabricating a buried reservoir capacitor structure for high-density dynamic random access memory (DRAM) circuits	11/05/1997
D097-01	5956594	USA	Method for simultaneously forming capacitor plate and metal contact structures for a high density DRAM device	11/02/1998
D097-02	131815	Taiwan	同時形成電容器極板與金屬接觸窗構造的高密度ＤＲＡＭ裝置	12/18/1998
D099-01	5976981	USA	Method for manufacturing a reverse crown capacitor for DRAM memory cell	06/12/1998
D104-01	6010933	USA	Method for making a planarized capacitor-over-bit-line structure for dynamic random access memory (DRAM) devices	07/17/1998
D104-02	113320	Taiwan	在基板上製作具有直線位元線形狀的位元線上電容器結構之ＤＲＡＭ元件的方法	10/30/1998
D105-01	6010942	USA	Post chemical mechanical polishing, clean procedure, used for fabrication of a crown shaped capacitor structure	05/26/1999
D107-01	6025227	USA	Capacitor over bit line structure using a straight bit line shape	11/03/1997
D107-02	6137130	USA	Capacitor over bit line structure using a straight bit line shape	12/06/1999
D108-01	6037216	USA	Method for simultaneously fabricating capacitor structures, for giga-bit DRAM cells, and peripheral interconnect structures, using a dual damascene process	11/02/1998
D108-02	125505	Taiwan	使用雙重鑲嵌法以同時製造動態隨機存取記憶體單元之電容結構及其周邊互連結構之方法	03/09/1999
D109-01	6037219	USA	One step in situ doped amorphous silicon layers used for selective hemispherical grain silicon formation for crown shaped capacitor applications	06/25/1998
D109-02	113906	Taiwan	製造動態隨機存取記憶體元件之電容器結構的方法	09/17/1998
D111-01	6046083	USA	Growth enhancement of hemispherical grain silicon on a doped polysilicon storage node capacitor structure, for dynamic random access memory applications	06/26/1998
D111-02	112870	Taiwan	在半導體基材上製造動態隨機存取記憶體元件之電容器結構的方法	08/14/1998
D112-01	6046084	USA	Isotropic etching of a hemispherical grain silicon layer to Improve the quality of an overlying dielectric layer	09/03/1999
D112-02	119433	Taiwan	電容器的製造方法	01/26/1999
D113-01	6054347	USA	Method for forming a modified crown shaped, dynamic random access memory, (DRAM), capacitor structure	01/04/1999
D113-02	119815	Taiwan	形成一改良式皇冠狀動態隨機存取記憶體之電容器結構的方法	05/06/1999
D114-01	6060353	USA	Method of forming a ring shaped storage node structure for a DRAM capacitor structure	10/22/1999
D115-01	6077742	USA	Method for making dynamic random access memory (DRAM) cells having zigzag-shaped stacked capacitors with increased capacitance	04/24/1998
D115-02	115000	Taiwan	一種鋸齒狀堆疊電容的動態隨機存取記憶體單元陣列的製作方法	06/26/1998
D116-01	6077743	USA	Method for making dynamic random access memory cells having brush-shaped stacked capacitors patterned from a hemispherical grain hard mask	04/24/1998



Item No.	Patent No.	Country	Title	File Date
D117-01	6080620	USA	Method for fabricating interconnection and capacitors of a DRAM using a simple geometry active area, self-aligned etching, and polysilicon plugs	06/03/1998
D117-02	129045	Taiwan	具有電容器之動態隨機存取記憶體以及其製造方法	08/12/1999
D119-01	6114198	USA	Method for forming a high surface area capacitor electrode for DRAM applications	05/07/1999
D119-02	129388	Taiwan	電容結構之製造方法	07/27/1999
D122-01	6130127	USA	Method for making dynamic random access memory cells having cactus-shaped stacked capacitors with increased capacitance	07/23/1999
D122-02	129003	Taiwan	製造具有仙人掌形堆疊式電容之動態隨機存取記憶胞以增加電容量的方法	11/01/1999
D123-01	6136643	USA	Method for fabricating capacitor-over-bit-line dynamic random access memory (DRAM) using self-aligned contact etching technology	02/11/1999
D123-02	120060	Taiwan	一種使用自動對準接觸窗方式製造位元線上之電容器之動態隨機存取記憶體的方法	04/27/1999
D127-01	6165830	USA	Method to decrease capacitance depletion, for a DRAM capacitor, via selective deposition of a doped polysilicon layer on a selectively formed hemispherical grain silicon layer	11/02/1998
D127-02	123629	Taiwan	藉由選擇性沈積一摻雜複晶矽層於選擇形成之半球形晶粒矽層上以減少ＤＲＡＭ電容器發生電容空乏的方法	06/29/1999
D128-01	6168987	USA	Method for fabricating crown-shaped capacitor structures	04/09/1996
D128-02	089246	Taiwan	製造皇冠型電容器結構的方法	07/04/1996
D134-01	6194265	USA	Process for integrating hemispherical grain silicon and a nitride-oxide capacitor dielectric layer for a dynamic random access memory capacitor structure	07/22/1999
D135-01	6200898	USA	Global planarization process for high step DRAM devices via use of HF vapor etching	10/25/1999
D141-01	6251742	USA	Method of manufacturing a cup-shape capacitor	01/04/1999
D141-02	164908	Taiwan	動態隨機存取記憶體之杯型電容製作方法	12/14/1998
D142-01	6258663	USA	Method for forming storage node	05/01/1998
D142-02	113494	Taiwan	動態隨機存取記憶體內儲存節點之製造方法	05/18/1998
D155-01	6479341	USA	Capacitor over metal DRAM structure	03/02/1998
D155-02	122028	Taiwan	具有在金屬上的電容器之堆疊的電容器結構之ＤＲＡＭ裝置及製造方法	10/15/1998
D170-01	124109	Taiwan	塗佈光阻層於杯狀電容上之方法	07/29/1999
D172-01	123622	Taiwan	一種皇冠形電容板結構形成方法	05/11/1999
D001-01	5508223	USA	Method for manufacturing DRAM cell with fork-shaped capacitor	05/05/1995
D002-01	5543345	USA	Method for fabricating crown capacitors for a dram cell	12/27/1995
D003-01	5547890	USA	DRAM cell with a cradle-type capacitor	05/05/1995
D006-01	5563088	USA	Method for fabricating a stacked capacitor in a DRAM cell	02/02/1996
D007-01	5567640	USA	Method for fabricating T-shaped capacitors in DRAM cells	01/11/1996
D008-01	5578516	USA	High capacitance dynamic random access memory manufacturing process	07/07/1995
D010-01	5595928	USA	High density dynamic random access memory cell structure	09/18/1995

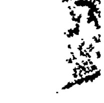
TSMC VIS

Item No.	Patent No.	Country	Title	File Date
			having a polysilicon pillar capacitor	
D010-02	6262449	USA	High density dynamic random access memory cell structure having a polysilicon pillar capacitor	09/09/1996
D011-01	5595929	USA	Method for fabricating a dram cell with a cup shaped storage node	01/16/1996
D011-02	6204526	USA	Method for fabricating a DRAM cell with a cup shaped storage node	10/02/1996
D012-01	5604146	USA	Method to fabricate a semiconductor memory device having an E-shaped storage node	06/10/1996
D012-02	5889301	USA	Semiconductor memory device having an E-shaped storage node	10/04/1996
D012-03	113997	Taiwan	高密度堆疊式電容器的製造方法	11/28/1995
D013-01	5643819	USA	Method of fabricating fork-shaped stacked capacitors for DRAM cells	10/30/1995
D015-01	5650351	USA	Method to form a capacitor having multiple pillars for advanced DRAMS	01/11/1996
D016-01	5652165	USA	Method of forming a stacked capacitor with a double wall crown shape	06/10/1996
D016-02	085855	Taiwan	多柱型電容器的形成方法	02/09/1996
D017-01	5656532	USA	Method for fabricating a coaxial capacitor of a semiconductor device	01/11/1996
D017-02	077916	Taiwan	雙凹溝電容器之動態隨機存取記憶體的製造方法	08/29/1995
D018-01	5656536	USA	Method of manufacturing a crown shaped capacitor with horizontal fins for high density DRAMs	03/29/1996
D020-01	5663093	USA	Method for forming a cylindrical capacitor having a central spine	06/17/1996
D020-02	085647	Taiwan	高密度記憶體元件的結構和製造方法	02/09/1996
D023-01	5670407	USA	Method of fabricating a toothed-shape capacitor node in a semiconductor DRAM circuit	01/30/1997
D023-02	089408	Taiwan	一種記憶體電容器元件的製造方法	02/05/1997
D025-01	5677221	USA	Method of manufacture DRAM capacitor with reduced layout area	06/19/1996
D026-01	5677222	USA	Method for forming a DRAM capacitor	10/11/1996
D026-02	088942	Taiwan	一種改良型堆疊式電容器的製造方法	08/27/1996
D027-01	5677223	USA	Method for manufacturing a DRAM with reduced cell area	10/07/1996
D027-02	123089	Taiwan	一種縮小記憶元面積的方法	08/12/1996
D029-01	5679596	USA	Spot deposited polysilicon for the fabrication of high capacitance, DRAM devices	10/18/1996
D029-02	087198	Taiwan	一種利用點狀複晶矽製造高電容動態隨機存取記憶體元件的方法	12/05/1996
D030-01	5681773	USA	Method for forming a DRAM capacitor	10/28/1996
D031-01	5681774	USA	Method of fabricating a toothed-shape capacitor node using a thin oxide as a mask	01/30/1997
D031-02	098987	Taiwan	一種積體電路記憶元件的製造方法	02/05/1997
D032-01	5686337	USA	Method for fabricating stacked capacitors in a DRAM cell	01/11/1996
D032-02	083244	Taiwan	記憶體之堆疊式電容器的製造方法	01/03/1996
D033-01	5688713	USA	Method of manufacturing a DRAM cell having a double-crown capacitor using polysilicon and nitride spacers	08/26/1996

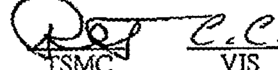
TSMC VIS

Item No.	Patent No.	Country	Title	File Date
D034-01	5705438	USA	Method for manufacturing stacked dynamic random access memories using reduced photoresist masking steps	10/18/1996
D034-02	086756	Taiwan	一種減少光罩之堆疊式動態隨機存取記憶體的製造方法	08/27/1996
D035-01	5706164	USA	Method of fabricating high density integrated circuits, containing stacked capacitor DRAM devices, using elevated trench isolation and isolation spacers	07/17/1996
D035-02	095633	Taiwan	包含堆疊式電容器ＤＲＡＭ元件並使用高架溝槽隔絕物和隔絕空間子的高密度積體電路的製造方法	08/29/1996
D037-01	5710074	USA	Increased surface area of an STC structure via the use of a storage node electrode comprised of polysilicon mesas and polysilicon sidewall spacers	10/18/1996
D037-02	096592	Taiwan	一種半導體記憶元件的製造方法	08/27/1996
D038-01	5710075	USA	Method to increase surface area of a storage node electrode, of an STC structure, for DRAM devices	11/06/1996
D038-02	095727	Taiwan	記憶體元件的製造方法	08/12/1996
D040-01	5744387	USA	Method for fabricating dynamic random access memory with a flat topography and fewer photomasks	03/07/1997
D041-01	5759894	USA	Method for forming a DRAM capacitor using HSG-Si	02/28/1997
D048-01	5792689	USA	Method for manufacturing double-crown capacitors self-aligned to node contacts on dynamic random access memory	04/11/1997
D050-01	5792693	USA	Method for producing capacitors having increased surface area for dynamic random access memory	03/07/1997
D050-02	095336	Taiwan	具有大表面積之電荷儲存電極之電容器的製造方法	12/05/1996
D051-01	5795806	USA	Method to increase the area of a stacked capacitor structure by creating a grated top surface bottom electrode	04/09/1997
D053-01	5807775	USA	Method for forming a double walled cylindrical capacitor for a DRAM	06/24/1996
D054-01	5807782	USA	Method of manufacturing a stacked capacitor having a fin-shaped storage electrode on a dynamic random access memory cell	09/25/1995
D056-01	5817554	USA	Use of a grated top surface topography for capacitor structures	03/07/1997
D057-01	5821142	USA	Method for forming a capacitor with a multiple pillar structure	04/08/1996
D057-02	6071774	USA	Method for forming a capacitor with a multiple pillar structure	07/24/1998
D057-03	089248	Taiwan	形成具有多個柱体結構之電容器的方法	07/24/1996
D058-01	5824582	USA	Stack DRAM cell manufacturing process with high capacitance capacitor	06/04/1997
D058-02	093776	Taiwan	堆疊式動態隨機存取記憶體之電容器的製造方法	03/14/1997
D059-01	5830792	USA	Method of making a stack capacitor in a DRAM cell	05/21/1997
D059-02	101475	Taiwan	一種動態隨機存取記憶體的製造方法	05/02/1997
D060-01	5834349	USA	Method for fabricating memory cells using chemical mechanical polishing technology	12/02/1996
D060-02	087853	Taiwan	一種利用化學機械式琢磨技術製造記憶元的方法	08/27/1996
D061-01	5837575	USA	Method for forming a DRAM capacitor	10/11/1996
D064-01	5843820	USA	Method of fabricating a new dynamic random access memory (DRAM) cell having a buried horizontal trench capacitor	09/29/1997
D064-02	6218693	USA	Dynamic random access memory (DRAM) cell having a buried horizontal trench capacitor by a novel fabrication method	09/30/1998

TSMC VIS



Item No.	Patent No.	Country	Title	File Date
D064-03	103360	Taiwan	製造隱匿於一半導體基底的水平溝槽電容器的方法	01/06/1998
D064-04	3110013	Japan	製造隱匿於一半導體基底的水平溝槽電容器的方法	04/21/1998
D064-05	128743	China	製造隱匿於一半導體基底的水平溝槽電容器的方法	05/29/1998
D065-01	5843821	USA	Fabrication method for a cylindrical capacitor for a semiconductor device	06/04/1997
D065-02	102481	Taiwan	高密度記憶體積體電路的製造方法	03/14/1997
D066-01	5851877	USA	Method of forming a crown shape capacitor	01/06/1998
D066-02	105835	Taiwan	皇冠形電容之製作方法	12/29/1997
D067-01	5854105	USA	Method for making dynamic random access memory cells having double-crown stacked capacitors with center posts	11/05/1997
D067-02	095352	Taiwan	積體電路電容器之多層同軸型電荷儲存電極的製造方法	07/31/1997
D070-01	5869861	USA	Coaxial capacitor for DRAM memory cell	06/03/1996
D077-01	5888863	USA	Method to fabricate capacitors in memory circuits	05/16/1996
D082-01	5899716	USA	Oxygen ion implantation procedure to increase the surface area of an STC structure	05/19/1997
D082-02	093232	Taiwan	具高電容之記憶體積體電路之電容器的製造方法	03/14/1997
D083-01	5904521	USA	Method of forming a dynamic random access memory	08/28/1997
D083-02	120331	Taiwan	形成動態隨機存取記憶體之方法	08/22/1997
D089-01	5923973	USA	Method of making greek letter psi shaped capacitor for DRAM circuits	10/24/1997
D090-01	5926710	USA	Method for making dynamic random access memory cells using a novel stacked capacitor process	10/23/1997
D110-01	6037220	USA	Method of increasing the surface area of a DRAM capacitor structure via the use of hemispherical grained polysilicon	07/24/1998
D110-02	117836	Taiwan	ＤＲＡＭ裝置用之堆疊電容結構之製造方法及堆疊電容結構之儲存節點結構的製造方法	11/13/1998
D118-01	6100137	USA	Etch stop layer used for the fabrication of an overlying crown shaped storage node structure	08/12/1999
D118-02	129048	Taiwan	在半導體基板上製造動態隨機存取記憶體電容器冠狀儲存節點結構的方法	10/05/1999
D120-01	6114202	USA	Method of fabricating dynamic random access memory	06/09/1999
D120-02	123156	Taiwan	動態隨機存取記憶體的製造方法	05/27/1999
D137-01	6218242	USA	Method for fabricating capacitors in semiconductor integrated circuit	09/13/2000
D137-02	138182	Taiwan	半導體積體電路之電容器的製造方法	10/09/2000
D143-01	6261901	USA	Method of manufacturing a DRAM capacitor with a dielectric column	06/30/2000
D143-02	139432	Taiwan	具有介電柱之電容器的製造方法	07/24/2000
D143-03	178094	China	具有介電柱之電容器的製造方法	08/08/2000
D144-01	6271072	USA	Method of manufacturing a storage node having five polysilicon bars	06/14/1999
D145-01	6277688	USA	Method of manufacturing a DRAM capacitor with increased electrode surface area	06/30/2000
D145-02	142572	Taiwan	具有導電柱之電容器的製造方法	08/07/2000
D147-01	6297121	USA	Fabrication method for capacitors in integrated circuits with a self-aligned contact structure	08/16/2000



Item No.	Patent No.	Country	Title	File Date
D147-02	139777	Taiwan	具有自對準接觸結構之積體電路電容器的製造方法	10/04/2000
D148-01	6309923	USA	Method of forming the capacitor in DRAM	07/20/2000
D148-02	140597	Taiwan	一種於自動對準接觸窗結構上之電容器的製造方法	07/11/2000
D148-03	180873	China	一種於自動對準接觸窗結構上之電容器的製造方法	09/15/2000
D149-01	6319771	USA	Fabrication process for a lower electrode of a memory capacitor	07/21/2000
D149-02	137194	Taiwan	記憶體之電容器下電極的製造方法	07/03/2000
D149-03	153407	China	記憶體之電容器下電極的製造方法	08/14/2000
D150-01	6340614	USA	Method of forming a DRAM cell	10/03/2000
D150-02	144816	Taiwan	形成動態隨機存取記憶體的方法	01/03/2001
D152-01	6358795	USA	Method of making stacked capacitor in memory device	09/13/2000
D152-02	155256	Taiwan	在記憶體元件中製作堆疊電容器的方法	10/09/2000
D154-01	6440869	USA	Method of forming the capacitor with HSG in DRAM	06/26/2000
D154-02	137419	Taiwan	形成一具有半球型矽晶粒之電容器的方法	06/13/2000
D156-01	6503764	USA	Method of making in high density DRAM circuit having a stacked capacitor	12/12/2001
D156-02	165518	Taiwan	記憶體堆疊式電容器之結構及其製法	11/06/2001
D159-01	087682	Taiwan	電容器的製造方法	02/09/1996
D160-01	088271	Taiwan	四層鰭型電容器結構的製造方法	12/05/1996
D161-01	091196	Taiwan	一種積體電路電容器之電荷儲存電極的製造方法	05/23/1997
D163-01	122064	Taiwan	動態隨機存取記憶體及其製造方法	03/01/1999
D164-01	096122	Taiwan	記憶體積體電路之具有四複晶矽結構之堆疊式電容器之下層電極的製造方法	09/02/1997
D165-01	183272	Taiwan	高密度動態隨機存取記憶體之冠狀電容	03/27/1998
D166-01	130878	Taiwan	一種半導體記憶體電路之電容器的製造方法	03/26/1998
D168-01	135246	Taiwan	一種自行校準動態隨機存取記憶體單元之節狀物結構及其製造方法	01/29/1999
D169-01	128926	Taiwan	動態隨機存取記憶體中電容器之製造方法	08/19/1998
D173-01	118715	Taiwan	堆疊式電容器的製造方法	12/04/1998
D174-01	153093	Taiwan	形成動態隨機存取記憶體的方法	01/17/2001
D175-01	165037	Taiwan	一種動態隨機存取記憶體電路之接觸窗製程	03/23/2001
D176-01	176396	Taiwan	製作高介電常數電容之方法	12/14/2001
D005-01	5554557	USA	Method for fabricating a stacked capacitor with a self aligned node contact in a memory cell	02/02/1996
D005-02	090358	Taiwan	具有自動對準源極接觸窗之堆疊式電容器的製造方法	07/18/1996
D014-01	5648291	USA	Method for fabricating a bit line over a capacitor array of memory cells	06/03/1996
D014-02	090033	Taiwan	於記憶胞之電容陣列上製作位元線之方法	07/09/1996
D014-03	3424200	Japan	於記憶胞之電容陣列上製作位元線之方法	06/03/1997
D014-04	055377	China	於記憶胞之電容陣列上製作位元線之方法	04/24/1997
D021-01	5665623	USA	Method of fabricating totally self-aligned contacts for dynamic random access memory cells	12/27/1995
D021-02	084077	Taiwan	積體電路之自動對準接觸窗的製作方法	07/13/1995

TSMC VIS

Item No.	Patent No.	Country	Title	File Date
D022-01	5668036	USA	Fabrication method of the post structure of the cell for high density DRAM	06/21/1996
D028-01	5677227	USA	Method of fabricating single crown, extendible to triple crown, stacked capacitor structures, using a self-aligned capacitor node contact	09/09/1996
D028-02	5804852	USA	Stacked capacitor DRAM structure featuring a multiple crown shaped polysilicon lower electrode	06/16/1997
D036-01	5710073	USA	Method for forming interconnections and conductors for high density integrated circuits	01/16/1996
D036-02	087752	Taiwan	高密度積體電路之內連線與導體形成方法	03/04/1996
D036-03	3425849	Japan	高密度積體電路之內連線與導體形成方法	06/03/1997
D036-04	058098	China	高密度積體電路之內連線與導體形成方法	04/15/1997
D042-01	5763306	USA	Method of fabricating capacitor over bit line COB structure for a very high density DRAM applications	10/24/1997
D042-02	114060	Taiwan	一種高密度ＤＲＡＭ電容器結構的製造方法	05/12/1998
D042-03	3981205	Japan	一種高密度ＤＲＡＭ電容器結構的製造方法	06/09/1998
D042-04	128431	China	一種高密度ＤＲＡＭ電容器結構的製造方法	05/27/1998
D052-01	5804480	USA	method for forming a DRAM capacitor using HSG-Si technique and oxygen implant	02/28/1997
D052-02	091135	Taiwan	一種利用氧離子佈植技術製造記憶體電容器的方法	12/06/1996
D062-01	5837577	USA	Method for making self-aligned node contacts to bit lines for capacitor-over-bit-line structures on dynamic random access memory (DRAM) devices	04/24/1998
D062-02	107447	Taiwan	在動態隨機存取記憶體元件上之電容器在位元線上結構形成成節點接觸窗自我對準於位元線的方法	06/04/1998
D068-01	5858829	USA	Method for fabricating dynamic random access memory (DRAM) cells with minimum active cell areas using sidewall-spacer bit lines	06/29/1998
D068-02	6008513	USA	Dynamic random access memory (DRAM) cells with minimum active cell areas using sidewall-space bit lines	11/20/1998
D068-03	114016	Taiwan	具有最小儲存格面積的動態隨機存取記憶體單元的製造方法	08/19/1998
D069-01	5858831	USA	Process for fabricating a high performance logic and embedded dram devices on a single semiconductor chip	02/27/1998
D069-02	117019	Taiwan	高效能邏輯與埋入式ＤＲＡＭ記憶元件之製造方法	04/08/1998
D091-01	5926719	USA	Method for fabricating a crown shaped capacitor structure	10/29/1997
D091-02	102749	Taiwan	皇冠型電容結構之製造方法	01/05/1998
D091-03	2944990	Japan	皇冠型電容結構之製造方法	04/30/1998
D091-04	122711	China	皇冠型電容結構之製造方法	05/29/1998
D095-02	103592	Taiwan	高密度動態隨機存取記憶體的埋藏式電容結構及其組裝方法	01/05/1998
D095-03	128747	China	高密度動態隨機存取記憶體的埋藏式電容結構及其組裝方法	05/29/1998
D096-01	5956587	USA	Method for crown type capacitor in dynamic random access memory	02/17/1998
D096-02	114753	Taiwan	動態隨機存取記憶體中之皇冠形電容器的製造方法	04/24/1998
D096-03	3002665	Japan	動態隨機存取記憶體中之皇冠形電容器的製造方法	03/11/1998
D098-01	5976945	USA	Method for fabricating a DRAM cell structure on an SOI wafer incorporating a two dimensional trench capacitor	11/20/1997
D098-02	6171923	USA	Method for fabricating a DRAM cell structure on an SOI wafer	08/23/1999

TSMC VIS

Item No.	Patent No.	Country	Title	File Date
			incorporating a two dimensional trench capacitor	
D098-03	106235	Taiwan	在具有二維溝渠電容的絕緣體上矽之晶圓製造動態隨機存取記憶體結構的方法	02/02/1998
D100-01	6001717	USA	Method of making local interconnections for dynamic random access memory (DRAM) circuits with reduced contact resistance and reduced mask set	02/12/1999
D100-02	122510	Taiwan	降低動態隨機存取記憶體電路中接觸電阻並減少製程光罩數之局部連接線製造方法	04/22/1999
D101-01	6004853	USA	Method to improve uniformity and the critical dimensions of a DRAM gate structure	05/27/1999
D101-02	149881	Taiwan	一種電晶體之閘極及其製作方法	03/26/1999
D124-01	6136661	USA	Method to fabricate capacitor structures with very narrow features using silyated photoresist	06/14/1999
D124-02	137182	Taiwan	使用矽化光阻來製作窄間距之電容器	04/24/2000
D126-01	6150213	USA	Method of forming a cob dram by using self-aligned node and bit line contact plug	07/08/1998
D130-01	6174815	USA	Method for planarizing DRAM cells	10/27/1997
D130-02	125057	Taiwan	動態隨機存取記憶體記憶胞平坦化之方法	07/24/1997
D131-01	6177695	USA	DRAM using oxide plug in bitline contacts during fabrication	10/07/1999
D131-02	6413813	USA	Method for making DRAM using an oxide plug in the bitline contacts during fabrication	09/22/2000
D131-03	117234	Taiwan	於位元線接觸窗製造中使用氧化物插塞之動態隨機存取記憶體及其製造方法	12/21/1998
D135-02	126688	Taiwan	全面平坦化方法	09/15/1999
D136-01	6207491	USA	Method for preventing silicon substrate loss in fabricating semiconductor device	02/25/1999
D136-02	120398	Taiwan	半導體元件製程中防止矽底材流失的方法	02/12/1999
D138-01	6232240	USA	Method for fabricating a capacitor	01/29/1999
D151-01	6344392	USA	Methods of manufacture of crown or stack capacitor with a monolithic fin structure made with a different oxide etching rate in hydrogen fluoride vapor	11/16/1998
D151-02	6476437	USA	Crown or stack capacitor with a monolithic fin structure	06/18/2001
D151-03	6555433	USA	Method of manufacture of a crown or stack capacitor with a monolithic fin structure made with a different oxide etching rate in hydrogen fluoride vapor	06/18/2001
D151-04	123292	Taiwan	一種具有緊密連接鰭狀結構之皇冠式或堆疊式電容結構及其製造方法	04/09/1999
D158-01	6640403	USA	Method for forming a dielectric-constant-enchanced capacitor	05/29/2001
D158-02	174653	Taiwan	高介電常數之電容	03/05/1999
D162-01	134235	Taiwan	氧化層成長之方法	06/02/1998
D167-01	146650	Taiwan	降低場氧化層所導致的接面漏電流之動態隨機存取記憶體及其方法	03/12/1999
D171-01	108387	Taiwan	製造電容器之方法	08/14/1998
D004-01	5547893	USA	method for fabricating an embedded vertical bipolar transistor and a memory cell	12/27/1995
D019-01	5661691	USA	Simple layout low power data line sense amplifier design	05/23/1996

TSMC VIS

Item No.	Patent No.	Country	Title	File Date
D019-02	120220	Taiwan	動態隨機存取記憶體之資料線感測放大裝置	07/16/1996
D024-01	5674773	USA	Method for planarizing high step-height integrated circuit structures	03/15/1996
D024-02	086266	Taiwan	一種改善記憶體之記憶元陣列和周邊電路之高度差的方法	08/23/1995
D024-03	055618	China	一種改善記憶體之記憶元陣列和周邊電路之高度差的方法	04/16/1997
D047-01	5792680	USA	Method of forming a low cost DRAM cell with self aligned twin tub CMOS devices and a pillar shaped capacitor	11/25/1996
D047-02	097372	Taiwan	自動對準雙井區ＣＭＯＳ元件及柱體構形電容之製造方法	04/28/1997
D049-01	5792690	USA	Method of fabricating a DRAM cell with an area equal to four times the used minimum feature	05/15/1997
D049-02	6198121	USA	Method fabricating a DRAM cell with an area equal to four times the used minimum feature	02/12/1998
D049-03	094449	Taiwan	動態隨機存取記憶體結構及其製造方法	07/24/1997
D055-01	5808335	USA	Reduced mask DRAM process	07/14/1997
D055-02	105582	Taiwan	降低微影光罩使用次數之動態隨機存取記憶體製程	11/01/1995
D071-01	5870343	USA	DRAM sensing scheme for eliminating bit-line coupling noise	04/06/1998
D071-02	135579	Taiwan	減少位元線耦合噪音的新動態隨機存取記憶體之感測結構	01/19/1999
D072-01	5872018	USA	Testchip design for process analysis in sub-micron DRAM fabrication	05/05/1997
D072-02	5977558	USA	Testchip design for process analysis in sub-micron DRAM fabrication	12/10/1998
D073-01	5872032	USA	Fabrication method for a DRAM cell with bipolar charge amplification	11/03/1997
D073-02	5998820	USA	Fabrication method and structure for a DRAM cell with bipolar charge amplification	11/24/1998
D073-03	117183	Taiwan	具有雙極性電荷放大之動態隨機存取記憶體單元的結構與製造方法	01/16/1998
D084-01	5909619	USA	Method for forming a DRAM cell and array to store two-bit data	02/04/1998
D084-02	6018177	USA	DRAM cell and array to store two-bit data	02/25/1999
D084-03	130241	Taiwan	動態隨機存取記憶體及其製造方法	07/20/1998
D086-01	5917748	USA	Multi-level DRAM sensing scheme	03/17/1998
D086-02	107449	Taiwan	多位階ＤＲＡＭ感測設計	06/06/1998
D087-01	5920775	USA	Method for forming a storage capacitor within an integrated circuit	02/23/1996
D087-02	076649	Taiwan	具備金屬連線和電容器電極簡併結構之動態隨機存取記憶體的製造方法	07/07/1995
D088-01	5920785	USA	Dram cell and array to store two-bit data having merged stack capacitor and trench capacitor	02/04/1998
D088-02	6184548	USA	DRAM cell and array to store two-bit data having merged stack capacitor and trench capacitor	02/25/1999
D093-01	5933725	USA	Word line resistance reduction method and design for high density memory with relaxed metal pitch	05/27/1998
D093-02	6057573	USA	Design for high density memory with relaxed metal pitch	05/17/1999
D093-03	140693	Taiwan	可放鬆金屬間距的高密度記憶體之字元線阻抗減小之方法及設計	04/21/1999
D094-01	5936898	USA	Bit-line voltage limiting isolation circuit	04/02/1998

TSMC VIS

Item No.	Patent No.	Country	Title	File Date
D094-02	107680	Taiwan	限壓位元線隔離電路	05/12/1998
D102-01	6008084	USA	Method for fabricating low resistance bit line structures, along with bit line structures exhibiting low bit line to bit line coupling capacitance	02/27/1998
D102-02	117483	Taiwan	具有低的位元線對位元線耦合電容之低電阻位元線結構的製造方法	04/17/1998
D102-03	3950547	Japan	具有低的位元線對位元線耦合電容之低電阻位元線結構的製造方法	05/01/1998
D103-01	6008085	USA	Design and a novel process for formation of DRAM bit line and capacitor node contacts	04/01/1998
D103-02	6133599	USA	Design and a novel process for formation of DRAM bit line and capacitor node contacts	11/18/1999
D103-03	135985	Taiwan	動態隨機存取記憶體之製造方法及其結構	06/04/1998
D106-01	6016279	USA	DRAM sensing scheme and isolation circuit	03/30/1998
D121-01	6124165	USA	Method for making openings in a passivation layer over polycide fuses using a single mask while forming reliable tungsten via plugs on DRAMs	05/26/1999
D121-02	123162	Taiwan	在動態隨機接達記憶體電路中形成保險絲的方法	06/15/1999
D125-01	6141285	USA	Power down scheme for regulated sense amplifier power in dram	02/22/2000
D125-02	169269	Taiwan	將動態隨機存取記憶體之讀取放大器電源關閉的方法	02/18/2000
D129-01	6174767	USA	Method of fabrication of capacitor and bit-line at same level for 8F2 DRAM cell with minimum bit-line coupling noise	05/11/1998
D129-02	6373090	USA	Scheme of capacitor and bit-line at same level and its fabrication method for 8F2 DRAM cell with minimum bit-line coupling noise	09/05/2000
D129-03	129914	Taiwan	具有低位元線耦合訊號８Ｆ　動態隨機存取記憶體晶胞之電容器及相同位階位元線之結構及其製造方法	04/20/1999
D132-01	6180453	USA	Method to fabricate a DRAM cell with an area equal to five times the minimum used feature, squared	12/21/1998
D132-02	145200	Taiwan	製造具有最小方形特徵五倍區域之DRAM記憶胞的方法	02/18/2000
D133-01	6184081	USA	Method of fabricating a capacitor under bit line DRAM structure using contact hole liners	10/08/1999
D133-02	139743	Taiwan	使用接觸洞襯層製造位元線下電容器的方法	05/04/2000
D139-01	6249018	USA	Fabrication method to approach the conducting structure of a DRAM cell with straightforward bit line	04/14/1999
D139-02	131778	Taiwan	積體電路之電性傳導結構	04/28/1998
D140-01	6249473	USA	Power down system for regulated internal voltage supply in DRAM	02/21/2000
D140-02	178177	Taiwan	動態隨機存取記憶體中內部電源供給之電源減載系統	02/15/2000
D146-01	6297105	USA	Method of forming asymmetric source/drain for a DRAM cell	06/15/2000
D146-02	139989	Taiwan	DRAM胞之不對稱源極／汲極的製造方法	03/24/2000
D153-01	6380045	USA	Method of forming asymmetric wells for DRAM cells	06/12/2000
D153-02	141346	Taiwan	DRAM胞之不對稱井區的製造方法	03/24/2000
D157-01	6529427	USA	Test structures for measuring DRAM cell node junction leakage current	08/12/1999
D157-02	138138	Taiwan	動態隨機存取記憶體之測試結構及測試方法	10/22/1999

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