

PATENT ASSIGNMENT

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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT
CONVEYING PARTY DATA	
Name	Execution Date
Lucian Shifren	12/20/2010
Pushkar Ranade	01/03/2011
Scott E. Thompson	01/12/2011
Sachin R. Sonkusale	12/20/2010
Weimin Zhang	12/20/2010
RECEIVING PARTY DATA	
Name:	SUVOLTA, INC.
Street Address:	130 Knowles Drive
Internal Address:	Suite D
City:	Los Gatos
State/Country:	CALIFORNIA
Postal Code:	95032
PROPERTY NUMBERS Total: 1	
Property Type	Number
Application Number:	12971884
CORRESPONDENCE DATA	
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<i>Correspondence will be sent via US Mail when the fax attempt is unsuccessful.</i>	
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Email:	judy.baggett@bakerbotts.com
Correspondent Name:	BAKER BOTTS L.L.P.
Address Line 1:	2001 ROSS AVENUE
Address Line 2:	SUITE 600
Address Line 4:	DALLAS, TEXAS 75201-2980
ATTORNEY DOCKET NUMBER:	078023.0360

CH \$40.00 12971884

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**PATENT
 REEL: 025740 FRAME: 0107**

NAME OF SUBMITTER:

Judy Baggett

Total Attachments: 6

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078023.0360
(10-002 US)

ASSIGNMENT

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ASSIGNMENT

WHEREAS, I, the undersigned inventor (or one of the undersigned joint inventors), of residence as listed, having invented certain new and useful improvements as below entitled, for which application for United States Letters Patent is made, said application having been executed on the date set forth below; and

WHEREAS, SUVOLTA, INC. (hereinafter referred to as "Assignee"), a Delaware corporation, with an address of 130 Knowles Drive, Suite D, Los Gatos, California 95032, desires to acquire my entire right, title and interest in and to the invention, and in and to the said application and any Letters Patent that may issue thereon;

NOW, THEREFORE, for and in consideration of One United States Dollar (\$1.00) and other good and valuable consideration, the receipt and sufficiency of which is hereby acknowledged, I assign to Assignee, all right, title and interest in and to said invention and in and to said application and all patents which may be granted therefor, and all provisional, divisions, reissues, continuations, continuations-in-part and extensions thereof; and I hereby authorize and request the Commissioner of Patents and Trademarks to issue all patents for said invention, or patents resulting therefrom, insofar as my interest is concerned, to Assignee.

I also assign to Assignee, all right, title and interest to the invention disclosed in said application throughout the world, including the right to file applications and obtain patents, utility models, industrial models and designs for said invention in its own name throughout the world including all rights to publish cautionary notices reserving ownership of said invention and all rights to register said invention in appropriate registries; and I further agree to execute any and all powers of attorney, applications, assignments, declarations, affidavits, and any other papers in connection therewith necessary to perfect such right, title and interest in Assignee.

I will communicate to Assignee any facts known to me respecting any improvements; and, at the expense of Assignee, I will testify in any legal proceedings, sign all lawful papers, execute all provisional, divisional, continuation, continuation-in-part, reissue and substitute applications, make lawful oaths and declarations, and generally do everything possible to vest title in Assignee and to aid Assignee to obtain and enforce proper protection for said invention in all countries.

This Assignment shall be binding on the parties' successors, assigns and legal representatives.

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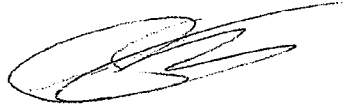
ASSIGNMENT

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Title of Invention:

LOW POWER SEMICONDUCTOR TRANSISTOR
STRUCTURE AND METHOD OF FABRICATION
THEREOF

Signature of Inventor:
Full name of inventor:



Lucian Shifren

Residence:

San Jose, California 95118

Date:

12/20/2010

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Title of Invention:

LOW POWER SEMICONDUCTOR TRANSISTOR
STRUCTURE AND METHOD OF FABRICATION
THEREOF

Signature of Inventor:
Full name of inventor:

P. Ranade
Pushkar Ranade

Residence:

Los Gatos, California 95032

Date:

1-3-2011

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(10-002 US)

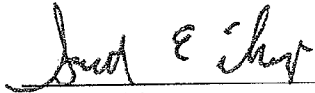
ASSIGNMENT

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Title of Invention:

LOW POWER SEMICONDUCTOR TRANSISTOR
STRUCTURE AND METHOD OF FABRICATION
THEREOF

Signature of Inventor:
Full name of inventor:



Scott E. Thompson

Residence:

Gainesville, Florida 32607

Date:

11/2/2011

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Title of Invention:

LOW POWER SEMICONDUCTOR TRANSISTOR
STRUCTURE AND METHOD OF FABRICATION
THEREOF

Signature of Inventor:
Full name of inventor:



Sachin R. Sonkusale

Residence:

Los Gatos, California 95030

Date:

12 / 20 / 2010

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Title of Invention:

LOW POWER SEMICONDUCTOR TRANSISTOR
STRUCTURE AND METHOD OF FABRICATION
THEREOF

Signature of Inventor:
Full name of inventor:



Weimin Zhang

Residence:

Campbell, California 95008

Date:

Dec. 20, 2010