PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	CORRECTIVE ASSIGNMENT
NATURE OF CONVEYANCE:	Corrective Assignment to correct the execution date of the assignment previously recorded on Reel 025635 Frame 0340. Assignor(s) hereby confirms the assignment.

CONVEYING PARTY DATA

Name	Execution Date
Hewlett-Packard Company	10/19/2010

RECEIVING PARTY DATA

Name:	Samsung Electronics Co., Ltd.
Street Address:	416, Maetan-dong, Yeongtong-gu
City:	Suwon-si, Gyeonggi-do
State/Country:	REPUBLIC OF KOREA

PROPERTY NUMBERS Total: 41

Property Type	Number
Patent Number:	5197058
Patent Number:	5206638
Patent Number:	5428587
Patent Number:	5497281
Patent Number:	5537275
Patent Number:	5555003
Patent Number:	5557485
Patent Number:	5615345
Patent Number:	5644559
Patent Number:	5654529
Patent Number:	5662539
Patent Number:	5680375
Patent Number:	5682096
Patent Number:	5687039
Patent Number:	6061202

OP $1640.00 5197058

Patent Number:	5880456
Patent Number:	5939707
Patent Number:	5909661
Patent Number:	5940361
Patent Number:	5995315
Patent Number:	6020749
Patent Number:	6046969
Patent Number:	6061209
Patent Number:	6075702
Patent Number:	6097594
Patent Number:	6310844
Patent Number:	6141211
Patent Number:	6147505
Patent Number:	6157977
Patent Number:	6178146
Patent Number:	6188538
Patent Number:	6204994
Patent Number:	6215613
Patent Number:	6272103
Patent Number:	6285196
Patent Number:	6351153
Patent Number:	6393596
Patent Number:	6396518
Patent Number:	6518982
Patent Number:	6400382
Patent Number:	6496485

CORRESPONDENCE DATA

Fax Number: (202)315-3758

Correspondence will be sent via US Mail when the fax attempt is unsuccessful.

Phone: 202-429-0020

Email: info@nsiplaw.com

Correspondent Name: North Star Intellectual Property Law, PC

Address Line 1: 1156 15th St, NW Ste # 603

Address Line 4: Washington, DISTRICT OF COLUMBIA 20005

ATTORNEY DOCKET NUMBER:	HP CORRECTIVE ASSIGNMENT

NAME OF SUBMITTER:	Randall S. Svihla

Total Attachments: 46
source=USPTO_EPAS_rcpt_HPtoSEC#page1.tif
source=USPTO_EPAS_rcpt_HPtoSEC#page2.tif
source=USPTO_EPAS_rcpt_HPtoSEC#page3.tif
source=USPTO_EPAS_rcpt_HPtoSEC#page4.tif
source=SamsungHP_Assignment_ExhibitB#page1.tif
source=SamsungHP_Assignment_ExhibitB#page2.tif
source=SamsungHP_Assignment_ExhibitB#page3.tif
source=SamsungHP_Assignment_ExhibitB#page4.tif
source=SamsungHP_Assignment_ExhibitB#page5.tif
source=SamsungHP_Assignment_ExhibitB#page6.tif
source=SamsungHP_Assignment_ExhibitB#page7.tif
source=SamsungHP_Assignment_ExhibitB#page8.tif
source=SamsungHP_Assignment_ExhibitB#page9.tif
source=SamsungHP_Assignment_ExhibitB#page10.tif
source=SamsungHP_Assignment_ExhibitB#page11.tif
source=SamsungHP_Assignment_ExhibitB#page12.tif
source=SamsungHP_Assignment_ExhibitB#page13.tif
source=SamsungHP_Assignment_ExhibitB#page14.tif
source=SamsungHP_Assignment_ExhibitB#page15.tif
source=SamsungHP_Assignment_ExhibitB#page16.tif
source=SamsungHP_Assignment_ExhibitB#page17.tif
source=SamsungHP_Assignment_ExhibitB#page18.tif
source=SamsungHP_Assignment_ExhibitB#page19.tif
source=SamsungHP_Assignment_ExhibitB#page20.tif
source=SamsungHP_Assignment_ExhibitB#page21.tif
source=SamsungHP_Assignment_ExhibitB#page22.tif
source=SamsungHP_Assignment_ExhibitB#page23.tif
source=SamsungHP_Assignment_ExhibitB#page24.tif
source=SamsungHP_Assignment_ExhibitB#page25.tif
source=SamsungHP_Assignment_ExhibitB#page26.tif
source=SamsungHP_Assignment_ExhibitB#page27.tif
source=SamsungHP_Assignment_ExhibitB#page28.tif
source=SamsungHP_Assignment_ExhibitB#page29.tif
source=SamsungHP_Assignment_ExhibitB#page30.tif
source=SamsungHP_Assignment_ExhibitB#page31.tif
source=SamsungHP_Assignment_ExhibitB#page32.tif
source=SamsungHP_Assignment_ExhibitB#page33.tif
source=SamsungHP_Assignment_ExhibitB#page34.tif
source=SamsungHP_Assignment_ExhibitB#page35.tif
source=SamsungHP_Assignment_ExhibitB#page36.tif
source=SamsungHP_Assignment_ExhibitB#page37.tif
source=SamsungHP_Assignment_ExhibitB#page38.tif
source=SamsungHP_Assignment_ExhibitB#page39.tif
source=SamsungHP_Assignment_ExhibitB#page40.tif
source=SamsungHP_Assignment_ExhibitB#page41.tif
source=SamsungHP_Assignment_ExhibitB#page42.tif

United States Patent and Trademark Office

Electronic Patent Assignment System

Confirmation Receipt

< PXUIDVVLJ QP HQWKDVIEHHQIUHFHLYHGIE\IVWHI86372I
7KHIFRYHUVKHHWPRIVWHIDVVLJ QP HQWVMGLVSOD\HGIEHOBZI

PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Hewlett-Packard Company	10/15/2010

RECEIVING PARTY DATA

Name:	Samsung Electronics Co., Ltd.
Street Address:	416, MAETAN-DONG, YEONGTONG-GU
City:	SUWON-SI, GYEONGGI-DO
State/Country:	REPUBLIC OF KOREA

PROPERTY NUMBERS Total: 41

Property Type	Number
Patent Number:	5197058
Patent Number:	5206638
Patent Number:	5428587
Patent Number:	5497281
Patent Number:	5537275
Patent Number:	5555003

Patent Number:	5557485
Patent Number:	5615345
Patent Number:	5644559
Patent Number:	5654529
Patent Number:	5662539
Patent Number:	5680375
Patent Number:	5682096
Patent Number:	5687039
Patent Number:	6061202
Patent Number:	5880456
Patent Number:	5939707
Patent Number:	5909661
Patent Number:	5940361
Patent Number:	5995315
Patent Number:	6020749
Patent Number:	6046969
Patent Number:	6061209
Patent Number:	6075702
Patent Number:	6097594
Patent Number:	6310844
Patent Number:	6141211
Patent Number:	6147505
Patent Number:	6157977
Patent Number:	6178146
Patent Number:	6188538
Patent Number:	6204994
Patent Number:	6215613
Patent Number:	6272103
Patent Number:	6285196
Patent Number:	6351153
Patent Number:	6393596
Patent Number:	6396518
Patent Number:	6518982
Patent Number:	6400382
Patent Number:	6496485

CORRESPONDENCE DATA

Fax Number:	(202)315-3758
Correspondence will be sent via US Mail when the fax attempt is unsuccessful.	
Phone:	202-429-0020
Email:	info@nsiplaw.com
Correspondent Name:	North Star Intellectual Property Law, PC
Address Line 1:	1156 15th St, NW Ste # 603
Address Line 4:	Washington, DISTRICT OF COLUMBIA 20005

ATTORNEY DOCKET NUMBER:	HP ASSIGNMENT
NAME OF SUBMITTER:	Charles Y. Park
Signature:	/Charles Y. Park/
Date:	01/13/2011

Total Attachments: 42
source=SamsungHP_Assignment_ExhibitB#page1.tif
source=SamsungHP_Assignment_ExhibitB#page2.tif
source=SamsungHP_Assignment_ExhibitB#page3.tif
source=SamsungHP_Assignment_ExhibitB#page4.tif
source=SamsungHP_Assignment_ExhibitB#page5.tif
source=SamsungHP_Assignment_ExhibitB#page6.tif
source=SamsungHP_Assignment_ExhibitB#page7.tif
source=SamsungHP_Assignment_ExhibitB#page8.tif
source=SamsungHP_Assignment_ExhibitB#page9.tif
source=SamsungHP_Assignment_ExhibitB#page10.tif
source=SamsungHP_Assignment_ExhibitB#page11.tif
source=SamsungHP_Assignment_ExhibitB#page12.tif
source=SamsungHP_Assignment_ExhibitB#page13.tif
source=SamsungHP_Assignment_ExhibitB#page14.tif
source=SamsungHP_Assignment_ExhibitB#page15.tif
source=SamsungHP_Assignment_ExhibitB#page16.tif
source=SamsungHP_Assignment_ExhibitB#page17.tif
source=SamsungHP_Assignment_ExhibitB#page18.tif
source=SamsungHP_Assignment_ExhibitB#page19.tif
source=SamsungHP_Assignment_ExhibitB#page20.tif
source=SamsungHP_Assignment_ExhibitB#page21.tif
source=SamsungHP_Assignment_ExhibitB#page22.tif
source=SamsungHP_Assignment_ExhibitB#page23.tif
source=SamsungHP_Assignment_ExhibitB#page24.tif
source=SamsungHP_Assignment_ExhibitB#page25.tif
source=SamsungHP_Assignment_ExhibitB#page26.tif
source=SamsungHP_Assignment_ExhibitB#page27.tif
source=SamsungHP_Assignment_ExhibitB#page28.tif
source=SamsungHP_Assignment_ExhibitB#page29.tif
source=SamsungHP_Assignment_ExhibitB#page30.tif
source=SamsungHP_Assignment_ExhibitB#page31.tif
source=SamsungHP_Assignment_ExhibitB#page32.tif
source=SamsungHP_Assignment_ExhibitB#page33.tif
source=SamsungHP_Assignment_ExhibitB#page34.tif
source=SamsungHP_Assignment_ExhibitB#page35.tif
source=SamsungHP_Assignment_ExhibitB#page36.tif

source=SamsungHP_Assignment_ExhibitB#page37.tif
source=SamsungHP_Assignment_ExhibitB#page38.tif
source=SamsungHP_Assignment_ExhibitB#page39.tif
source=SamsungHP_Assignment_ExhibitB#page40.tif
source=SamsungHP_Assignment_ExhibitB#page41.tif
source=SamsungHP_Assignment_ExhibitB#page42.tif

RECEIPT INFORMATION

EPAS ID:	PAT1432778
Receipt Date:	01/13/2011
Fee Amount:	$1640

Return to home page

| .HOME | INDEX| SEARCH | eBUSINESS | CONTACT US | PRIVACY STATEMENT

Exhibit B

ASSIGNMENT OF PATENTS AND PATENT APPLICATIONS

WHEREAS, Hewlett-Packard Development Company, L.P., a limited partnership established and existing under the laws of the State of Texas and having its registered place of business at 20555 S.H. 249 Houston, Texas 77070, U.S.A. and Hewlett-Packard Company, a corporation organized and existing under the laws of the State of Delaware and having its principal place of business at 3000 Hanover Street, Palo Alto, California 94304, U.S.A. (collectively "HP") are the owners of record, either individually or collectively, of the Assigned Patents (as defined below);

WHEREAS, Samsung Electronics Co., Ltd. ("Samsung"), a corporation duly organized and existing under and by virtue of the laws of the Republic of Korea, and having a place of business at 416 Maetan-dong, Yeongtong-gu, Suwon-si, Gyeonggi-do, Republic of Korea, is desirous of acquiring the entire interest in and to the Assigned Patents (as defined below);

WHEREAS, HP and Samsung have entered into a Patent Purchase and Sale Agreement for certain patents and patent applications dated October 14, 2010 ("Purchase and Sale Agreement") wherein HP has agreed to sell and Samsung has agreed to purchase the Assigned Patents subject to all prior encumbrances and licenses;

WHEREAS, Samsung has agreed and covenanted in said Purchase and Sale Agreement to license back to HP certain rights under the Assigned Patents as a condition of and as part of the consideration for the Parties entering into the Purchase and Sale Agreement;

WHEREAS, for the purpose of this Assignment, the following terms, whether in singular or in plural form, when used with a capital initial letter shall have the respective meanings as follows.

"**Affiliate**" means with respect to any person, any other Person that directly, or indirectly through one or more intermediaries, controls, is controlled by, or is under the common control of the Person in question; provided, however, that in any country where the local law or regulation does not permit foreign equity participation of more than fifty percent (50%), an "Affiliate" shall include any Person in which the Person in question owns or controls, directly or indirectly, the maximum percentage of such outstanding stock or voting rights permitted by such local law or regulation. For purposes of the foregoing, "control," including the terms "controlling," "controlled by" and "under common control with," means the possession, direct or indirect, of the power to direct or cause the direction of the management and policies of a Person, whether through the ownership of voting securities, by contract or otherwise.

"**Assigned Patents**" means the issued patents and patent applications listed in Appendix A of this Assignment.

"**Encumbrances**" means any commitments, licenses or other rights relating to any of the Assigned Patents, whether express, implied or otherwise, that are made, entered into or granted by, or that arise from the actions taken by, HP, any current or former Affiliate of HP, or any Person, prior to the Effective Date including, but not limited to, the commitments, licenses and rights described in Sections 5 and 6.1 of the Purchase and Sale Agreement.

"**Person**" means any natural person, corporation, company, partnership, association, sole proprietorship, trust, joint venture, non-profit entity, institute, governmental authority, trust association or other form of entity not specifically listed herein including, without limitation, HP or any of its Affiliates, or Samsung or any of its Affiliates.

NOW, THEREFORE, to all whom it may concern, be it known that for good and valuable consideration to HP in hand paid, the receipt of which is hereby acknowledged, HP has sold, assigned, transferred, and set over, and by these presents does sell, assign, transfer, and set over unto said Samsung, subject to all Encumbrances, its whole right, title, and interest in and to all of the Assigned Patents, said whole right, title, and interest in and to said Assigned Patents including all past, present, and future causes of action and claims for damages derived by reason of patent infringement thereof (to the extent such damages are not already paid, awarded or contractually owed to HP, its Affiliates or any predecessor of HP or HP's Affiliates), for said Samsung's own use and for the use of its assigns, successors, and legal representatives to the full end of the term of each of the Assigned Patents. For clarity, the foregoing assignment does not include (i) any trademarks, trade dress, trade names, or other indicia of origin; (ii) except for inventions of the Assigned Patents, any inventions or discoveries, whether patentable or not, and registrations, invention disclosures, patents and applications therefor; (iii) any trade secrets, confidential information or know-how; (iv) any works of authorship, whether copyrightable or not; and (v) any other intellectual property or proprietary rights of HP, its Affiliates or any predecessor of HP or HP's Affiliates.

HP, for itself, and its heirs, assigns, and legal representatives hereby further covenants to and with Samsung, its assigns, successors, and legal representatives to fully cooperate therewith in perfecting this assignment in the United States and in any and all foreign jurisdictions, said cooperation extending to the Assigned Patents, and including the execution of additional assignments or other formal documents as may be required in connection therewith.

In Testimony Whereof, HP by its fully authorized representatives has executed this Assignment as of the dates indicated below.

HEWLETT-PACKARD DEVELOPMENT COMPANY, L.P.

By: HPQ Holdings, LLC, its General Partner

By: _____ Date: 10/19/10

Bruce H. Watrous, Jr., Manager
HPQ Holdings, LLC

HEWLETT-PACKARD COMPANY

By: _____ Date: October 19, 2010

Susan Goodhue
VP & AGC, Intellectual Property
Hewlett-Packard Company

Appendix A of Exhibit B: List of Assigned Patents

No.	Record ID	Country	Patent No.	Application No.	Title	Status
1	10011561-1	US	US6716737	10/208363	Method Of Forming A Through-substrate Interconnect	GRANTED
2	10012867-1	US	US6727115	10/000008	Back Side Through-Hole Interconnection Of A Die To A Substrate	GRANTED
3	10990689-1	US	US6501663	09/514484	Three-dimensional Interconnect System	GRANTED
4	100110007-1	US	US6902872	10/208163	Method Of Forming A Through-Substrate Interconnect	GRANTED
5	100110007-2	TW	I281227	92105392		GRANTED
6	100110007-5	AU	2003275108	2003275108	Method Of Forming A Through-substrate Interconnect	GRANTED
7	100110007-7	KR		2006-7007397	Method Of Forming A Through-substrate Interconnect	PENDING
8	100110007-8	EP		3759378.7	Method Of Forming A Through-substrate Interconnect	PENDING
9	100202067-1	US	US6790775	10/286060	Method Of Forming A Through-Substrate Interconnect	GRANTED
10	100202067-2	JP		P2003-361648	Method Of Forming A Through-substrate Interconnect	PENDING
11	200602928-1	US	US7566657	11/654338	Methods Of Forming Through-substrate Interconnects	GRANTED
12	200602928-5	JP		2009-546414	Methods Of Forming Through-substrate Interconnects	PENDING
13	200602928-6	KR		10-2009-7015077	Methods Of Forming Through-substrate Interconnects	PENDING
14	1092561-1	US	US5941983	08/881244	Out-Of-Order Execution ing Encoded Dependencies Between Instructions In Queues To Determine Stall Values That Control Issuance Of Instructions From The Queues	GRANTED
15	1092563-5	US	US5596733	08/361874	System For Exception Recovery ing A Conditional Substitution Instruction Which Inserts A Replacement Result In The Destination Of The Excepting Instruction (as Amended)	GRANTED
16	10951104-1	US	US6105123	09/038364	A High Speed Register File Organization For A Pipelined Computer Architecture	GRANTED
17	10970100-1	US	US5930508	08/871128	Method For Storing And Instructions For A Microprocessor Having A Plurality Of Function Units	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
18	90960017-2	US	US5859975	08/695266	Parallel Processing Computer System Having Share Coherent Memory And Interconnections Utilizing Separate Unidirectional Request & Response Lines For Direct Communication Or ing Crossbar Switching Device (amd	GRANTED
19	200301895-1	US	US6633967	09/652985	COHERENT TRANSLATION LOOK-ASIDE BUFFER	GRANTED
20	200302972-2	US	US5721836	08/741643	METHOD AND APPARAT FOR SENSING AND CHANGING THE STATE OF A COMPUTER BEFORE CONNECTING THE COMPUTER TO OR DISCONNECTING THE COMPUTER FROM AN EXPANSION UNIT	GRANTED
21	200304918-1	US	US6408401	09/191679	EMBEDDED SRAM ARCHITECTURE WITH BUILT-IN SELF-TEST AND BUILT-IN SELF-REPAIR WITH SPARE ROWS AND COLUMNS	GRANTED
22	200304972-1	US	US6397302	09/099304	METHOD AND APPARAT FOR DEVELOPING MULTIPROCESSOR CACHE CONTROL PROTOCOLS BY PRESENTING A CLEAN VICTIM SIGNAL TO AN EXTERNAL SYSTEM	GRANTED
23	200307180-1	US	US5164916	07/861276	HIGH-DENSITY DOUBLE-SIDED MULTI-STRING MEMORY MODULE WITH RESISTOR FOR INSERTION DETECTION	GRANTED
24	10004618-1	US	US6955767	09/815913	Scanning Probe Based Lithographic Alignment	GRANTED
25	10004618-4	EP		2725318.6	Scanning Probe Based Lithographic Alignment	PENDING
26	10007140-1	US	US6743368	10/062952	Nano-Size Imprinting Stamp ing Spacer Technique	GRANTED
27	10007140-2	JP	4005927	P2003-018275	Nano-size Imprinting Stamp Using Spacer Technique	GRANTED
28	10007140-3	CN	ZL03103150.1	3103150.1	Nano-size Imprinting Stamp Using Spacer Technique	GRANTED
29	10007140-5	DE	60307336	3250633.9	Nano-size Imprinting Stamp Using Spacer Technique	GRANTED
30	10007140-6	FR	1333324	3250633.9	Nano-size Imprinting Stamp Using Spacer Technique	GRANTED
31	10990800-1	US	US6294450	09/516989	Nanoscale Patterning For The Formation Of Extensive Wires	GRANTED
32	10990800-3	US	US6407443	09/886355	Nanoscale Patterning For The Formation Of Extensive Wires	GRANTED
33	10990800-5	KR	10-744884	2002-7011346	Nanoscale Patterning For The Formation Of Extensive Wires	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
34	10990800-7	SG	91109	200204946.8	Nanoscale Patterning For The Formation Of Extensive Wires	GRANTED
35	100110197-1	US	US7445742	10/642371	Imprinting Nanoscale Patterns For Catalysis And Fuel Cell	GRANTED
36	100201082-1	US	US6759180	10/133772	Method Of Fabricating Sub-lithographic Size Line And Space Patterns For Nano Imprinting Lithography	GRANTED
37	100201083-1	US	US6673714	10/133605	Method Of Fabricating A Sub-lithographic Sized Via	GRANTED
38	100201083-5	DE	60301295.7	3252512.3	Method Of Fabricating A Sub-lithographic Sized Via	GRANTED
39	100201083-6	GB	1359609	3252512.3	Method Of Fabricating A Sub-lithographic Sized Via	GRANTED
40	100204967-1	US	US7654816	10/960731	Lithographic Mask Alignment	GRANTED
41	100204967-4	JP	4564537	P2007-535728	Lithographic Mask Alignment	PENDING
42	200209573-1	US	US7060625	10/766710	Imprint Stamp	GRANTED
43	200401445-1	US	US7641468	10/931672	Imprint Lithography Apparat And Method Employing An Effective Pressure	GRANTED
44	200401445-2	TW		94126045	Imprint Lithography Apparatus And Method Employing An Effective Pressure	PENDING
45	200401860-1	US	US7766640	11/203551	Contact Lithography Apparat, System And Method	GRANTED
46	200401860-3	TW		95128664	Contact Lithography Apparatus, System And Method	PENDING
47	200402463-1	US	US7329115	11/061226	Patterning Nanoline Arrays With Spatially Varying Pitch	GRANTED
48	200405511-1	US	US7400665	11/084886	A Nano-vcsel Device And Fabrication Thereof ing Nano-colonnades	GRANTED
49	200406191-1	US	US7449776	11/126430	Cooling Devices That e Nanowires	GRANTED
50	200406625-1	US	US7507293	11/096669	Photonic Crystals With Nanowire-based Fabrication	GRANTED
51	200503568-1	US	US7734084	11/584074	Method And System For Offset Estimation And Alignment	GRANTED
52	200507163-1	US	US7618752	11/548975	Defomation-based Contact Lithography Systems, Apparat And Methods	GRANTED
53	10010899-1	US	US6969667	10/114392	Electrical Device And Method Of Making	GRANTED
54	200308162-1	US	US5990520	08/795159	METHOD FOR FABRICATING A HIGH PERFORMANCE VERTICAL BIPOLAR NPN OR PNP TRANSISTOR HAVING LOW BASE RESISTANCE IN A STANDARD CMOS PROCESS	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
55	200311911-1	US	US7067355	10/854110	Package Having Bond-sealed Underbump	GRANTED
56	200311911-2	US	US7443017	11/447764	Package Having Bond-sealed Underbump	GRANTED
57	200315285-1	US	US7026189	10/776084	Wafer Packaging And Singulation Method	GRANTED
58	200315285-2	TW		93124540	Wafer Packaging And Singulation Method	PENDING
59	200315285-4	US	US7196410	11/340321	Wafer Packaging And Singulation Method	GRANTED
60	200315285-5	DE		112005000276.4	Wafer Packaging And Singulation Method	PENDING
61	200315285-6	GB	2425890	616223.4	Wafer Packaging And Singulation Method	GRANTED
62	200315285-7	JP		P2006-553293	Wafer Packaging And Singulation Method	PENDING
63	200404323-2	US	US7262498	11/038374	Assembly With A Ring And Bonding Pads Formed Of A Same Material On A Substrate (as Amended)	GRANTED
64	200404323-3	TW		94132292	Assembly	PENDING
65	200405286-1	US	US7682934	11/011640	WAFER PACKAGING AND SINGULATION METHOD	GRANTED
66	200405701-1	US	US7045885	11/008542	Improved Placement Of Absorbing Material In A Semiconductor Device	GRANTED
67	200405701-2	US	US7442576	11/276875	Improved Placement Of Absorbing Material In A Semiconductor Device	GRANTED
68	10001454-1	US	US6647487	09/506972	Apparat And Method For Shift Register Rate Control Of Microprocessor Instruction Prefetches (as Amended)	GRANTED
69	10001454-2	JP	4195778	P2001-041237	Apparatus And Method For Rate Control Of Microprocessor Instruction Prefetches	GRANTED
70	10001690-1	US	US6643766	09/565017	Speculative Pre-Fetching Additional Line On Cache Miss If No Request Pending In Out-of-order Processor (amended)	GRANTED
71	10001690-2	FR	2808902	105866	Speculative Pre-fetch Of Data In An Out-of-order Execution Processor System	GRANTED
72	10002761-1	US	US6725369	09/560192	A Circuit For Allwoing Data Return In Dual-Data Formats	GRANTED
73	10004882-1	US	US6745299	09/988121	Method For Evaluation Of Scalable Symmetric Multiple Processor Cache Coherency Protocols And Algorithms	GRANTED
74	10960757-2	US	US6009539	08/756594	Cross-Triggering CP For Enhanced Test Operations In A Multi-CPU Computer System	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
75	10960758-2	US	US5956477	08/753454	Method For Processing Information In A Microprocessor To Facilitate Debug And Performance Monitoring	GRANTED
76	10961302-1	US	US5905663	08/867452	A Minimal Circuit For Detecting Loss Of Precision In Floating Point Numbers	GRANTED
77	10961408-1	US	US5951656	08/792329	Method And System For Controlling Queue Deletions In Which Pointer Corresponding To Item To Be Deleted Is Moved Back And Pointers For Items After Deleted Item Are Shifted (as Amemded)	GRANTED
78	10961410-1	US	US5958072	08/782964	Computer-System Process-To-Memory-B Interface Having Repeating -Test-Event Generation Hardware	GRANTED
79	10961411-1	US	US5907853	08/783918	e Of Partial Duplicate Cache Tags For A Processor Cache	GRANTED
80	10970529-1	US	US5991893	08/921275	Virtually Reliable Shared Memory	GRANTED
81	10971189-1	US	US6643762	09/490392	Processing System And Method Utilizing A Scoreboard To Detect Data Hazards Between Instructions Of Computer Programs (as Amended)	GRANTED
82	200301595-2	US	US6002851	08/790030	METHOD AND APPARAT FOR NODE PRUNING A MULTI-PROCESSOR SYSTEM FOR MAXIMAL, FULL CONNECTION DURING RECOVERY	GRANTED
83	200301840-1	US	US6671822	09/651948	METHOD AND SYSTEM FOR ABSORBING DEFECTS IN HIGH PERFORMANCE MICROPROCESSOR WITH A LARGE N-WAY SET ASSOCIATIVE CACHE	GRANTED
84	200302357-1	US	US6687799	10/061552	Expedited Memory Dumping And Reloading Of Computer Processors	GRANTED
85	200303421-1	US	US5944809	08/699921	METHOD AND APPARAT FOR DISTRIBUTING INTERRUPTS IN A SYMMETRIC MULTIPROCESSOR SYSTEM	GRANTED
86	200303769-1	US	US6009524	08/920810	METHOD FOR THE SECURE REMOTE FLASHING OF A BIOS MEMORY (As Amended)	GRANTED
87	200304558-1	US	US5924122	08/818757	METHOD FOR ERROR RECOVERY SPINLOCK IN ASYMMETRICALLY ACCESSED MULTIPROCESSOR SHARED MEMORY	GRANTED
88	200304572-2	US	US6009514	09/183734	COMPUTER METHOD AND APPARAT FOR ANALYZING PROGRAM INSTRUCTIONS EXECUTING IN A COMPUTER SYSTEM	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
89	200304782-1	US	US5924120	09/018320	METHOD AND APPARAT FOR MAXIMIZING UTILIZATION OF AN INTERNAL PROCESSOR B IN THE CONTEXT OF EXTERNAL TRANSACTIONS RUNNING AT SPEEDS FRACTIONALLY GREATER THAN INTERNAL TRANSACTION TIMES	GRANTED
90	200304796-1	US	US6704856	09/465175	Method For Compacting An Instruction Queue	GRANTED
91	200308160-1	US	US6018756	09/041905	REDUCED-LATENCY FLOATING-POINT PIPELINE ING NORMALIZATION SHIFTS OF BOTH OPERANDS	GRANTED
92	1094045-1	US	US5974534	08/194899	Predecoding And Steering Mechanism For Instructions IN A Superscalar Processor	GRANTED
93	1094045-2	JP	3670043	PH07-013533	Predecoding And Steering Mechanism For Instruction In A Superscalar Processor	GRANTED
94	1094045-5	DE	69510966.9	95300682.2	Steering Of Instructions In A Computer System	GRANTED
95	10961023-3	US	US5930822	08/720330	Method And System For Maintaining Strong Ordering In A Coherent Memory System	GRANTED
96	10961407-3	US	US5978886	08/785371	Method And Apparat For Duplicating Tag Systems To Maintain Addresses Of CPU Data Stored In Write Buffers External To A Cache	GRANTED
97	10971191-1	US	US6622238	09/490395	System And Method For Providing Predicate Data To Multiple Pipeline Stages (as Amended)	GRANTED
98	10971191-3	US	US7213132	10/648960	System And Method For Providing Predicate Data To Multiple Pipeline Stages (as Amended)	GRANTED
99	10971193-3	US	US6651164	09/418286	System And Method For Detecting An Erroneo Data Hazard Between Instructions Of An Instruction Group And Resulting From A Compiler Grouping Error (as Amended)	GRANTED
100	10971262-1	US	US6591360	09/484138	Local Stall/Hazard Detect In Superscalar, Pipelined Microprocessor	GRANTED
101	10971338-1	US	US6618802	09/390199	Superscalar Processing System And Method For Efficiently Performing In-Order Processing Of Instructions (amended)	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
102	10971350-3	US	US6711670	09/417582	System And Method For Detecting Data Hazards Within An Instruction Group Of A Compiled Computer Program	GRANTED
103	200301624-1	US	US5915088	08/761116	INTERPROCESSOR MESSAGING SYSTEM	GRANTED
104	200301761-1	US	US6591345	09/723825	METHOD FOR ENSURING MAXIMUM BANDWIDTH ON ACCESSES TO STRIDED VECTORS IN A BANK INTERLEAVED CACHE	GRANTED
105	200304588-1	US	US6055605	08/957544	TECHNIQUE FOR REDUCING LATENCY OF INTER-REFERENCE ORDERING IN A MULTIPROCESSOR SYSTEM HAVING SHARED CACHES (COMBINED WITH PD96-0162)	GRANTED
106	10007793-1	US	US6534850	09/836061	Electronic Device Sealed Under Vacuum Containing A Getter And Method Of Operation	GRANTED
107	10007793-4	US	US7042075	10/328261	Electronic Device Sealed Under Vacuum Containing A Getter And Method Of Operation	GRANTED
108	100204047-1	US	US7045958	10/413048	VACUUM DEVICE HAVING A GETTER	GRANTED
109	100204047-2	US	US7608998	11/387222	VACUUM DEVICE HAVING A GETTER	GRANTED
110	200209439-1	US	US7508132	10/689819	Device Having A Getter Structure And A Photomask	GRANTED
111	200300117-1	US	US7005335	10/620858	Array Of Nanoscopic Mosfet Transistors And Fabrication Methods	GRANTED
112	200300117-2	TW	I320971	93102411	Array Of Nanoscopic Mosfet Transistors And Fabrication Methods	GRANTED
113	200300117-4	US	US20050219936	11/126710	Array Of Nanoscopic Mosfet Transistors And Fabrication Methods	PENDING
114	200300117-5	CN	200480020106.2	200480020106.2	Array Of Nanoscopic Mosfet Transistors And Fabrication (as Amended By ISA)	GRANTED
115	200300117-6	EP		4777187.8	Array Of Nanoscopic Mosfet Transistors And Fabrication (as Amended By ISA)	PENDING
116	200310116-1	US	US7009268	10/828334	Wheatstone Bridge Scheme For Sensor	GRANTED
117	200310116-2	EP		5252231.5	Wheatstone Bridge Scheme For Sensor	PENDING
118	200310831-1	US	US6988924	10/412918	METHOD OF MAKING A GETTER STRUCTURE	GRANTED
119	200311658-1	US	US7655152	10/832640	Etching	GRANTED
120	200312224-1	US	US7247531	10/835659	Field-effect-transistor Multiplexing/demultiplexing Architectures And Methods Of Forming The Same	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
121	200312224-2	EP		5006937.6	Field-effect-transistor Multiplexing/demultiplexing Architectures And Methods Of Forming The Same	PENDING
122	200312224-3	JP	4467460	P2005-128913	Field-effect-transistor Multiplexing/demultiplexing Architectures And Methods Of Forming The Same	GRANTED
123	200312224-4	TW		94110482	Field-Effect-Transistor Multiplexing/Demultiplexing Architectures And Methods Of Forming The Same	PENDING
124	200312224-5	US	US7633098	11/765374	Field-effect-transistor Multiplexing/demultiplexing Architectures And Methods Of Forming The Same	GRANTED
125	200312500-1	US	US7183215	10/895733	Etching With Electrostatically Attracted Ions	GRANTED
126	200312500-2	TW		94120576	Etching With Electrostatically Attracted Ions	PENDING
127	200312500-4	DE		112005001713.3	Etching With Electrostatically Attracted Ions	PENDING
128	200312500-5	GB	2431129	703252.7	Etching With Electrostatically Attracted Ions	GRANTED
129	200312500-6	JP		P2007-522529	Etching With Electrostatically Attracted Ions	PENDING
130	200401845-1	US	US7374968	11/046107	METHOD OF UTILIZING A CONTACT PRINTING STAMP	GRANTED
131	200406672-1	US	US7491595	11/176033	CREATING HIGH VOLTAGE FETS WITH LOW VOLTAGE PROCESS	GRANTED
132	200406672-3	US	US7704819	12/350102	Creating High Voltage FETs with Low Voltage Process	GRANTED
133	10002316-1	US	US6782616	09/759952	Connection Arrangements For Electrical Devices	GRANTED
134	10002316-2	US	US6916182	10/792264	Connection Arrangements For Electrical Devices Having A Ledge On Which Contact Terminals Are Provided (As Amended)	GRANTED
135	10011959-1	US	US6662663	10/120944	A Pressure Sensor And Method Of Making The Same	GRANTED
136	10011959-5	US	US7004034	10/666609	A Pressure Sensor And Method Of Making The Same Having Membranes Forming A Capacitor	GRANTED
137	10019534-1	US	US7404981	10/420565	Printing Electronic And Opto-electronic Circuits	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
138	10991070-1	US	US6152790	09/422813	A Bifurcated Contact With A Connecting Member That Can Add Redundant Contact Points To Single Point Connectors	GRANTED
139	100200445-1	US	US6989684	10/309967	System For And Method Of Assessing Chip Acceptability And Increasing Yield	GRANTED
140	100202599-1	US	US6937039	10/447693	Improved Tip And Tip Assembly For Signal Probe	GRANTED
141	200205327-1	US	US6970001	10/370537	Variable Impedance Test Probe	GRANTED
142	200210076-6	US	US7393712	11/350662	Fluidic MEMS Device	GRANTED
143	200309427-1	US	US7536781	10/455862	Method And System For Applying Target Load To An Application Specific Integrated Circuit (ASIC) Assembly With Attach Hardware	GRANTED
144	200309566-1	US	US7323358	10/639853	Method And System For Sizing A Load Plate	GRANTED
145	200310196-1	US	US7332263	10/830508	A Method For Patterning An Organic Light Emitting Diode Device	GRANTED
146	200400344-1	US	US7345302	10/945756	E-FIELD POLARIZED MATERIALS	GRANTED
147	200402755-1	US	US7314772	11/080113	PHOTONIC DEVICE	GRANTED
148	200403753-1	US	US7309642	11/271354	Metallic Quantum Dots Fabricated By A Superlattice Structure	GRANTED
149	200404235-1	US	US7358169	11/105262	Laser-assisted Deposition	GRANTED
150	200504734-1	US	US7381631	11/174798	e Of Expanding Material Oxides For Nano-fabrication	GRANTED
151	10001410-1	US	US6654712	09/507508	Method To Reduce Skew In Clock Signal Distribution ing Balanced Wire Widths	GRANTED
152	10001410-2	GB	2365178	102443.9	Method To Reduce Skew In Clock Signal Distribution Using Balanced Wire Widths	GRANTED
153	10001410-3	GB	2395325	403622.4	Method To Reduce Skew In Clock Signal Distribution Using Balanced Wire Widths	GRANTED
154	10002478-1	US	US6611936	09/560191	Programmable Delay Elements For Source Synchrono Link Function Design Verification Through Simulation	GRANTED
155	10002814-1	US	US6571357	09/563006	High Speed Device Emulation Computer System Tester	GRANTED
156	10960765-2	US	US6003107	08/707936	Circuitry For Providing External Access To Signals That Are Internal To An Integrated Circuit Chip Package	GRANTED
157	10961412-1	US	US5994918	08/924720	Zero Delay Regenerative Circuit For Noise Supression On A Computer Data B	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
158	10970126-2	US	US6012836	08/760550	Method Of Reducing Boolean Complements In Code Generated By A Circuit Compiler	GRANTED
159	10970552-1	US	US6061819	08/999099	Generation Of Reproducible Random Initial States In RTL Simulators (As Amended)	GRANTED
160	10970805-2	US	US5959631	08/919630	Hardware And Software For The Visualization Of Three-Dimensional Data Sets	GRANTED
161	10971159-1	US	US6742011	09/504984	Apparat And Method For Increasing Performance Of Multipliers Utilizing Regular Summation Circuitry	GRANTED
162	10971278-1	US	US6708193	09/510274	Linear Summation Multiplier Array Implementation For Both Signed And Unsigned Multiplication	GRANTED
163	10971278-2	DE	10105945	10105945	Linear Summation Multiplier Array Implementation For Both Signed And Unsigned Multiplication	GRANTED
164	10971375-1	US	US6077717	09/237425	Sytem And Method For Detecting NOR Gates And NAND Gates	GRANTED
165	10980769-1	US	US6041092	09/183311	Digital Circuit To Count Like Signals In A Data Word	GRANTED
166	10982043-1	US	US6564178	09/290806	A Method And Apparat For Evaluating Processors For Architectural Compliance	GRANTED
167	200304794-1	US	US6606587	09/291721	METHOD AND APPARAT FOR ESTIMATING ELMORE DELAYS WITHIN CIRCUIT DESIGNS	GRANTED
168	200307428-3	US	US5978571	08/854419	METHOD AND APPARAT FOR SYNCRONO CIRCUIT DESIGN BY ELIMINATING UNNEEDED TIMING BEHAVIORS PRIOR TO SIMULATION RUN-TIME	GRANTED
169	200308246-1	US	US6654713	09/447019	METHOD TO COMPRESS A PIECEWISE LINEAR WAVEFORM SO COMPRESSION ERROR OCCURS ON ONLY ONE SIDE OF THE WAVEFORM	GRANTED
170	200500547-1	US	US7250800	11/179400	Clock Pulse Width Control Circuit	GRANTED
171	1094630-4	US	US6000047	09/023665	Scanning Memory Device And Error Correction Method	GRANTED
172	10004120-1	US	US6678811	09/827768	Memory Controller With 1x/MX Write Capability	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
173	10004120-3	US	US7103790	10/695881	Memory Controller Driver Circuitry Having A Multiplexing Stage To Provide Data To At Least N-1 Of N Data Propagation Circuits, And Having Output Merging Circuitry To Alternately Couple The N Data Propagation Circuits To A Data Pad To Generate Either A 1x	GRANTED
174	10950179-5	US	US6000019	08/841187	SDRAM Data Allocation System And Method Utilizing Dual Bank Storage And Retrieval	GRANTED
175	10951091-3	US	US6069496	09/207303	CMOS Circuit Techniques For Improved Switching Speed Of Single-Ended And Differential Dynamic Logic (As Amended)	GRANTED
176	10960395-1	US	US6041393	08/704218	Array Padding For Higher Memory Throughput In The Presence Of Dirty Misses	GRANTED
177	10961397-3	US	US6718375	08/797674	ing Local Storage To Handle Multiple Outstanding Requests In A SCI System	GRANTED
178	10971069-1	US	US5986923	09/073670	A Method And Apparat For Improving Read/Write Stability Of A Single-Port SRAM Cell (as Amended)	GRANTED
179	10971422-1	US	US6704820	09/507033	Unified Cache Port Consolidation	GRANTED
180	10990358-1	US	US6728843	09/451499	System And Method For Tracking And Processing Parallel Coherent Memory Access	GRANTED
181	100204296-3	US	US7328378	11/507272	Repair Techniques For Memory With Multiple Redundancy	GRANTED
182	200303672-1	US	US5986880	08/876730	ELECTRONIC APPARAT HAVING I/O BOARD WITH CABLE-FREE REDUNDANT ADAPTER CARDS THEREON	GRANTED
183	200303837-1	US	US6073206	09/070866	A METHOD FOR FLASHING ESCD AND VARIABLES INTO A ROM	GRANTED
184	200303837-2	US	US6505278	09/571467	A METHOD FOR FLASHING ESCD AND VARIABLES INTO A ROM	GRANTED
185	200303837-3	US	US6754793	10/320147	METHOD FOR FLASHING ESCD AND VARIABLES INTO A ROM	GRANTED
186	200308332-1	US	US6647466	09/769552	METHOD AND APPARAT FOR ADAPTIVELY BYPASSING ONE OR MORE LEVELS OF A CACHE HIERARCHY	GRANTED
187	200312648-1	US	US7296136	10/861710	Methods And Systems For Loading Data From Memory	GRANTED
188	10002028-1	US	US6567817	09/657552	A Cache Management System ing Hashing	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
189	10011538-1	US	US6745307	10/001075	Method And System For Privilege-Level-Access To Memory Within A Computer	GRANTED
190	10960151-1	US	US5995967	08/734003	Forming Linked Lists ing Content Addressable Memory	GRANTED
191	10960151-3	US	US6820086	09/336046	Forming Linked Lists ing Content Addressable Memory	GRANTED
192	10961300-1	US	US5933643	08/837422	Enhancement Of Data Prefetching By ing A Sampling-Oriented Execution Profiler	GRANTED
193	10980969-2	US	US6604116	09/282115	Decreasing Memory Return Latency By Predicting The Order Of Completion Of Partially Ready Returns	GRANTED
194	200301893-1	US	US6665776	09/755719	APPARAT AND METHOD FOR SPECULATIVE PREFETCHING AFTER DATA CACHE MISSES	GRANTED
195	200303035-1	US	US5634073		System having a plurality of posting queues associated with different types of write operations for selectively checking one queue based upon type of read operation	EXPIRED
196	200303035-2	US	US5938739	08/811587	MEMORY CONTROLLER INCLUDING WRITE POSTING QUEUES B READ CONTROL LOGIC, AND A DATA CONTENTS COUNTER	GRANTED
197	200303121-2	US	US6009500	08/950327	REPLACEMENT OF ERRONEO FIRMWARE IN A REDUNDANT NON-VOLATILE MEMORY SYSTEM (AS AMENDED)	GRANTED
198	200304711-1	US	US5996055	08/979738	METHOD FOR RECLAIMING PHYSICAL PAGES OF MEMORY WHILE MAINTAINING AN EVEN DISTRIBUTION OF CACHE PAGE ADDRESSES WITHIN AN ADDRESS SPACE	GRANTED
199	200304712-1	US	US6026475	08/978932	METHOD FOR DYNAMICALLY REMAPPING A VIRTUAL ADDRESS TO A PHYSICAL ADDRESS TO MAINTAIN AN EVEN DISTRIBUTION OF CACHE PAGE ADDRESSES IN A VIRTUAL ADDRESS SPACE	GRANTED
200	200304800-1	US	US6016529	08/978940	MEMORY ALLOCATION TECHNIQUE FOR MAINTAINING AN EVEN DISTRIBUTION OF CACHE PAGE ADDRESSES WITHIN A DATA STRUCTURE	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
201	200304904-1	US	US6405304	09/138957	METHOD FOR MAPPING INSTRUCTIONS ING A SET OF VALID AND INVALID LOGICAL TO PHYSICAL REGISTER ASSIGNMENTS INDICATED BY BITS OF A VALID VECTOR TOGETHER WITH A LOGICAL REGISTER LIST (As Amended)	GRANTED
202	200307460-3	US	US5966737	08/971630	APPARAT AND METHOD FOR SERIALIZED SET PREDICTION	GRANTED
203	200307889-2	US	US5933860	08/902487	MULTIPROBE INSTRUCTION CACHE WITH INSTRUCTION-BASED PROBE HINT GENERATION AND TRAINING WHEREBY THE CACHE BANK OR WAY TO BE ACCESSED NEXT IS PREDICTED	GRANTED
204	200900653-1	US	US5923877	08/641466	Object-oriented Programming Memory Management Framework And Method	GRANTED
205	10001937-1	US	US6310495	09/504598	Clock Wave Noise Reducer	GRANTED
206	10002401-1	US	US6247137	09/553737	Delaying Clock And Data Signals To Force Synchrono Operation In Digital Systems That Determine Phase Relationships Between Clocks With Related Frequencies	GRANTED
207	10004507-1	US	US6380779	09/903927	An Edge-Triggered, Self-Resetting Pulse Generator	GRANTED
208	10950673-1	US	US5739715	08/551221	Digital Signal Driver Circuit Having A High Slew Rate (as Amended)	GRANTED
209	10951073-1	US	US5659259	08/631100	Circuit And Method Of Sensing Small Voltage Changes On Highly Capacitively Loaded Electronic Signals	GRANTED
210	10951074-1	US	US5698998	08/635250	A Fast Low Power Differential Sense Amplifier	GRANTED
211	10971295-1	US	US6292093	09/507862	A Multi-Bit Comparator	GRANTED
212	200206865-2	US	US7173496	11/266863	On-chip Variable Oscillator Method And Apparat	GRANTED
213	200207014-1	US	US7019367	10/655640	Integrated Circuit	GRANTED
214	200300297-1	US	US6930932	10/650071	Data Signal Reception Latch Control ing Clock Aligned Relative To Strobe Signal	GRANTED
215	200301517-1	US	US5371417	08/087556	MULTIPLE FREQUENCY OUTPUT CLOCK GENERATOR SYSTEM	GRANTED
216	200301517-2	US	US5461332	08/289823	MULTIPLE FREQUENCY OUTPUT CLOCK GENERATOR SYSTEM	GRANTED
217	200301517-3	US	US5491442	08/442851	MULTIPLE FREQUENCY OUTPUT CLOCK GENERATOR SYSTEM	GRANTED
218	200301517-4	US	US5539328	08/449450	TERMINATION FOR HIGH FREQUENCY CLOCK DISTRIBUTION PATH	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
219	200302111-1	US	US5281861	07/855453	SINE WAVE CLOCK DISTRIBUTION WITH HIGH VOLTAGE OUTPUT	GRANTED
220	200302111-2	US	US5656961	08/135086	SINE WAVE CLOCK DISTRIBUTION WITH HIGH VOLTAGE OUTPUT	GRANTED
221	200305048-1	US	US6367025	09/241000	PASS-GATE INPUTS THAT TEMPORARILY HOLD STAGE ON A HIGH INPUT IMPEDANCE, STROBED CMOS DIFFERENTIAL SENSE AMPLIFIER	GRANTED
222	200307264-1	US	US5680644	08/331780	LOW DELAY MEANS FOR COMMUNICATING BETWEEN SYSTEMS ON DIFFERENT CLOCKS	GRANTED
223	1092086-1	US	US5302461	07/894398	Dielectric Films For e In Magnetoresistive Transducers	GRANTED
224	1093748-1	US	US5506527	08/227935	Low Power Diode (As Amended)	GRANTED
225	1094194-1	US	US5519581	08/327072	Mounting Of Toroidal Inductors	GRANTED
226	10007343-1	US	US6777172	09/917650	Method And Apparat For ing An Excimer Laser To Pattern Electrodeposited Photoresist	GRANTED
227	10960582-1	US	US5825625	08/728394	Heat Conductive Substrate Mounted In PC Board Hole For Transferring Heat From IC To Heat Sink	GRANTED
228	10981054-1	US	US6118670	09/107662	PCB Mounting Arrangement For Two Components Requiring High-Speed Connections To A Third Component	GRANTED
229	191239-3	US	US5555003	08/417183	Method For Selecting An Item On A Graphics Screen	GRANTED
230	1094430-1	US	US5654529	08/433771	Styl-Input Computing System With Erasure	GRANTED
231	1094430-2	JP	3786464	PH08-082365	Method For Erasing Images And Styles-Based Electronic	GRANTED
232	1094430-4	DE	741353	96302193.6	A Pen Eraser For A Pen-Based Computing Device	GRANTED
233	1094430-5	GB	741353	96302193.6	A Pen Eraser For A Pen-Based Computing Device	GRANTED
234	1094430-6	FR	741353	96302193.6	A Pen Eraser For A Pen-Based Computing Device	GRANTED
235	1094430-7	IT	741353	96302193.6	A Pen Eraser For A Pen-Based Computing Device	GRANTED
236	10980462-5	US	US6396518	09/130869	Appliance And Method Of ing Same Having A Send Capability For Stored Data	GRANTED
237	10980462-7	US	US6518982	09/894555	System And Method Of Selecting Pages That An Appliance Is Sending	GRANTED
238	10980743-1	US	US6400382	09/170507	Apparat And Method For A Shortcut Link Creation System In A Computer System	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
239	30011900-2	GB	2376123	201632.7	Facilitation Of Speech Recognition In User Interface	GRANTED
240	30011900-3	US	US6912500	10/058046	Facilitation Of Speech Recognition In er Interface	GRANTED
241	200306320-2	US	US5557729	07/874750	APPLICATION DESIGN INTERFACE ENHANCEMENT	GRANTED
242	200307524-1	US	US5499330	08/123403	DOCUMENT DISPLAY SYSTEM FOR ORGANIZING AND DISPLAYING DOCUMENTS AS SCREEN OBJECTS ORGANIZED ALONG STRAND PATHS	GRANTED
243	200307524-2	US	US5621874		Three dimensional document representation using strands	EXPIRED
244	200307524-3	US	US5905992	08/756207	DOCUMENT DISPLAY SYSTEM FOR ORGANIZING AND DISPLAYING DOCUMENTS AS SCREEN OBJECTS ORGANIZED ALONG STRAND PATHS	GRANTED
245	10003438-1	US	US6789151	09/810965	DIP Switch Configuration For Increased ability With Multiple Cards	GRANTED
246	10012713-1	US	US6931464	09/984281	Method For Connecting Gigabit Interface Converters With Serial Identification Capability Into An Active Two-Wire Serial B	GRANTED
247	10012920-1	US	US6653863	10/108082	Method And Apparat For Improving B Capacity	GRANTED
248	10012920-2	US	US6833733	10/651422	Apparat For Improving B Capacity	GRANTED
249	10013123-1	US	US6944695	10/107725	Method And Apparat For Connecting Devices To A B	GRANTED
250	10981948-1	US	US6157977	09/198833	B Bridge And Method For Ordering Read And Write Operations In A Write Posting System	GRANTED
251	10981948-2	JP	3696012	PH11-331526	Bus Bridge And Method For Ordering Read And Write Operations In A Write Posting System	GRANTED
252	10990528-1	US	US6496485	09/332796	Method Of Loop Breaking Tree Identification In A System B Hierarchy	GRANTED
253	200301543-1	US	US5536176	08/248805	FLEXIBLE B ROUTING STRUCTURE	GRANTED
254	200303213-1	US	US5748911	08/684710	SERIAL B SYSTEM FOR SHADOWING REGISTERS	GRANTED
255	200303213-2	US	US6108729	09/073135	SERIAL B FOR SHADOWING REGISTERS	GRANTED
256	200303755-1	US	US6199131	08/995699	COMPUTER SYSTEM EMPLOYING OPTIMIZED DELAYED TRANSACTION ARBITRATION TECHNIQUE	GRANTED
257	200303755-2	US	US6212590	09/042038	COMPUTER SYSTEM EMPLOYING OPTIMIZED DELAYED TRANSACTION ARBITRATION TECHNIQUE	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
258	200304200-1	US	US6067596	09/153821	FLEXIBLE PLACEMENT OF GTL END POINTS ING DOUBLE TERMINATION POINTS	GRANTED
259	200307981-1	US	US5625802	08/353754	APPARAT AND METHOD FOR ADAPTING A COMPUTER SYSTEM TO DIFFERENT ARCHITECTURES	GRANTED
260	200308083-1	US	US6075704	08/884777	INPUT/OUTPUT B SYSTEM IN A TOWER BUILDING BLOCK SYSTEM	GRANTED
261	10961174-2	US	US5951696	08/748760	Debug System With Hardware Breakpoint Trap	GRANTED
262	10970840-1	US	US6094730	08/958291	A Hardware-Assisted Firmware Tracing Method And Apparat	GRANTED
263	10980753-1	US	US6253344	09/182715	System And Method For Testing A Microprocessor With An Onboard Test Vector Generator	GRANTED
264	10980753-3	US	US6378097	09/672536	System And Method For Testing A Microprocessor With An Onboard Test Vector Generator	GRANTED
265	10992435-1	US	US6643800	09/496367	Method And Apparat For Testing Microarchitectural Features By ing Tests Written In Microcode	GRANTED
266	10992627-1	US	US6625759	09/502366	Method And Apparat For Verifying The Fine-Grained Correctness Of A Behavioral Model Of A Central Processor Unit	GRANTED
267	200307940-1	US	US5680544	08/523297	METHOD FOR TESTING AN ON-CHIP CACHE FOR REPAIR	GRANTED
268	10003899-1	US	US7127433	09/974103	Method For Generating Pay-per-page Pricing Data For Managed Printer Services	GRANTED
269	60006751-2	US	US7222368	10/056117	Mechanism For Controlling If/when Material Can Be Printed On A Specific Printer	GRANTED
270	600200961-1	US	US7191237	10/271519	Automatic Registration Of Receiving Device On A Remote Printing Application	GRANTED
271	10007413-1	US	US6725207	09/841512	Media Selection ing A Neural Network	GRANTED
272	10013459-1	US	US6745934	10/236423	Sequential Device Start-Up Guide	GRANTED
273	10014403-1	US	US6698750	10/339991	Media Tray Refill Shuttle	GRANTED
274	10980993-1	US	US7034951	09/568779	Printer Collator Facility And Method	GRANTED
275	10990090-1	US	US6542892	09/288048	Configuring A Client For A Printer ing Electronic Mail	GRANTED
276	10991677-1	US	US6614454	09/430383	Scheme For Presentation Of Multiple Print-job Modification Elements In A Printing Software er-interface	GRANTED
277	200501569-1	US	US7025260	11/118202	Method And System For Permitting Limited e Of An Imaging Device	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
278	10003812-1	US	US6867132	10/245897	Large Line Conductive Pads For Interconection Of Stackable Circuitry	GRANTED
279	10003812-7	US	US6864576	10/696992	Large Line Conductive Pads For Interconection Of Stackable Circuitry	GRANTED
280	10011771-1	US	US6599796	09/896480	Apparat And Fabrication Process To Reduce Crosstalk In Pirm Memory Array	GRANTED
281	10014491-1	US	US6887792	10/244862	Embossed Mask Lithography	GRANTED
282	10014491-7	US	US7304364	10/885842	Embossed Mask Lithography	GRANTED
283	10002319-1	US	US6791931	09/811299	Accelerometer ing Field Emitter Technology	GRANTED
284	10003488-1	US	US6928042	09/900662	Data Storage Device Including Nanotube Electron Sources	GRANTED
285	10003488-5	US	US7295503	11/136882	Data Storage Device Including Nanotube Electron Sources	GRANTED
286	10007269-1	US	US6700853	09/910530	Data Storage Devices With Wafer Alignment Compensation	GRANTED
287	10007269-2	US	US6987722	10/695566	Data Storage Devices With Wafer Alignment Compensation	GRANTED
288	90960008-1	US	US5560027	08/167663	Scalable Parallel Processing Systems Wherein Each Hypernode Has Plural Processing Modules Interconnected By Crossbar And Each Processing Module Has SCI Circuitry For Forming Multi-Dimensional	GRANTED
289	90960017-1	US	US5577204	08/168531	Parallel Processing Computer System Interconnections Utilizing Unidirectional Communication Links With Separate Request And Response Lines For Direct Communication Or ing Crossbar Switching Device	GRANTED
290	200301954-1	US	US6920516	09/944516	Anti-Starvation Interrupt Protocol	GRANTED
291	200304844-1	US	US6175814	08/977438	APPARAT FOR DETERMINING THE INSTANTANEO AVERAGE NUMBER OF INSTRUCTIONS PROCESSED	GRANTED
292	200305803-3	US	US5590293	08/425683	DYNAMIC MICROBRANCHING WITH PROGRAMMABLE HOLD ON CONDITION, TO PROGRAMMABLE DYNAMIC MICROBRANCHING DELAY MINIMIZATION	GRANTED
293	200306219-4	US	US5251227	07/852509	RESETS FOR A FAULT TOLERANT, DUAL ZONE COMPUTER SYSTEM	GRANTED
294	200306520-4	US	US5341491	08/141427	APPARAT AND METHOD FOR ENSURING THAT LOCK REQUESTS ARE SERVICED IN A MULTIPROCESSOR SYSTEM	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
295	200308013-1	US	US6167503	08/552517	REGISTER AND INSTRUCTION CONTROLLER FOR SUPERSCALAR PROCESSOR	GRANTED
296	100200991-1	US	US7342675	10/281672	Systems And Methods For Improved Operation And Troubleshooting Of A Printing Device	GRANTED
297	100200991-3	GB	2395828	325040.4	Systems And Methods For Improved Operation And Troubleshooting Of A Printing Device	GRANTED
298	200312601-2	US	US7422384	10/912330	A System And A Method For Printing Small Print Jobs	GRANTED
299	200314465-1	US	US7443520	10/837962	Imaging Device Configuration Pages	GRANTED
300	10990897-1	US	US6327157	09/405935	High-Current Power Bus System	GRANTED
301	200302267-1	US	US6904534	09/968416	PROGRESSIVE CPU SLEEP STATE DUTY CYCLE TO LIMIT PEAK POWER OF MULTIPLE COMPUTERS ON SHARED POWER DISTRIBUTION UNIT	GRANTED
302	200302557-1	US	US6944687	10/126059	Reducing Power Consumption Of An Electronic System Having A Communication Device (revised). (as Filed Per Application Uploaded From Alecto.)	GRANTED
303	200303566-1	US	US5745358	08/775558	VARIABLE FREQUENCY CONVERTER WITH CONSTANT PROGRAMMED DELAY	GRANTED
304	200303567-1	US	US5745359	08/777848	VARIABLE-INPUT-VOLTAGE CONVERTER WITH DELAY PROPORTIONAL TO Vin Vout	GRANTED
305	200304078-1	US	US6934772	09/164527	LOWERING DISPLAY POWER CONSUMPTION BY DITHERING BRIGHTNESS	GRANTED
306	200314071-1	US	US7073078	10/734855	Power Control Unit That Provides One Of A Plurality Of Voltages On A Common Power Rail	GRANTED
307	10003593-1	US	US6541309	09/815844	Fabricating A Molecular Electronic Device Having A Protective Barrier Layer	GRANTED
308	10003593-3	US	US6724016	10/365946	Fabricating A Molecular Electronic Device Having A Protective Barrier Layer	GRANTED
309	10003762-1	US	US6707063	09/815922	Passivation Layer For Molecular Electronic Device Fabrication	GRANTED
310	10003762-3	US	US6835575	10/402642	Passivation Layer For Molecular Electronic Device Fabrication	GRANTED
311	10004741-1	US	US6925555	09/915531	Optimization Of Clock Scheduling For A Synchronous System	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
312	10014071-1	US	US6931607	10/282342	System And Method For Designing Dynamic Circuits In A SOI Process	GRANTED
313	10980715-3	US	US6300822	09/104921	On Chip CMOS VLSI Reference Voltage With Feedback For Hysteresis Noise Margin	GRANTED
314	10992466-1	US	US6687862	09/663307	Apparatus And Method For Fast Memory Fault Analysis	GRANTED
315	10992768-1	US	US6314039	09/578968	Characterization Of Sense Amplifiers	GRANTED
316	100111692-1	US	US6903386	10/172213	Transistor With Means For Providing A Non-Silicon-Based Emitter (as Amended)	GRANTED
317	100111692-2	US	US6984554	10/666434	Transistor With Group III/VI Emitter	GRANTED
318	100200217-1	US	US6629002	10/138455	Semiconductor Automation Markup Language Based Gem/secs Development Application	GRANTED
319	100200396-1	US	US6922822	10/199668	Verifying Proximity Of Ground Vias To Signal Vias In An Integrated Circuit	GRANTED
320	100200571-1	US	US6804137	10/461632	Data Storage Medium Having Layers Acting As Transistor	GRANTED
321	100200963-1	US	US6936496	10/326708	Nanowire Filament	GRANTED
322	100200963-2	JP	4041063	P2003-422583	Nanowire Filament	GRANTED
323	200205297-1	US	US6907589	10/368988	System And Method For Evaluating Vias Per Pad In A Package Design	GRANTED
324	200205304-1	US	US6938230	10/368778	System And Method For Evaluating Signal Trace Discontinuities In A Package Design	GRANTED
325	200205553-1	US	US6826112	10/347723	A Low Power Logic Gate	GRANTED
326	200207611-1	US	US6983434	10/366489	Differential Via Pair Impedance Adjustment Tool	GRANTED
327	200207612-1	US	US6983433	10/366208	Differential Line Pair Impedance Adjustment Tool	GRANTED
328	200207613-1	US	US6971077	10/366135	Signal Line Impedance Adjustment Tool	GRANTED
329	200207614-1	US	US6889367	10/366205	Differential Via Pair Impedance Verification Tool	GRANTED
330	200207615-1	US	US6968522	10/366134	Differential Line Pair Impedance Verification Tool	GRANTED
331	200208031-1	US	US6993056	10/387480	Hetero Laser And Light-Emitting Source Of Polarized Radiation	GRANTED
332	200301360-2	US	US5546406	08/507737	A CELL ARCHITECTURE FOR BUILT-IN SELF-TEST OF APPLICATION..	GRANTED
333	200302614-1	US	US6975136	10/393191	Isolated Channel In An Integrated Circuit	GRANTED
334	200304860-2	US	US6352913	09/286185	DAMASCENE PROCESS FOR MOSFET FABRICATION	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
335	200305090-1	US	US6369998	09/300016	ELECTROSTATIC DISCHARGE PROTECTION CLAMP FOR NOMINAL-VOLTAGE POWER SUPPLY OR I/O WITH HIGH-VOLTAGE REFERENCE	GRANTED
336	200307243-2	US	US5629840	08/218877	HIGH POWERED DIE WITH BUS BARS	GRANTED
337	200308123-5	US	US7062850	10/681843	A Method Of Forming Electrical Interconnects Having Electromigration-Inhibiting Segments To A Critical Length (Amended)	GRANTED
338	200308249-1	US	US6356427	09/300129	ELECTROSTATIC DISCHARGE PROTECTION CLAMP FOR HIGH VOLTAGE POWER SUPPLY OR I/O WITH HIGH VOLTAGE REFERENCE	GRANTED
339	200308250-1	US	US6268993	09/349269	ELECTROSTATIC DISCHARGE PROTECTION CLAMP FOR HIGH-VOLTAGE POWER SUPPLY OR I/O WITH NOMINAL-VOLTAGE REFERENCE	GRANTED
340	200308251-1	US	US6320735	09/404981	ELECTROSTATIC DISCHARGE PROTECTION CLAMP FOR NOMINAL-VOLTAGE POWER SUPPLY OR I/O WITH HIGH-VOLTAGE REFERENCE AND NON-RELIANCE ON SNAPBACK	GRANTED
341	200312588-1	US	US6858466	10/700713	A System And A Method For Fluid Filling Wafer Level Packages	GRANTED
342	10951093-1	US	US5689228	08/731632	Parallel Magnitude Comparison Using Manchester Carry Chains	GRANTED
343	10971160-1	US	US6381624	09/301830	Faster Multiply/Accumulator	GRANTED
344	10990471-1	US	US6892294	09/497533	Identifying Execution Ready Instructions And Allocating Ports Associated With Execution Resources In An Out-of-order Process (as Amended)	GRANTED
345	10990471-2	JP	4405095	P2001-023626	Find-instructions-and-allocate-ports (FIAP) Circuit And Method For An Out Of Order Processor	GRANTED
346	200301510-1	US	US5435001	08/088562	METHOD OF STATE DETERMINATION IN LOCK-STEPPED PROCESSORS SYSTEM	GRANTED
347	200301510-25	SE	636973	94304669.8	PROCESSOR INTERFACE CHIP FOR DUAL-MICROPROCESSOR SYSTEM	GRANTED
348	200301955-2	US	US7142998	10/655321	Clock Skew Measurement Circuit On A Microprocessor Die	GRANTED
349	200304477-1	US	US6314156	09/517369	SPACE EFFICIENT MULTI-CYCLE BARREL SHIFTER CIRCUIT	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
350	200304777-1	US	US6249855	09/089474	ARBITER SYSTEM FOR CENTRAL PROCESSING UNIT HAVING DUAL DOMINOED ENCODERS FOR FOUR INSTRUCTION ISSUE PER MACHINE CYCLE	GRANTED
351	200304929-1	US	US6317772	09/234021	A SPLIT REMAINDER DIVIDER	GRANTED
352	200305007-1	US	US6366942	09/281501	METHOD AND APPARATUS FOR ROUNDING FLOATING POINT RESULTS IN A DIGITAL PROCESSING SYSTEM	GRANTED
353	200306486-2	US	US6240508	08/505810	PIPELINED COMPUTER WITH SYNCHRONIZATION COUNTER TO ENFORCE MEMORY ORDERING	GRANTED
354	200307818-2	US	US5742537	08/833310	FAST DETERMINATION OF FLOATING POINT STICKY BIT FROM INPUT OPERANDS	GRANTED
355	200307819-1	US	US5729485	08/526255	FAST DETERMINATION OF CARRY INPUTS FROM LOWER ORDER PRODUCT FOR RADIX-8 ODD/EVEN MULTIPLIER ARRAY	GRANTED
356	200307819-2	US	US6131107	09/208169	FAST DETERMINATION OF CARRY INPUTS FROM LOWER ORDER PRODUCT FOR RADIX-8 ODD/EVEN MULTIPLIER ARRAY	GRANTED
357	200307819-3	US	US5889692	08/938951	FAST DETERMINATION OF CARRY INPUTS FROM LOWER ORDER PRODUCT FOR RADIX-8 ODD/EVEN MULTIPLIER ARRAY	GRANTED
358	100111495-1	US	US6770353	10/341651	Co-Deposited Films With Nano-Columnar Structures And Formation Process	GRANTED
359	100201346-1	US	US6762094	10/256984	Nanometer-scale Semiconductor Devices And Method Of Making	GRANTED
360	100201346-2	EP		3255355.4	Nanometer-scale Semiconductor Devices And Method Of Making	PENDING
361	100201346-3	TW	I318453	92123806	Nanometer-scale Semiconductor Devices And Method Of Making	GRANTED
362	100201346-4	JP	4431340	P2003-293392	Nanometer-scale Semiconductor Devices And Method Of Making	GRANTED
363	200209412-1	US	US6921670	10/603434	Nanostructure Fabrication Using Microbial Mandrel	GRANTED
364	200209412-2	JP	4156569	P2004-186206	Nanostructure Fabrication Using Microbial Mandrel	GRANTED
365	200209412-3	TW	I314915	92135812	Nanostructure Fabrication Using Microbial Mandrel	GRANTED
366	200209412-5	DE	60317489.2	3029781.6	Nanostructure Fabrication Using Microbial Mandrel	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
367	200209412-6	FR	1491493	3029781.6	Nanostructure Fabrication Using Microbial Mandrel	GRANTED
368	200209412-7	GB	1491493	3029781.6	Nanostructure Fabrication Using Microbial Mandrel	GRANTED
369	200209412-8	NL	1491493	3029781.6	Nanostructure Fabrication Using Microbial Mandrel	GRANTED
370	200308777-1	US	US7205675	10/353632	MICRO-FABRICATED DEVICE WITH THERMOELECTRIC DEVICE AND METHOD OF MAKING	GRANTED
371	200308777-2	JP	4030967	P2004-018551	MICRO-FABRICATED DEVICE WITH THERMOELECTRIC DEVICE AND METHOD OF MAKING	GRANTED
372	200308777-3	TW	I303238	92123598	MICRO-FABRICATED DEVICE WITH THERMOELECTRIC DEVICE AND METHOD OF MAKING	GRANTED
373	200308777-4	EP		3020338.4	MICRO-FABRICATED DEVICE WITH THERMOELECTRIC DEVICE AND METHOD OF MAKING	PENDING
374	200309766-1	US	US7371331	10/817135	A Method Of Creating A Patterned Monolayer On A Surface	GRANTED
375	200309766-2	EP		5252015.2	A Method Of Creating A Patterned Monolayer On A Surface	PENDING
376	200309766-3	JP	4044940	P2005-105676	A Method Of Creating A Patterned Monolayer On A Surface	GRANTED
377	200309766-4	TW		94110278	A Method Of Creating A Patterned Monolayer On A Surface	PENDING
378	200309781-1	US	US7597814	10/807873	STRUCTURE FORMED WITH TEMPLATE HAVING NANOSCALE FEATURES	GRANTED
379	200309781-2	EP		5251732.3	STRUCTURE FORMED WITH TEMPLATE HAVING NANOSCALE FEATURES	PENDING
380	200309781-4	TW		94107555	STRUCTURE FORMED WITH TEMPLATE HAVING NANOSCALE FEATURES	PENDING
381	200309781-5	JP		P2008-132877	STRUCTURE FORMED WITH TEMPLATE HAVING NANOSCALE FEATURES	PENDING
382	200309813-1	US	US7223611	10/683527	Fabrication Of Nanowires	GRANTED
383	200309813-2	TW		93110116	Fabrication Of Nanowires	PENDING
384	200309813-4	CN		200480035875.X	Fabrication Of Nanowires	PENDING
385	200309813-5	DE		112004001881.1	Fabrication Of Nanowires	PENDING
386	200309813-6	GB	2422378	608358.8	Fabrication Of Nanowires	GRANTED
387	200309813-8	US	US7375368	11/582002	Superlattice For Fabricating Nanowires	GRANTED
388	200310640-1	US	US7132298	10/744516	Fabrication Of Nano-object Array	GRANTED
389	200310640-3	JP		P2004-372613	Fabrication Of Nano-object Array	PENDING
390	200310640-4	TW		93119042	Fabrication Of Nano-object Array	PENDING
391	200310640-5	HK	1073643	5106127.8	Fabrication Of Nano-object Array	GRANTED
392	200310640-6	US	US20070020773	11/457776	Fabrication Of Nano-object Array	PENDING
393	200310640-7	DE	602004013265.9	4258019.1	Fabrication Of Nano-object Array	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
394	200310640-8	FR	1547970	4258019.1	Fabrication Of Nano-object Array	GRANTED
395	200310640-9	GB	1547970	4258019.1	Fabrication Of Nano-object Array	GRANTED
396	200310640-10	IT	1547970	4258019.1	Fabrication Of Nano-object Array	GRANTED
397	200311571-1	US	US7407738	10/817729	Fabrication And Use Of Superlattice	GRANTED
398	200311571-2	TW		94110480	Fabrication And Use Of Superlattice	PENDING
399	200311571-4	CN	ZL200580017198.3	200580017198.3	Fabrication And Use Of Superlattice	GRANTED
400	200311571-6	JP		P2007-506321	Fabrication And Use Of Superlattice	PENDING
401	200311571-7	DE	602005021082.2	5763773.8	Fabrication And Use Of Superlattice	GRANTED
402	200311571-8	FR	1735820	5763773.8	Fabrication And Use Of Superlattice	GRANTED
403	200311571-9	GB	1735820	5763773.8	Fabrication And Use Of Superlattice	GRANTED
404	200311571-10	NL	1735820	5763773.8	Fabrication And Use Of Superlattice	GRANTED
405	200403969-1	US	US7375012	11/068363	MULTILAYER FILM	GRANTED
406	200403969-3	EP		6735682.4	MULTILAYER FILM	PENDING
407	200403969-4	US	US20090126977	12/104252	MULTILAYER FILM	PENDING
408	200408463-1	US	US7276424	11/169470	Fabrication Of Aligned Nanowire Lattices	GRANTED
409	200408463-3	US	US7727855	11/842818	Fabrication Of Aligned Nanowire Lattices	GRANTED
410	100202794-1	US	US6734709	10/383127	Method And System For Performing Sampling On The Fly Using Minimum Cycle Delay Synchronization	GRANTED
411	200206538-1	US	US6683483	10/280472	Clock Pulse Width Control Circuit	GRANTED
412	200301550-1	US	US6029263	08/268370	INTERCONNECT TESTING USING NON-COMPATIBLE SCAN ARCHITECTURES	GRANTED
413	200304905-1	US	US6658506	09/292051	METHOD AND APPARATUS FOR PERFORMING TIMING VERIFICATION OF A CIRCUIT	GRANTED
414	10007763-1	US	US6753544	09/846047	Silicon-Based Dielectric Tunneling Emitter	GRANTED
415	10007763-9	US	US6902458	10/755890	Silicon-Based Dielectric Tunneling Emitter	GRANTED
416	10007794-1	US	US6781146	09/846127	Annealed Tunneling Emitter (As Amended)	GRANTED
417	10007794-10	US	US7044823	10/848695	Annealed Tunneling Emitter (As Amended)	GRANTED
418	10011192-1	US	US6558968	10/002422	Method Of Making An Emitter With Variable Density Photoresist Layer (Amended)	GRANTED
419	10011192-7	US	US6806488	10/389556	Method Of Making An Emitter With Variable Density Photoresist Layer (Amended)	GRANTED
420	10012326-1	US	US6787792	10/126426	Emitter With Filled Zeolite Emission Layer	GRANTED
421	10012326-4	US	US6783418	10/758801	Emitter With Filled Zeolite Emission Layer	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
422	10013431-1	US	US7170223	10/197722	Emitter With Dielectric Layer Having Implanted Conducting Centers	GRANTED
423	10013802-1	US	US6852554	10/085866	Emission Layer Formed By Rapid Thermal Formation Process	GRANTED
424	10017974-4	US	US6933517	10/686965	Method Of Manufacturing An Emitter (as Amended)	GRANTED
425	10017974-5	US	US7049158	10/688731	Method Of Manufacturing An Emitter (as Amended)	GRANTED
426	10019410-1	US	US6835947	10/066158	Emitter And Method Of Making	GRANTED
427	10019410-4	US	US7118982	10/935795	Emitter And Method Of Making	GRANTED
428	200206011-1	US	US6841794	10/369365	Dielectric Emitter With PN Junction	GRANTED
429	200209446-1	US	US6954297	10/387245	Micro-mirror Device Including Dielectrophoretic Liquid	GRANTED
430	200311844-2	US	US7301688	10/995690	MIRROR DEVICE FOR PROJECTION SYSTEM HAVING PLURALITY OF TILTABLE MIRRORS TILTED	GRANTED
431	200312474-2	US	US7079301	11/092410	MEMS Device And Method Of Forming MEMS Device	GRANTED
432	200315475-1	US	US6999228	10/793977	Micro Mirror Device With Adjacently Suspended Spring And Method For The Same	GRANTED
433	200402524-2	US	US7320899	10/977278	MICRO-DISPLAYS AND THEIR MANUFACTURE	GRANTED
434	200407092-1	US	US7019887	11/101820	Light Modulator Device	GRANTED
435	1093580-1	US	US5340997	08/124328	A Vacuum Transistor For Flat Panel Displays	GRANTED
436	10004629-1	US	US6628052	09/972430	Enhanced Electron Field Emitter Spindt Tip And Method For Fabricating Enhanced Spindt Tips	GRANTED
437	10004629-4	US	US6817916	10/622909	Enhanced Electron Field Emitter Spindt Tip And Method For Fabricating Enhanced Spindt Tips	GRANTED
438	10006492-1	US	US6648710	09/880160	Method For Low-Temperature Sharpening Of Silicon-Based Field Emitter Tips	GRANTED
439	10006517-1	US	US6607415	09/880158	Method For FabricatingTiny Field Emitter Tips	GRANTED
440	10012050-1	US	US6741016	09/882933	Focusing Lens For Electron Emitter	GRANTED
441	10015150-1	US	US6758711	09/881981	Integrated Focusing Emitter	GRANTED
442	10015150-9	US	US7148621	10/825754	Integrated Focusing Emitter	GRANTED
443	10017974-1	US	US6703252	10/066149	Method Of Manufacturing An Emitter (as Amended)	GRANTED
444	100110944-1	US	US6822379	10/262808	Emission Device And Method For Forming	GRANTED
445	100201223-1	US	US6822241	10/264599	Emitter Device With Focusing Columns	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
446	200209320-1	US	US6891185	10/603445	Electronic Device With Aperture And Wide Lens For Small Emission Spot Size	GRANTED
447	389023-2	US	US5206638	07/647591	Method And Apparatus For Exchanging Data Within A Digital Communications System	GRANTED
448	10018377-1	US	US6914597	09/978279	System For Bi-directional Video Signal Transmission	GRANTED
449	200301589-1	US	US5687372	08/478058	CUSTOMER INFORMATION CONTROL SYSTEM AND METHOD WITH TRANSACTION SERIALIZATION CONTROL FUNCTIONS IN A LOOSELY COUPLED PARALLEL PROCESSING ENVIRONMENT	GRANTED
450	200303820-1	US	US5644593	08/300490	HIGH PERFORMANCE COMMUNICATIONS INTERFACE	GRANTED
451	200303820-2	US	US5729573	08/461506	HIGH PERFORMANCE COMMUNICATIONS INTERFACE	GRANTED
452	200303820-3	US	US6067318	08/866930	HIGH PERFORMANCE COMMUNICATIONS INTERFACE	GRANTED
453	200304630-1	US	US6279062	09/221906	SYSTEM FOR REDUCING DATA TRANSMISSION BETWEEN COPROCESSORS IN A VIDEO COMPRESSION/DECOMPRESSION ENVIRONMENT BY DETERMINING LOGICAL DATA ELEMENTS OF NON-ZERO VALUE AND RETRIEVING SUBSET OF THE LOGICAL DATA ELEMENTS	GRANTED
454	1094037-4	US	US5537275	08/434627	Lead Screw Positioning Mechanism With Each End Of The Lead Screw Self-Aligning And Tiltable (as Amended)	GRANTED
455	1094810-4	US	US6061202	08/906632	Tape Chassis With Integrated Isolation Mounting Features	GRANTED
456	10002957-3	US	US7163175	11/231053	Irregular Surfaced Tape Guide	GRANTED
457	10950094-1	US	US6215613	08/534149	Cartridge Tape Door Opening Apparatus For Use With Tape Cartridges Having Differing Size Formats	GRANTED
458	10950096-1	US	US5557485	08/414972	Alignment And Latching Mechanism In A Drive For Magnetic Data Tape Mini Cartridges	GRANTED
459	10950234-3	US	US6204994	08/767997	Door Opener For Magnetic Tape Data Cartridge	GRANTED
460	10970324-1	US	US5995315	08/853241	Servo System For Following A Magnetic Track Having Identifying Pulse Widths	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
461	10970659-4	US	US5939707	09/154937	Circuit For Lateral Photoeffect Position Sensor	GRANTED
462	10970659-5	US	US5880456	08/853242	Circuit For Lateral Photoeffect Position Sensor	GRANTED
463	10971718-1	US	US6188538	09/100438	Retry Off-Track Positioning Table (Amended)	GRANTED
464	10980675-1	US	US6061209	09/069477	Positioning System For A Magnetic Head For A Tape Drive	GRANTED
465	10981111-2	US	US6097594	09/296092	Recessed Bezel For Tape Drive	GRANTED
466	10003232-1	US	US6752525	09/670467	Light Emitting Device Providing A Collimated Light Beam	GRANTED
467	10003232-2	US	US6916112	10/612865	Light Emitting Device Providing A Collimated Light Beam	GRANTED
468	10950181-1	US	US5644559	08/368465	Flip Latch Assembly For Media Autochanger	GRANTED
469	10950602-1	US	US5662539	08/491440	Tensioning Device For A Flexible Drive Member	GRANTED
470	10950232-1	US	US5673068	08/482157	End-Of-Travel Detection Sensor And Method Of Calibrating Confined Pointing Device	GRANTED
471	10970957-1	US	US5978928	08/953280	Relative Logarithmic Time Stamps For Reduced Memory Map Size	GRANTED
472	10981205-1	US	US6292876	09/249494	Method For Providing Access Protection For SCSI Storage Devices	GRANTED
473	30960008-5	US	US6035415	08/930032	SES Sender 1	GRANTED
474	30960009-5	US	US6023772	08/913933	Fault-tolerant Processing Method	GRANTED
475	200302988-1	US	US5664139	08/243364	METHOD FOR ALLOCATING HIGH MEMORY IN A PERSONAL COMPUTER	GRANTED
476	200303053-3	US	US5797003	08/911346	QUICK ACCESS TO COMPUTER APPLICATIONS	GRANTED
477	200306468-4	US	US5452433	08/386610	COMMON AGENT COMPUTER MANGAGEMENT SYSTEM AND METHOD	GRANTED
478	200307099-1	US	US5428761	07/849887	SYSTEM FOR ACHIEVING ATOMIC NON-SEQUENTIAL MULTI-WORD OPERATIONS IN SHARED MEMORY	GRANTED
479	200307340-2	US	US5588112	08/603968	DMA CONTROLLER FOR MEMORY SCRUBBING	GRANTED
480	189277-1	US	US5197058	07/664881	Electronic Offset Compensation Of The Continuous Composite T Error Signal In Optical Recording	GRANTED
481	10001895-1	US	US6693860	09/692309	Timing Signal Recovery By Superheterodyne Phase Locked Loop	GRANTED
482	10003458-1	US	US6351153	09/698100	Phase Detector With High Precision	GRANTED
483	10960228-5	US	US6310844	09/605949	Erasable Digital Video Disk With Reference Clock Track	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
484	10960228-6	US	US6791924	09/917891	Erasable Digital Video Disk With Reference Clock Track	GRANTED
485	10970167-1	US	US6046969	09/040142	Multiple Clock Tracks For Erasable And Rewriteable Optical Disks	GRANTED
486	10970697-1	US	US5909661	08/866367	Method And Apparatus For Decomposing Drive Error Signal Noise Sources	GRANTED
487	10971019-1	US	US6178146	09/211393	Optical Storage Device For Writing Data At A Constant Bit Density During A CAV Mode Of Operation	GRANTED
488	10980963-1	US	US6393596	09/183832	Missing Pulse Detector Using Synchronous Detection	GRANTED
489	10981123-1	US	US6272103	09/181691	Timing Signal Recovery Device	GRANTED
490	10990672-1	US	US6646964	09/536298	Harmonic Correction In Phase-locked Loops	GRANTED
491	10990672-3	US	US6928036	10/696993	Harmonic Correction In Phase-locked Loops	GRANTED
492	10990808-1	US	US6636467	09/608600	Method And Apparatus For Accurately Calibrating The Timing Of A Write Onto Storage Media	GRANTED
493	10990815-1	US	US6956799	09/615646	Phase Discontinuity Compensation In A Bit-Accurate Optical Drive	GRANTED
494	10001110-1	US	US6316944	09/562596	Effective Netlength Calculation	GRANTED
495	10004234-1	US	US6892374	10/174674	Systems And Methods For Generating An Artwork Representation According To A Circuit Fabrication Process	GRANTED
496	10982009-1	US	US6625597	09/625138	Design Information Exchange System	GRANTED
497	200205546-1	US	US6904573	10/446097	Logic Gate Identification Based On Hardware Description Language Circuit Specification (as Amended)	GRANTED
498	200300183-1	US	US7013449	10/699241	Method Of Designing Custom Circuit Device Using Scheduling Clock Cycles (As Amended)	GRANTED
499	200307425-1	US	US5694579	08/019574	USING PRE-ANALYSIS AND A 2-STATE OPTIMISTIC MODEL TO REDUCE COMPUTATION IN TRANSISTOR CIRCUIT STIMULATION	GRANTED
500	10971022-1	US	US6099579	08/943085	Method And Apparatus For Checking Asynchronous HDL Circuit Designs	GRANTED
501	10971316-1	US	US6990643	09/311313	A Method And Apparatus For Determining Whether An Element In An Integrated Circuit Is A Feedback Element	GRANTED
502	10971317-1	US	US6327542	09/358837	System And Method For Approximating The Coupling Voltage Noise On A Node	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
503	10971321-1	US	US6275970	09/252378	Evaluation Of The Design Quality Of Network Nodes (As Amended) Testing-title SIM	GRANTED
504	10971322-1	US	US6305003	09/318907	System And Method For Propagating Clock Nodes In A Netlist Of A Circuit Design	GRANTED
505	10971323-1	US	US6295632	09/311314	System And Method For Detecting The Output Of A Clock Driver	GRANTED
506	10971324-1	US	US6311314	09/300205	System And Method For Evaluating The Loading Of A Clock Driver	GRANTED
507	10971330-1	US	US6279143	09/274798	A Method And Apparatus For Generating A Database Which Is Used For Determining The Design Quality Of Network Nodes	GRANTED
508	10982152-1	US	US6321173	09/209018	System And Method For Efficient Verification Of Functional Equivalence Between Design Models	GRANTED
509	100111238-1	US	US7032206	10/647688	System And Method For Iteratively Traversing A Hierarchical Circuit Design	GRANTED
510	200208595-1	US	US7000204	10/653650	Power Estimation Based On Power Characterizations	GRANTED
511	200307275-3	US	US5648909	08/490439	STATIC TIMING VERIFICATION IN THE PRESENCE OF LOGICALLY FALSE PATHS	GRANTED
512	200307427-1	US	US5659775	08/025605	TOPOLOGY INDEPENDENT SYSTEM FOR STATE ELEMENT CONVERSION	GRANTED
513	10003866-3	US	US6624002		Bistable molecular mechanical devices with an appended rotor activated by an electric field for electronic switching, gating and memory applications	EXPIRED
514	10003867-3	US	US6888978	10/618172	Electric-Field Actuated Chromogenic Materials Based On Molecules With A Rotating Middle Segment For Applications In Photonic Switching	GRANTED
515	10003869-1	US	US6674932	09/846135	Bistable Molecular Mechanical Devices With A Middle Rotating Segment Activated By An Electric Field For Electronic Switching, Gating And Memory Applications	GRANTED
516	10003869-3	US	US6920260	10/660277	Bistable Molecular Mechanical Devices With A Middle Rotating Segment Activated By An Electric Field For Electronic Switching, Gating And Memory Applications	GRANTED
517	10004762-1	US	US6663797	09/738793	Stabilization Of Configurable Molecular Mechanical Devices	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
518	10017873-1	US	US6751365	10/013643	A New E-Filed-Modulated Bistable Molecular Mechanical Device	GRANTED
519	10991997-1	US	US6248674	09/496365	Method Of Aligning Nanowires	GRANTED
520	200209690-1	US	US6989623	10/735197	Method And Apparatus For Measurement Using Piezoelectric Sensor	GRANTED
521	200210216-1	US	US6926921	10/430125	Imprint Lithography For Superconductor Devices	GRANTED
522	10001542-1	US	US6643812	09/563001	Manipulation Of Hardware Control Status Registers Via Boundary Scan	GRANTED
523	10002502-1	US	US6734690	09/562585	Back Pressure Test Fixture To Allow Probing Of Integrated Circuit Package Signals	GRANTED
524	10002502-2	US	US6765402	10/725715	Back Pressure Test Fixture To Allow Probing Of Integrated Circuit Package Signals	GRANTED
525	10017221-1	US	US6966693	10/345637	THERMAL CHARACTERIZATION CHIP	GRANTED
526	10017764-1	US	US6825651	10/121356	Test Method For Characterizing Currents Associated With Powered Components In An Electronic System	GRANTED
527	10019876-1	US	US6993685	10/241453	Technique For Testing Processor Interrupt Logic	GRANTED
528	10960916-5	US	US6535049	09/992907	Multipurpose Test Chip Input/Output Circuit	GRANTED
529	10971386-1	US	US6671664	09/510371	Management Of Uncommitted Register Values During Random Program Generation	GRANTED
530	10971386-3	US	US6886125	10/647296	Testing A Processor Using A Random Code Generator	GRANTED
531	200301523-2	US	US5694401	08/787452	FAULT ISOLATION USING PSEUDO-RANDOM SCAN	GRANTED
532	200302437-3	US	US6247144	08/355104	METHOD & APPARATUS FOR COMPARING REAL TIME OPERATION OF OBJECT CODE COMPATIBLE PROCES-SORS	GRANTED
533	200303017-1	US	US5717903	08/440638	A METHOD AND APPARATUS FOR EMULATING A PERIPHERAL DEVICE TO ALLOW DEVICE DRIVER DEVELOPMENT BEFORE AVAILABILITY OF THE PERIPHERAL DEVICE	GRANTED
534	200303017-2	US	US5953516	08/881183	METHOD AND APPARATUS FOR EMULATING A PERIPHERAL DEVICE TO ALLOW DEVICE DRIVER DEVELOPMENT BEFORE AVAILABILITY OF THE PERIPHERAL DEVICE	GRANTED
535	200304242-1	US	US6352203	09/270691	PENTIUM 2 AUTOMATIC CORE SPEED SELECT	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
536	200307888-1	US	US5684946	08/526293	APPARATUS AND METHOD FOR IMPROVING THE EFFICIENCY AND QUALITY OF FUNCTIONAL VERIFICATION	GRANTED
537	200304810-1	US	US6317417	09/166410	METHOD AND APPARATUS FOR DYNAMIC PULSE SIGNAL MODIFICATION ON A PARALLEL BUS	GRANTED
538	200307453-1	US	US5608883	08/012484	ADAPTER FOR INTERCONNECTING SINGLE-ENDED AND DIFFERENTIAL SCSI BUSES	GRANTED
539	200307777-1	US	US5527996	08/261571	APPARATUS FOR INCREASING SCSI BUS LENGTH BY INCREASING THE SIGNAL PROPOGATION VELOCITY OF ONLY TWO BUS SIGNALS	GRANTED
540	200307875-1	US	US5740198	08/262083	APPARATUS FOR INCREASING SCSI BUS LENGTH THROUGH SPECIAL TRANSMISSION OF ONLY TWO BUS SIGNALS	GRANTED
541	10007976-1	US	US6606733	09/782233	Method And System For Finding Static NAND And NOR Gates Within A Circuit And Identifying The Constitutent FETs For Each Gate	GRANTED
542	10971312-1	US	US6560571	09/345079	A Method And Apparatus For Prioritizing The Order In Which Checks Are Performed On A Node In An Integrated Circuit	GRANTED
543	10971318-1	US	US6249899	09/273631	System And Method For Detecting Pass FETs	GRANTED
544	10971328-1	US	US6301691	09/299975	System And Method For Detecting NFETs That Pull Up To VDD And PFETs That Pull Down To Ground	GRANTED
545	10971372-1	US	US6308301	09/358317	System And Method For Detecting Multiplexers In A Circuit Design	GRANTED
546	10001566-1	US	US6484302	09/614032	Auto-contactor System And Method For Generating Variable Size Contacts	GRANTED
547	10001843-1	US	US6625798	09/624790	A Method For Translating Conditional Expressions From A Non-Verilog Hardware Description Language To Verilog Hardware Description Language While Preserving Structure Suitable For Logic Synthesis	GRANTED
548	10007977-1	US	US6496031	09/845384	A Method For Calculating The P/N Ratio Of A Static Gate Based On Input Voltages	GRANTED
549	10007979-1	US	US6618840	09/782001	Method And System For Analyzing A VLSI Circuit Design	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
550	10010882-1	US	US6609242	09/909480	Automated Creation Of Power Distribution Grids For Tiled Cell Arrays In Integrated Circuit Designs	GRANTED
551	10011762-1	US	US6564365	09/921847	Method Of Simultaneously Displaying Schematic And Timing Data	GRANTED
552	10011762-2	US	US6964028	10/431383	Method Of Simultaneously Displaying Schematic And Timing Data	GRANTED
553	10971308-1	US	US7031889	09/273784	Method And Apparatus For Evaluating The Design Quality Of Network Nodes	GRANTED
554	10991469-1	US	US6567956	09/566765	Method For Performing Electrical Rules Checks On Digital Circuits With Mutually Exclusive Signals	GRANTED
555	100111078-1	US	US6687888	10/098111	A Method Of Optimizing High Performance CMOS Integrated Circuit Designs For Power Consumption And Speed	GRANTED
556	100111228-1	US	US7058908	10/647687	Systems And Methods Utilizing Fast Analysis Information During Detailed Analysis Of A Circuit Design	GRANTED
557	10961155-1	US	US6020749	08/745531	Method And Apparatus For Performing Testing Of Double-Sided Ball Grid Array Devices	GRANTED
558	20970004-2	US	US6147505	08/997008	Adaption Device For The Electrical Test Of Printed Circuit Boards	GRANTED
559	20980032-2	US	US6285196	09/388763	Process For The Electrical Testing Of The Base Material For The Manufacture Of Printed Circuit Boards	GRANTED
560	100204504-1	US	US6732352	10/154277	System And Method For Creating Probe Masks	GRANTED
561	200303948-1	US	US6123564	09/009667	APPARATUS AND METHODS FOR TESTING ELECTRO- NIC CIRCUITRY WITH MULTIPLE CONNECTOR SOCKET ARRAYS	GRANTED
562	200307672-2	US	US5701667	08/442938	METHOD OF MANUFACTURE OF AN INTERCONNECT STRESS TEST COUPON	GRANTED
563	10008130-1	US	US6785872	10/051078	An Algorithm-to-Hardware System And Method For Creating A Digital Circuit	GRANTED
564	10013527-1	US	US6631506	10/114545	A Method And Apparatus For Identifying Switching Race Conditions In A Circuit Design	GRANTED
565	10951096-1	US	US5910900	08/759585	Method Of Producing Cache Optimized Code From A Circuit Compiler	GRANTED
566	200301257-1	US	US6360284	09/231407	SYSTEM FOR PROTECTING OUTPUT DRIVERS CONNECTED TO A POWERED-OFF LOAD	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
567	200307823-2	US	US5646581	08/599512	LOW INDUCTANCE ELECTRICAL RESISTOR TERMINATOR PACKAGE	GRANTED
568	10007277-1	US	US6567960	09/972052	System For Improving Circuit Simulations By Utilizing A Simplified Circuit Model Based On Effective Capacitance And Inductance Values	GRANTED
569	10960861-1	US	US5729554	08/720604	Speculative Execution Of Test Patterns In A Random Test Generator	GRANTED
570	10960915-1	US	US5787092	08/863833	Test Chip Circuit For On-Chip Timing Characterization	GRANTED
571	10960916-1	US	US6407613	08/863832	Multipurpose Test Chip Input/Output Circuit	GRANTED
572	10971315-1	US	US6260180	09/311255	System And Method For Detecting FETs That Are Susceptible To Bootstrapping	GRANTED
573	10971374-1	US	US6910193	09/273820	System And Method For Executing Tests On An Integrated Circuit Design	GRANTED
574	10981367-1	US	US6298452	09/244872	Hardware Test Coverage Using Inter-Chip Event Filtering In Multi-Chip Simulations	GRANTED
575	10981928-1	US	US6332201	09/273582	Test Results Checking Via Predictive-Reactive Emulation	GRANTED
576	100205108-1	US	US6986087	10/238570	Method And Apparatus For Improving Testability Of I/O Driver/receivers	GRANTED
577	200300082-1	US	US6786761	10/425290	Method And System For Sensing The Status Of A ZIF Socket Lever	GRANTED
578	200302321-1	US	US6816989	10/033230	Method And Apparatus For Efficiently Managing Bandwidth Of A Debug Data Output Port Or Buffer	GRANTED
579	200307187-2	US	US5594741	08/345271	METHOD FOR CONTROL OF RANDOM TEST VECTOR GENERATION	GRANTED
580	10001118-1	US	US6618827	09/549233	System And Method For Parallel Testing Of IEEE 1149.1 Compliant Integrated Circuits	GRANTED
581	10004259-1	US	US6553524	09/615343	A Method For Automating Validation Of Integrated Circuit Test Logic	GRANTED
582	10951144-1	US	US5701335	08/658911	A Frequency Independent Scan Chain	GRANTED
583	10992563-1	US	US6829571	09/595036	Method For Determining The DC Margin Of A Latch	GRANTED
584	100201496-1	US	US6714035	10/184496	System And Method For Measuring Fault Coverage In An Integrated Circuit	GRANTED
585	100201496-2	US	US6876220	10/627564	System And Method For Measuring Fault Coverage In An Integrated Circuit	GRANTED
586	200209126-1	US	US7002358	10/732035	Method And Apparatus For Measuring Jitter	GRANTED
587	200301220-1	US	US6904553	09/670855	DETERMINISTIC TESTING OF EDGE-TRIGGERED LOGIC	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
588	200304999-1	US	US6292762	09/114753	METHOD FOR DETERMINING A RANDOM PERMUTATION OF VARIABLES BY APPLYING A TEST FUNCTION	GRANTED
589	200305091-1	US	US6327686	09/298265	METHOD TO ANALYZE MANUFACTURING TEST PATTERN COVERAGE OF CRITICAL-DELAY CIRCUIT PATHS	GRANTED
590	200307504-3	US	US5627842	08/658011	ARCHITECTURE FOR SYSTEM-WIDE STANDARDIZED INTRA-MODULE AND INTER-MODULE FAULT TESTING	GRANTED
591	1093829-1	US	US5940361	08/253641	Cartridge Hand Off Selection Mechanism	GRANTED
592	1094513-1	US	US5497281	08/331770	Expanded Tubular Hub Disk Pack Assembly Clamp	GRANTED
593	10011678-2	US	US6826056	10/455114	Systems For Use With Data Storage Devices	GRANTED
594	10971443-1	US	US6801954	09/515046	Method And Apparatus To Concurrently Operate On Multiple Data Movement Transactions In A Disk Array Subsystem	GRANTED
595	100202068-1	US	US6961299	10/310606	Storage Device	GRANTED
596	1092436-5	US	US5426383	08/229861	NCMOS - A High Performance Logic Circuit	GRANTED
597	1093696-1	US	US5444400	08/146254	Logic Output Circuit With High Transient Pull-Up Current	GRANTED
598	10016596-1	US	US6489830	09/947809	Apparatus And Method For Implementing A Multiplexer	GRANTED
599	10941058-1	US	US5554958	08/431252	Inverting Amplifier Having A Low Noise Biasing Network	GRANTED
600	50950017-4	US	US5608613	08/675300	Flyback Converter	GRANTED
601	70990061-1	US	US6831490	09/618405	Clock Synchronization Circuit And Method	GRANTED
602	200209546-1	US	US6943586	10/646935	Method And System To Temporarily Modify An Output Waveform	GRANTED
603	200209546-2	JP	3954601	P2004-242966	Method And System To Temporarily Modify An Output Waveform	GRANTED
604	200307052-1	US	US5287517	07/874322	SELF-COMPENSATING VOLTAGE LEVEL SHIFTING CIRCUIT	GRANTED
605	10970344-1	US	US6040530	08/986078	Versatile Printed Circuit Board For Testing Processing Reliability	GRANTED
606	200206515-1	US	US6956226	10/346046	Light Image Sensor Test Of Opto-Electronics For In-Circuit Test	GRANTED
607	200302917-1	US	US5432456	08/157641	CONNECTOR INSTALLATION GO/NO-GO TEST FIXTURE	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
608	200306747-4	US	US5596283	08/579038	CONTINUOUS MOTION ELECTRICAL CIRCUIT INTERCONNECT TEST METHOD AND APPARATUS	GRANTED
609	200307962-3	US	US5712858	08/627523	TEST METHODOLOGY FOR EXCEEDING TESTER PIN COUNT FOR AN ASIC DEVICE	GRANTED
610	10010620-1	US	US6510356	09/824427	A Method And Apparatus For Programming A Paste Dispensing Machine	GRANTED
611	10970575-1	US	US6039241	09/062050	Mechanism For Removal Of Surface Mount Connectors Using Heat Conduction Through Pins	GRANTED
612	10991691-2	US	US6315584	09/539285	Protective Cover For A Printed Circuit Board Electrical Connector	GRANTED
613	90960028-1	US	US5473510	08/218076	Land Grid Array Package/circuit Board Assemblies And Methods For Constructing The Same	GRANTED
614	100110496-1	US	US6972590	10/157496	Data Bus With Separate Matched Line Impedances And Method Of Matching Line Impedances	GRANTED
615	100110496-2	JP	4451614	P2003-150592	Data Bus With Separate Matched Line Impedances And Method Of Matching Line Impedances	GRANTED
616	200205243-1	US	US6931966	10/611825	Adjustable Socket	GRANTED
617	200210181-1	US	US7035111	10/444330	Circuit Board Orientation With Different Width Portions	GRANTED
618	200307923-2	US	US5890281	08/771994	METHOD FOR SIMPLIFIED AND COMPACT COMPONENT ADDITION TO A PRINTED CIRCUIT BOARD	GRANTED
619	10003298-1	US	US6544806	09/872809	Fast Computation Of Truth Tables	GRANTED
620	10011090-1	US	US6581197	09/927856	A Minimal Level Sensitive Timing Representative Of A Circuit Path	GRANTED
621	10011761-1	US	US6591404	09/916544	Method Of Automatically Finding And Fixing Min-time Violations	GRANTED
622	10011761-2	US	US6715137	10/426629	Method Of Resolving Min-time Violations In An Integrated Circuit	GRANTED
623	10970121-1	US	US5949990	08/761737	A Method Of Efficiently Modeling Tri-State Gates	GRANTED
624	10970124-1	US	US5880975	08/760744	A Method Of Producing Simplified Code From A Circuit Compiler	GRANTED
625	10971900-1	US	US6225929	09/204817	Digital-To-Analog Converter Having Switchable Current Sources And Resistor String	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
626	10990715-1	US	US6564354	09/586167	Method For Translating Conditional Expressions From A Non-verilog Hardware Description Language To Verilog Hardware Description Language While Preserving Structure Suitable For Logic Synthesis	GRANTED
627	100111076-1	US	US6711720	10/098136	A Method Of Optimizing High Performance CMOS Integrated Circuit Designs For Power Consumption And Speed Through Genetic Optimization	GRANTED
628	200307202-1	US	US5657239	07/969933	TIMING VERIFICATION USING SYNCHRONIZERS AND TIMING CONSTRAINTS	GRANTED
629	10002450-1	US	US6859770	09/727188	Method And Apparatus For Generating Transaction-based Stimulus For Simulation Of VLSI Circuits Using Event Coverage Analysis	GRANTED
630	10003290-1	US	US6718498	09/873874	Method And Apparatus For The Real Time Manipulation Of A Test Vector To Access The Microprocessor State Machine Information Using The Integrated Debug Trigger	GRANTED
631	10005853-1	US	US6675118	09/812660	System And Method Of Determining The Noise Sensitivity Characterization For An Unknown Circuit	GRANTED
632	10951071-1	US	US5901061	08/653581	Method Of Checking For Races In A Digital Design	GRANTED
633	10971309-1	US	US6389578	09/318988	A Method And Apparatus For Determining The Strengths And Weaknesses Of Paths In An Integrated Circuit	GRANTED
634	10971309-2	US	US6654936	10/099603	A Method And Apparatus For Determining The Strengths And Weaknesses Of Paths In An Integrated Circuit	GRANTED
635	10971389-1	US	US6678853	09/466503	Method And Apparatus For Generating Random Code	GRANTED
636	10990722-1	US	US6564162	09/541423	Method And Apparatus For Improving Electrical Verification Throughput Via Comparison Of Operating-Point Differentiated Test Results	GRANTED
637	10990723-1	US	US6704904	09/541253	Method And Apparatus For Permuting Code Sequences And Initial Context Of Code Sequences For Improved Electrical Verification	GRANTED
638	10991717-1	US	US6539503	09/448344	Method And Apparatus For Testing Error Detection	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
639	188473-4	US	US5428587	08/252146	Input/output Communication Between Autochanger And Drive	GRANTED
640	1094714-1	US	US5680375	08/372629	Media Autocharge Flipping Assembly With Brake	GRANTED
641	10941051-1	US	US5615345	08/489016	System For Interfacing An Optical Disk Autochanger To A Plurality Of Disk Drives	GRANTED
642	10950180-1	US	US5682096	08/386991	Method And Apparatus For Monitoring Operating Positions Of A Media Autochanger (As Amended)	GRANTED
643	10950181-5	US	US6738321	10/254691	Flip Latch Assembly For Media Autochanger	GRANTED
644	10960008-1	US	US5687039	08/641457	Dual Fixed-Finger Picker For Data Cartridges	GRANTED
645	10005067-1	US	US6904492	10/025306	WRITE-ONCE MEMORY DEVICE INCLUDING NON-VOLATILE MEMORY FOR TEMPORARY STORAGE	GRANTED
646	10007561-1	US	US6478231	09/894143	Methods For Reducing The Number Of Interconnects To The Pirm Memory Module	GRANTED
647	10007561-2	JP	3953902	P2002-189456	Methods And Apparatus For Reducing The Number Of Interconnects To The Pirm Memory Module (as Amended)	GRANTED
648	10011198-1	US	US6549099	09/896472	Electrically-coupled Mechanical Band-pass Filter	GRANTED
649	100110101-1	US	US6738307	10/145337	Address Structure And Methods For Multiple Arrays Of Data Storage Memory	GRANTED
650	100110101-2	JP	4152263	P2003-171412	Address Structure And Methods For Multiple Arrays Of Data Storage Memory	GRANTED
651	100110101-7	US	US6781918	10/777000	Address Structure And Methods For Multiple Array's Of Data Storage Memory	GRANTED
652	200313691-1	US	US7139183	10/896163	A Logical Arrangement Of Memory Arrays	GRANTED
653	200315433-1	US	US7106639	10/931842	Defect Management Enabled Pirm And Method	GRANTED
654	10017983-1	US	US6550732	10/020665	Heat Sink Retention Technique	GRANTED
655	10971929-1	US	US6141211	09/107095	Heat Sink Conduction Between Disk Drive Carrier And Information Storage Enclosure	GRANTED
656	10990607-1	US	US6075702	09/318569	A Heat Transfer Device For A Retention Assembly	GRANTED
657	200302866-1	US	US5406451	08/076467	HEAT SINK FOR PERSONAL COMPUTER	GRANTED
658	200308061-1	US	US5787976	08/674031	INTERLEAVED-FIN THERMAL CONNECTOR	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
659	200308165-1	US	US5838065	08/673976	INTEGRATED THERMAL COUPLING FOR HEAT GENERATING DEVICE	GRANTED
660	200308165-2	US	US6034430	08/970449	INTEGRATED THERMAL COUPLING FOR HEAT GENERATING DEVICE	GRANTED
661	200308165-3	US	US5948689	08/970750	INTEGRATED THERMAL COUPLING FOR HEAT GENERATING DEVICE	GRANTED
662	200401802-1	US	US7286352	11/107187	Thermally Expanding Base Of Heatsink To Receive Fins (as Amended)	GRANTED
663	10005727-1	US	US6919633	09/800939	Fabrication And Assembly Structures And Methods For Memory Devices	GRANTED
664	10005727-8	US	US7084007	10/697457	Fabrication And Assembly Structures And Methods For Memory Devices	GRANTED
665	10005727-9	US	US7199025	11/080284	Fabrication And Assembly Structures And Methods For Memory Devices	GRANTED
666	10006157-1	US	US6813182	10/160802	Diode-and-Fuse Memory Elements For A Write-Once Memory Comprising An Anisotropic Semiconductor Sheet	GRANTED
667	10005068-1	US	US6535418	09/911974	Optically Programmable Address Logic For Solid State Diode-based Memory	GRANTED
668	10005266-1	US	US6466512	09/990924	Method Of Generating Address Configuarations For Solid State Memory	GRANTED
669	10005266-2	JP	4081350	P2002-323686	Method Of Genrating Address Configuarations For Solid State Memory	GRANTED
670	10005266-3	CN	ZL02149530.0	2149530	Method Of Genrating Address Configuarations For Solid State Memory	GRANTED
671	10005266-5	TW	199127	91132102	Method Of Genrating Address Configuarations For Solid State Memory	GRANTED
672	10013681-1	US	US6535455	09/976792	FAULT-TOLERANT NEIGHBORHOOD DISJOINT ADDRESS LOGIC FOR SOLID STATE MEMORY	GRANTED
673	100110628-1	US	US6459648	09/976748	FAULT-TOLERANT ADDRESS LOGIC FOR SOLID STATE MEMORY	GRANTED
674	1092687-1	US	US5479356	08/031775	Computer-aided Method Of Designing A Carry-lookahead Adder	GRANTED
675	1093582-1	US	US5519626	08/089006	Method Of Dividing A Pipelined Stage Into Two Stages In A Computer-Aided Design System (As Amended)	GRANTED
676	10961366-1	US	US6892173	09/052358	Analyzing Effectiveness Of A Computer Cache By Estimating A Hit Rate Based On Applying A Subset Of Real-Time Addresses To A Model Of The Cache (as Amended)	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
677	100110556-1	US	US7107568	10/266719	A System And Method For Reducing Wire Delay Or Congestion During Synthesis Of Hardware Solvers	GRANTED
678	10011094-1	US	US6996515	09/927204	Enabling Verification Of A Minimal Level Sensitive Timing Abstraction Model	GRANTED
679	100110559-1	US	US7000137	10/266830	System For And Method Of Clock Cycle-Time Analysis Using Mode-Slicing Mechanism	GRANTED
680	100110560-1	US	US6966043	10/266831	Method For Designing Minimal Cost, Timing Correct Hardware During Circuit Synthesis	GRANTED
681	100110562-1	US	US7096438	10/266826	Method Of Using Clock Cycle-time In Determining Loop Schedules During Circuit Design	GRANTED
682	100111235-1	US	US7076752	10/647608	System And Method For Determining Unmatched Design Elements In A Computer-automated Design	GRANTED
683	200208415-1	US	US6952816	10/266856	Digital Circuit Synthesis Including Timing Convergence And Routability	GRANTED
684	989018-3	US	US5276826	07/742442	High Performance Computer Having Pseudo-Random Memory Address Transforms	GRANTED
685	10961397-4	US	US7117313	10/803289	Using Local Storage To Handle Multiple Outstanding Requests In A SCI System	GRANTED
686	10970005-4	US	US6381657	08/792077	Write Purge Partial In SCI Based System	GRANTED
687	200302506-1	US	US6990559	10/263835	Mechanism For Resolving Ambiguous Invalidates In A Computer System	GRANTED
688	200302506-2	US	US7174431	11/258586	Mechanism For Resolving Ambiguous Invalidates In A Computer System	GRANTED
689	5094011-2	US	US5708715	08/643066	Integrated Circuit Device With Function Usage Control	GRANTED
690	10001834-1	US	US6804810	09/510974	Resistance And Capacitance Estimation	GRANTED
691	10014143-1	US	US6637012	09/994151	Method And System For Identifying FETS Implemented In A Predefined Logic Equation	GRANTED
692	10016621-1	US	US6643828	10/016861	A Method For Controlling Critical Circuits In The Design Of Integrated Circuits	GRANTED
693	100111074-1	US	US6728941	10/098112	A Method Of Modeling The Crossover Current Component In Submicron CMOS Integrated Circuits Designs	GRANTED

No.	Record ID	Country	Patent No.	Application No.	Title	Status
694	100111075-1	US	US6785870	10/098110	A Method Of Optimizing High Performance CMOS Integrated Circuit Designs For Power Consumption And Speed Using Global And Greedy Optimizations In Combination	GRANTED
695	100200455-1	US	US6671862	10/213960	Method And Apparatus For Simplifying A Circuit Model	GRANTED
696	10002485-1	US	US6775814	09/561814	Dynamic System Configuration For Functional Design Verification	GRANTED
697	10011091-1	US	US6604227	09/928161	Minimal Level Sensitive Timing Abstraction Model Capable Of Being Used In General Static Timing Analysis Tools	GRANTED
698	10011092-1	US	US6611948	09/927220	Modeling Circuit Environmental Sensitivity Of A Minimal Level Sensitive Timing Abstraction Model	GRANTED
699	10011093-1	US	US6609233	09/927857	Improved Load Sensitivity Modeling In A Minimal Level Sensitive Timing Abstraction Model	GRANTED
700	10971300-1	US	US6718522	09/639613	Electrical Rules Checker System And Method Using Tri-state Logic For Electrical Rule Checks	GRANTED
701	100200883-1	US	US6775812	10/197346	Layout Design Process And System For Providing Bypass Capacitance And Compliant Density In An Integrated Circuit	GRANTED