

# PATENT ASSIGNMENT

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<b>SUBMISSION TYPE:</b>	CORRECTIVE ASSIGNMENT
<b>NATURE OF CONVEYANCE:</b>	Corrective Assignment to correct the assignment to re-record assignment previously recorded on Reel 025695 Frame 0105. Assignor(s) hereby confirms the correction of Patent No. 7779675 recorded in error to Patent No. 7799675.
<b>CONVEYING PARTY DATA</b>	
Name	Execution Date
Sang-Yun Lee	12/15/2010
<b>RECEIVING PARTY DATA</b>	
Name:	BeSang Inc.
Street Address:	1915 NW Amberglen Pkwy.
Internal Address:	Suite 310
City:	Beaverton
State/Country:	OREGON
Postal Code:	97006
<b>PROPERTY NUMBERS Total: 1</b>	
Property Type	Number
Patent Number:	7799675
<b>CORRESPONDENCE DATA</b>	
Fax Number:	(480)655-9536
<i>Correspondence will be sent via US Mail when the fax attempt is unsuccessful.</i>	
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<b>ATTORNEY DOCKET NUMBER:</b>	BESA.12758
<b>NAME OF SUBMITTER:</b>	Greg L. Martinez
Total Attachments: 14	

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**PATENT**  
**REEL: 025879 FRAME: 0921**

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### ASSIGNMENT

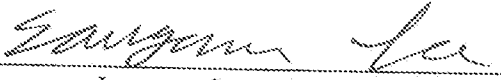
I, Sang-Yun Lee, residing at 18082 NW Elk Run Drive, Beaverton, Oregon 97006, represent that I have invented improvements in new and useful semiconductor technology for which I have executed applications for Letters Patent of the United States of America, as indicated in a list of applications for Letters Patent and issued patents provided in the Appendix included herewith.

BeSang, Inc., a corporation organized and existing under the laws of the State of Oregon, having a place of business at 1915 NW AmberGlen Pkwy, Suite 310, Beaverton, OR 97006 (hereinafter called BeSang), desires to acquire the entire right, title and interest in the said applications and issued patents and inventions, and to any United States and foreign patents to be obtained therefor.

For valuable consideration, the receipt and legal sufficiency of which I acknowledge, I have sold and do hereby sell, assign, transfer and set over unto BeSang, its successors and assigns, the entire right, title and interest in and to the inventions and all improvements thereon, in and to the applications for Letters Patent and issued patents thereon, as listed in the Appendix, in and to applications pertaining to or based upon the inventions, applications and issued patents, as listed in the Appendix, including divisional and continuing applications and continuations-in-part, and in and to any and all Letters Patent which may be granted and issued on the inventions, applications, and issued patents, as listed in the Appendix, or any of them, in the United States of America, its territories and possessions, and in all countries foreign thereto, together with and including all priority rights based upon any and all applications and issued patents in the United States of America covered by this Assignment.

I also agree that I will, at the request of BeSang, execute any and all applications for letters patent for the inventions, execute any and all other papers and documents and do all other and further lawful acts that BeSang may deem necessary or desirable to obtain Letters Patent on the invention, to secure the grant of such Letters Patent and to protect and vest in BeSang the undivided interests in the right, title and interest in the invention, applications and Letters Patent.

I also authorize and empower BeSang, its successors and assigns to apply for and obtain, in its or their own names, Letters Patent for the invention before competent International Authorities and in any and all countries foreign to the United States in which applications for Letters Patent can be so made or letters patent so obtained.

Signature:   
Inventor, Sang-Yun Lee

Signed at: Beaverton, Oregon, December 15, 2010  
Date

## Appendix

	Patent No.	App. No.	Title
1	7,378,702	10/934,270	Vertical Memory Device Structures
2	7,052,941	10/873,969	Method for Making a Three-Dimensional Integrated Circuit Structure
3	7,633,162	11/092,521	Electronic Circuit with Embedded Memory
4	7,470,598	11/092,499	Semiconductor Layer Structure and Method of Making the Same
5	7,470,142	11/092,498	Wafer Bonding Method
6		11/092,500	Semiconductor memory device
7		11/092,501	Semiconductor bonding and layer transfer method
8		11/180,286	Semiconductor Device with Base Support Structure
9		11/378,059	Three-Dimensional Integrated Circuit Structure and Method of Making Same
10		11/606,523	Three-Dimensional Integrated Circuit Structure
11		11/873,719	Electronic Circuit with Embedded Memory
12	7,718,508	11/873,851	Semiconductor Bonding and Layer Transfer Method
13		11/873,769	Semiconductor Memory Device
14	7,800,199	12/040,642	Semiconductor Circuit
15	7,671,371	12/165,445	Semiconductor Layer Structure and Method of Making the Same
16	7,846,814	12/165,475	Semiconductor Layer Structure and Method of Making the Same
17	7,632,738	12/345,303	Wafer Bonding Method
18		12/397,309	Semiconductor Circuit and Method of Fabricating the Same
19		12/470,344	Bonded Semiconductor Structure and Method of Making the Same
20	7,779,675	12/475,294	Bonded Semiconductor Structure and Method of Fabricating the Same
21		12/581,722	Information Storage System Which includes a Bonded Semiconductor Structure
22		12/618,542	Semiconductor Memory Device
23		12/637,559	Electronic Circuit with Embedded Memory
24		12/635,496	Method for Fabricating a Semiconductor Method Device
25		12/847,374	Semiconductor Circuit Structure and Method of Making the Same
26		12/874,866	Semiconductor Circuit
27		12/731,087	Three-Dimensional Semiconductor Structure and Method of Manufacturing the Same
28		61/346,847	Semiconductor Circuit and Method of Forming the Semiconductor Circuit Using a Capping Layer
29		61/349,134	Bonded Memory Circuit and Method of Fabrication
30		12/847,244	Semiconductor Circuit Structure and Method of Forming the Same Using a Capping Layer

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Property Type	Number												
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Total Attachments: 4

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