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To the Director of the U S Patent a... Please record the attached documents or the new address(es) below

1. Name of conveying party(ies)

Qspeed Semiconductor, Inc

Additional name(s) of conveying party(ies) attached? ☐ Yes ☒ No

2. Name and address of receiving party(ies)

Name: Power Integrations, Inc.
Internal Address:
Street Address: 5245 Hellyer Avenue
City: San Jose
State: California
Country: USA Zip: 95138

Additional name(s) & address(es) attached? ☐ Yes ☒ No

3. Nature of conveyance/Execution Date(s):

Execution Date(s): December 31, 2010

☒ Assignment ☐ Merger
☐ Security Agreement ☐ Change of Name
☐ Joint Research Agreement
☐ Government Interest Assignment
☐ Executive Order 9424, Confirmatory License
☐ Other

4. Application or patent number(s):

☒ This document is being filed together with a new application

A Patent Application No (s)

12/182,365 (filed July 30, 2008)

B Patent No (s)

6,251,716, 6,281,705, 6,304,007, 6,307,223, 6,349,047, 6,355,513, 6,356,059, 6,486,011, 6,528,880, 6,542,001, 6,549,439, 6,566,936, 6,580,252, 6,614,289, 6,621,722, 6,661,276, 6,674,107, 6,696,706

Additional numbers attached? ☒ Yes ☐ No

5. Name and address to whom correspondence concerning document should be mailed:

Name: The Law Offices of Bradley J. Bereznak
Internal Address:
Street Address: 800 W El Camino Real, Suite 180
City: Mountain View
State: California Zip: 94040
Phone Number: 650-903-2264
Fax Number: 650-903-2280
Email Address: bbereznak@bbpatent.com

6. Total number of applications and patents involved: 52

7. Total fee (37 CFR 1 21(h) & 3 41) $ 2,080.00

☒ Authorized to be charged to deposit account
☐ Enclosed
☐ None required (government interest not affecting title)

8. Payment Information

Deposit Account Number: 502060
Authorized User Name: Bradley J. Bereznak

03/15/2011 HTONIA 00000011 502060 12182365
01 FC:8021 2080.00 DA

9. Signature:

Signature

March 09, 2011
Date

Bradley J Bereznak
Name of Person Signing

Total number of pages including cover sheet, attachments, and documents: 8

Documents to be recorded (including cover sheet) should be faxed to (571) 273-0140, or mailed to:
Mail Stop Assignment Recordation Services, Director of the USPTO, P O Box 1450, Alexandria, V A 22313-1450

Additional patents assigned from Qspeed Semiconductor, Inc. to Power Integrations, Inc. (continuation of item 4):

6,734,715; 6,747,342; 6,750,698; 6,774,417; 6,777,722; 6,812,079; 6,887,768; 6,900,506; 6,921,932; 6,975,157; 6,995,052; 7,009,228; 7,009,229; 7,038,260; 7,045,397; 7,075,132; 7,098,634; 7,122,885; 7,211,845; 7,220,661; 7,227,242; 7,238,976; 7,262,461; 7,265,398; 7,268,378; 7,348,826; 7,417,266; 7,452,763; 7,655,964; 7,746,156; 7,608,888; 7,696,598; 7,696,540

ASSIGNMENT OF PATENTS

This **ASSIGNMENT OF PATENTS** (this "***Assignment***") granted by **QSPEED SEMICONDUCTOR INC.**, a Delaware corporation, ("***Transferor***") to **POWER INTEGRATIONS, INC.**, a Delaware corporation ("***Company***") is made effective as of December 31, 2010.

RECITALS

WHEREAS, pursuant to an Asset Purchase Agreement dated December 30, 2010 (the "***Purchase Agreement***"), by and between the Transferor, the Company, certain stockholders of Transferor and Natasha Skok as the Stockholders' Agent, Transferor agreed to transfer to Company various intellectual property rights, including the patents and patent applications set forth on **APPENDIX A** hereto and described below; and

WHEREAS, Transferor desires to transfer and assign to Company, and Company desires to accept the transfer and assignment of, all of Transferor's worldwide right, title and interest in, to, and under such patents and patent applications.

NOW THEREFORE, for and in consideration of the covenants and agreements set forth in the Purchase Agreement and other good and valuable consideration, the receipt and sufficiency of which are hereby acknowledged:

Transferor hereby assigns, delivers, transfers, and conveys unto Company, all right, benefits, title, and interest in and to the patents and patent applications and invention records set forth on **APPENDIX A** (collectively, the "***Patents***"), and all future patents which may be granted therefrom throughout the world and all divisions, reissues, reexaminations, substitutions, continuations, foreign counterparts and extensions of the Patents (collectively "***Future Patents***"); and Transferor hereby authorizes the Company to request that the United States Patent and Trademark Office and other patent offices throughout the world issue all Future Patents, insofar as Transferor's interest is concerned, to Company.

[Signature Page Follows]

IN WITNESS WHEREOF, Transferor has caused this Assignment to be executed by its duly authorized corporate officer effective as of the date first written above

QSPEED SEMICONDUCTOR INC.

By _____

Name _____

Title _____

IN WITNESS WHEREOF, the Company has caused this Assignment to be executed by its duly authorized corporate officer effective as of the date first written above.

POWER INTEGRATIONS, INC.

By: _____

Name: _____

Title: _____

APPENDIX A

[TO MATCH SCHEDULE 1.1(A) OF THE AGREEMENT]

1.1 (a) Certain Patents

	Patent #	Issue Date	Title	Inventor	Jurisdiction
1	6,251,716	June 26, 2001	JFET structure and manufacture method for low on-resistance and low voltage application	Ho-Yuan Yu	United States
2	6,281,705	August 28, 2001	Power supply module in integrated circuits	Ho-Yuan Yu	United States
3	6,304,007	October 16, 2001	Switcher for switching capacitors	Ho-Yuan Yu	United States
4	6,307,223	October 23, 2001	Complementary junction field effect transistors	Ho-Yuan Yu	United States
5	6,349,047	February 19, 2002	Full wave rectifier circuit using normally off JFETs	Ho-Yuan Yu	United States
6	6,355,513	March 12, 2002	Asymmetric depletion region for normally off JFET	Ho-Yuan Yu	United States
7	6,356,059	March 12, 2002	Buck converter with normally off JFET	Ho-Yuan Yu	United States
8	6,486,011	November 26, 2002	JFET structure and manufacture method for low on-resistance and low voltage application	Ho-Yuan Yu	United States
9	6,528,880	March 4, 2003	Semiconductor package for power JFET having copper plate for source and ribbon contact for gate	Bill Planey	United States
10	6,542,001	April 1, 2003	Power supply module in integrated circuits	Ho-Yuan Yu	United States
11	6,549,439	April 15, 2003	Full wave rectifier circuit using normally off JFETS	Ho-Yuan Yu	United States
12	6,566,936	May 20, 2003	Two terminal rectifier normally OFF JFET	Ho-Yuan Yu	United States
13	6,580,252	June 17, 2003	Boost circuit with normally off JFET	Ho-Yuan Yu	United States
14	6,614,289	September 2, 2003	Starter device for normally off FETs	Ho-Yuan Yu	United States
15	6,621,722	September 16, 2003	Rectifier circuits with low forward voltage JFET device	Ho-Yuan Yu	United States
16	6,661,276	December 9, 2003	MOSFET driver matching circuit for an enhancement mode JFET	Daniel Chang	United States
17	6,674,107	January 6, 2004	Enhancement mode junction field effect transistor with low on resistance	Ho-Yuan Yu	United States
18	6,696,706	February 24, 2004	Structure and method for a junction field effect transistor with reduced gate capacitance	Pete L Pegler	United States
19	6,734,715	May 11, 2004	Two terminal rectifier using normally off JFET	Ho-Yuan Yu	United States
20	6,747,342	June 8, 2004	Flip-chip packaging	William Planey	United States
21	6,750,698	June 15, 2004	Cascade circuits utilizing normally-off junction field effect transistors for low on-resistance and low voltage applications	Ho-Yuan Yu	United States
22	6,774,417	August 10, 2004	Electrostatic discharge protection device for integrated circuits	Ho-Yuan Yu, Chong Ming Lin	United States
23	6,777,722	August 17, 2004	Method and structure for double dose gate in a JFET	Ho-Yuan Yu, Pete Pegler, Valentino Liva	United States
24	6,812,079	November 2, 2004	Method for a junction field effect transistor with reduced gate capacitance	Pete L Pegler	United States
25	6,887,768	May 3, 2005	Method and structure for composite trench fill	Ho-Yuan Yu	United States
26	6,900,506	May 31, 2005	Method and structure for a high voltage junction field effect transistor	Ho-Yuan Yu, Eric Johnson	United States
27	6,921,932	July 26, 2005	JFET and MESFET structures for low voltage, high current and high frequency applications	Ho-Yuan Yu, Valentino Liva	United States
28	6,975,157	December 13, 2005	Starter device for normally off JFETs	Ho-Yuan Yu	United States
29	6,995,052	February 7, 2006	Method and structure for double dose gate in a JFET	Ho-Yuan Yu, Pete Pegler, Valentino Liva	United States
30	7,009,228	March 7, 2006	Guard ring structure and method for fabricating same	Ho-Yuan Yu	United States
31	7,009,229	March 7, 2006	Electrostatic discharge protection device for integrated circuits	Ho-Yuan Yu, Chong Ming Lin	United States
32	7,038,260	May 2, 2006	Dual gate structure for a FET and method for fabricating same	Ho-Yuan Yu	United States

33	7,045,397	May 16, 2006	JFET and MESFET structures for low voltage high current and high frequency applications	Ho-Yuan Yu, Valentino Liva	United States
34	7,075,132	July 11, 2006	Programmable junction field effect transistor and method for programming the same	Ho-Yuan Yu, Chong Ming Lin	United States
35	7,098,634	August 29, 2006	Buck-boost circuit with normally off JFET	Ho-Yuan Yu	United States
36	7,122,885	October 17, 2006	Flip-chip packaging	William Planey	United States
37	7,211,845	May 1, 2007	Multiple doped channel in a multiple doped gate junction field effect transistor	Ho-Yuan Yu, Jian Li	United States
38	7,220,661	May 22, 2007	Method of manufacturing a Schottky barrier rectifier	Ho-Yuan Yu, Chong Ming Lin	United States
39	7,227,242	June 5, 2007	Structure and method for enhanced performance in semiconductor substrates	Ho-Yuan Yu, Chong Ming Lin, Jay Denning	United States
40	7,238,976	July 3, 2007	Schottky barrier rectifier and method of manufacturing the same	Ho-Yuan Yu, Chong Ming Lin	United States
41	7,262,461	August 28, 2007	JFET and MESFET structures for low voltage, high current and high frequency applications	Ho-Yuan Yu, Valentino Liva	United States
42	7,265,398	September 4, 2007	Method and structure for composite trench fill	Ho-Yuan Yu	United States
43	7,268,378	September 11, 2007	Structure for reduced gate capacitance in a JFET	Ho-Yuan Yu, Valentino Liva	United States
44	7,348,826	March 25, 2008	Composite field effect transistor	Jonathan Klein, Morris Tsou	United States
45	7,417,266	August 26, 2008	MOSFET having a JFET embedded as a body diode	Ho-Yuan Yu, Jian Li, Daniel Chang	United States
46	7,452,763	November 18, 2008	Method for a junction field effect transistor with reduced gate capacitance	Ho-Yuan Yu	United States
47	7,655,964	February 2, 2010	PROGRAMMABLE JUNCTION FIELD EFFECT TRANSISTOR AND METHOD FOR PROGRAMMING SAME	Ho-Yuan YU	United States
48	7,746,156	June 29, 2010	CIRCUIT AND METHOD FOR DRIVING A JUNCTION FIELD EFFECT TRANSISTOR	Harold L MASSIE, Kuang Ming Daniel CHANG	United States
49	7,608,888	October 27, 2009	FIELD EFFECT TRANSISTOR	Jian LI, Ho-Yuan YU	United States
50	7,696,598	April 13, 2010	ULTRAFAST RECOVERY DIODE	Richard Francis, Jian Li, Yang-Yu Fan, Eric Johnson	United States
51	7,696,540	April 13, 2010	Structure and Method for a Fast Recovery Rectifier Structure	Richard FRANCIS, Yang Y FAN, Eric JOHNSON, Hy HOANG	United States
52	200680051396 60	December 19, 2006	ULTRAFAST RECOVERY DIODE	Richard Francis, Jian Li, Yang-Yu Fan, Eric Johnson	China
53	9107369 90	December 19, 2006	ULTRAFAST RECOVERY DIODE	Richard Francis, Jian Li, Yang-Yu Fan, Eric Johnson	Hong Kong
54	2008-548658	December 19, 2006	ULTRAFAST RECOVERY DIODE	Richard Francis, Jian Li, Yang-Yu Fan, Eric Johnson	Japan
55	95149314.00	December 19, 2006	ULTRAFAST RECOVERY DIODE	Richard Francis, Jian Li, Yang-Yu Fan, Eric Johnson	Taiwan
56	200680051344.90	December 20, 2006	APPARATUS AND METHOD FOR A FAST RECOVERY RECTIFIER STRUCTURE	Richard FRANCIS, Yang Y FAN, Eric JOHNSON, Hy HOANG	China
57	9107014 80	December 20, 2006	APPARATUS AND METHOD FOR A FAST RECOVERY RECTIFIER STRUCTURE	Richard FRANCIS, Yang Y FAN, Eric JOHNSON, Hy HOANG	Hong Kong
58	2008-548647	December 20, 2006	APPARATUS AND METHOD FOR A FAST RECOVERY RECTIFIER STRUCTURE	Richard FRANCIS, Yang Y FAN, Eric JOHNSON, Hy HOANG	Japan
59	95149303 00	December 20, 2006	APPARATUS AND METHOD FOR A FAST RECOVERY RECTIFIER STRUCTURE	Richard FRANCIS, Yang Y FAN, Eric JOHNSON, Hy HOANG	Taiwan
60	12/182,365	July 30, 2008	MOSFET HAVING A JFET EMBEDDED AS A BODY DIODE	Jian LI, Kuang Ming Daniel CHANG, Ho-Yuan YU	United States