PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Sino Matrix Technology Inc.	04/07/2011

RECEIVING PARTY DATA

Name:	Liyue Capital, LLC
Street Address:	2711 Centerville Road, Suite 400
City:	Wilmington
State/Country:	DELAWARE
Postal Code:	19808

PROPERTY NUMBERS Total: 22

Property Type	Number
Patent Number:	5481686
Patent Number:	5524220
Patent Number:	5615263
Patent Number:	5640415
Patent Number:	5937170
Patent Number:	5937193
Patent Number:	5953741
Patent Number:	6047358
Patent Number:	6105142
Patent Number:	6321321
Patent Number:	6338118
Patent Number:	6385749
Patent Number:	5701435
Patent Number:	6851010
Patent Number:	6334198

OP $880.00 5481686

Patent Number:	5896550
Patent Number:	6188257
Patent Number:	6553496
Patent Number:	6311302
Application Number:	08241108
Application Number:	09291371
Application Number:	07500612

CORRESPONDENCE DATA

Fax Number: (302)397-2678
Correspondence will be sent via US Mail when the fax attempt is unsuccessful.
Email: AssignmentRecordation@gmail.com
Correspondent Name: Liyue Capital, LLC
Address Line 1: 2711 Centerville Road, Suite 400
Address Line 4: Wilmington, DELAWARE 19808

NAME OF SUBMITTER:	Russell Boltwood

Total Attachments: 7
source=Sino-Liyue_US Assignment#page1.tif
source=Sino-Liyue_US Assignment#page2.tif
source=Sino-Liyue_US Assignment#page3.tif
source=Sino-Liyue_US Assignment#page4.tif
source=Sino-Liyue_US Assignment#page5.tif
source=Sino-Liyue_US Assignment#page6.tif
source=Sino-Liyue_US Assignment#page7.tif

EXHIBIT B, twice revised

ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, Sino Matrix Technology Inc., a Taiwan company having a business address at 3F-5, No. 371, Sec. 1, Guangfu Rd., Hsinchu City 300, Taiwan, R.O.C. (***"Assignor"***), does hereby sell, assign, transfer, and convey unto Liyue Capital, LLC, a Delaware limited liability company, with an office at 2711 Centerville Road, Suite 400, Wilmington, Delaware, 19808, U.S.A. (***"Assignee"***) its successors, assigns and legal representatives, all right, title, and interest that exist today and may exist in the future in and to any and all of the following (collectively, the ***"Patent Rights"***):

(a) the patents and patent applications listed in the Attachment hereto (the ***"Patents"***);

(b) any and all causes of action (whether currently pending, filed, or otherwise) and any and all other enforcement rights under the Patents, including the rights to (i) damages, (ii) injunctive relief, and (iii) any and all other remedies of any kind for past, current, and future infringement of the Patents;

(c) any and all rights to collect royalties or other payments for infringement of the Patents, not previously settled by NXP B.V.;

(d) all patent and patent application rights directed to and covering any inventions or the subject matter of any invention disclosures described in any of the Patents that, but only to the extent that any such inventions or the subject matter of any such invention disclosures, (i) are claimed and covered by any claim in the Patents, (ii) are capable of being reduced to a patent claim filed and/or awarded in any reissue or reexamination proceedings brought with respect to any of the Patents, and/or (iii) are capable of being reduced to a patent claim filed and/or awarded in any continuations, continuations in part, continuing prosecution applications, requests for continuing examinations and/or divisions of any of the Patents; and

(e) all rights to apply in any or all countries of the world for patents, certificates of invention, utility models, industrial design protections, design patent protections, or other governmental grants or issuances of any type related to any item in any of the foregoing categories (a) through (d), including, without limitation, under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement, or understanding.

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

The terms and conditions of this Assignment of Patent Rights will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed at _____ as of _____, 2011.

ASSIGNOR

Sino Matrix Technology Inc.

By: _____

Name: Chi-Ping Chang

Title: President

ATTESTATION OF SIGNATURE PURSUANT TO 28 U.S.C. 1746

The undersigned witnessed the signature of Chi-Ping Chang to the above Assignment of Patent Rights on behalf of Sino Matrix Technology Inc. and makes the following statements:

1. I am over the age of 18 and competent to testify as to the facts in this Attestation block if called upon to do so.

2. Chi-Ping Chang is personally known to me (or proved to me on the basis of satisfactory evidence) and appeared before me on Chi-Ping Chang April_____, 2011 to execute the above Assignment of Patent Rights on behalf of Sino Matrix Technology Inc.

3. Chi-Ping Chang subscribed to the above Assignment of Patent Rights on behalf of Sino Matrix Technology Inc.

I declare under penalty of perjury under the laws of the United States of America that the statements made in the three (3) numbered paragraphs immediately above are true and correct.

EXECUTED on Apr. 7, 2011 (date)

By: _____

Print Name: Johnson Yin

Attachment to EXHIBIT B, twice revised

08/241,108	US	Floating-point processor with apparent-precision based selection of execution-precision	Dockser, Kenneth A.	5/11/1994
5,481,686	US	Floating-point processor with apparent-precision based selection of execution-precision	Dockser, Kenneth A.	5/4/1995
PCT/US1995/004044	WO	Floating-point processor with apparent-precision based selection of execution-precision	Dockser, Kenneth A.	4/13/1995
5,524,220	US	Memory subsystems having look-ahead instruction prefetch buffers and intelligent posted write buffers for increasing the throughput of digital computer systems	Verma, Deepak; Potts, W. Henry	8/31/1994
5,615,263	US	Dual purpose security architecture with protected internal operating system	Takahashi, Richard J.	1/6/1995
5,640,415	US	Bit error performance of a frequency hopping, radio communication system	Pandula, Louis	6/10/1994
PCT/US1995/007379	WO	Redundant retransmission of digitized voice data in frequency hopping system	Pandula, Louis	6/9/1995
EP95923796.7	EP	Redundant retransmission of digitized voice data in frequency hopping system	Pandula, Louis	6/9/1995
5,937,170	US	Data communications with processor-assertable addresses mapped to peripheral-accessible-addresses-times-command product space	Bedarida, Alessandro	2/21/1997

5,937,193	US	Circuit arrangement for translating platform-independent instructions for execution on a hardware platform and method thereof	Evoy, David Ross	11/27/1996
09/291,371	US			4/14/1999
5,953,741	US	Stack cache for stack-based processor and method thereof	Evoy, David Ross; Levy, Paul S.	11/27/1996
6,047,358	US	Computer system, cache memory and process for cache entry replacement with selective locking of elements In different ways and groups	Jacobs, Eino	10/31/1997
PCT/IB1998/001484	WO	Cache replacement policy with locking	Jacobs, Eino	9/24/1998
JP11-525774	JP	Cache replacement policy with locking	Jacobs, Eino	9/24/1998
KR10-0637610	KR	Cache replacement policy with locking	Jacobs, Eino	9/24/1998
EP0950223	EP	Cache replacement policy with locking	Jacobs, Eino	9/24/1998
GB0950223	GB	Cache replacement policy with locking	Jacobs, Eino	9/24/1998
DE69840960.4	DE	Cache replacement policy with locking	Jacobs, Eino	9/24/1998
FR0950223	FR	Cache replacement policy with locking	Jacobs, Eino	9/24/1998
6,105,142	US	Intelligent power management interface for computer system hardware	Goff, Lonnie C.; Evoy, David R.; Story, Franklyn; Sullivan, Mark	2/11/1997

6,321,321	US	Set-associative cache-management method with parallel and single-set sequential reads	Johnson, Mark W.	6/21/1999
6,338,118	US	Set-associative cache-management method with parallel and single-set sequential reads	Johnson, Mark W.	3/1/2001
6,385,749	US	Method and arrangement for controlling multiple test access port control modules	Adusumilli, Swaroop; Steele, James; Cassetti, David	4/1/1999
07/500,612	US	Instruction cache system for implementing programs having non-sequential instructions and method of implementing same	Chi, Chi-Hung	3/27/1990
EP0449369	EP	A data processing system provided with a performance enhancing instruction cache	Chi, Chi-Hung	3/25/1991
DE69129872.6	DE	A data processing system provided with a performance enhancing instruction cache	Chi, Chi-Hung	3/25/1991
FR0449369	FR	A data processing system provided with a performance enhancing instruction cache	Chi, Chi-Hung	3/25/1991
GB0449369	GB	A data processing system provided with a performance enhancing instruction cache	Chi, Chi-Hung	3/25/1991
JP3095802	JP	Data processing system having performance improving instruction cache	Chi, Chi-Hung	3/27/1991
5,701,435	US	Instruction cache system for implementing programs having non-sequential instructions and method of implementing same	Chi, Chi-Hung	5/19/1993

6,851,010	US	Cache management instructions	Rao, Lakshmi; Huang, Sunny C.,; Bloks, Rudolf H. J.; Vissers, Kornelis A.,; Sijstermans; Frans W.	6/29/2001
6,334,198	US	Method and arrangement for controlling multiply-activated test access port control modules	Adusumilli, Swaroop; Steele, James; Cassetti, David	4/1/1999
5,896,550	US	Direct memory access controller with full read/write capability	Wehunt, Omer Lem; Lavin, Jeffrey M.	4/3/1997
6,188,257	US	Power-on-reset logic with secure power down capability	Buer, Mark Leonard	2/1/1999
6,553,496	US	Integration of security modules on an integrated circuit	Buer, Mark Leonard	2/1/1999
PCT/US1999/028289	WO	Integration of security modules on an integrated circuit	Buer, Mark Leonard	11/20/1999
CNZL99806915.9	CN	Integration of security modules on integrated circuit	Buer, Mark Leonard	11/20/1999
EP1066555	EP	Integration of security modules in an integrated circuit	Buer, Mark Leonard	11/20/1999
DE69914729.8	DE	Integration of security modules in an integrated circuit	Buer, Mark Leonard	11/20/1999
FR1066555	FR	Integration of security modules in an integrated circuit	Buer, Mark Leonard	11/20/1999
GB1066555	GB	Integration of security modules in an integrated circuit	Buer, Mark Leonard	11/20/1999

JP2000-596435	JP	Integration of security modules on an integrated circuit	Buer, Mark Leonard	11/20/1999
6,311,302	US	Method and arrangement for hierarchical control of multiple test access port control modules	Cassetti, David; Steele, James; Adusumilli, Swaroop	4/1/1999
DE19609865.3	DE	Computer implementation of security mode within processor	Takahashi, Richard J.	3/13/1996
FR2746199	FR	Computer implementation of security mode within processor	Takahashi, Richard J.	3/15/1996
JP08-064466	JP	Dual-purpose maintenance architecture having protected internal operating system	Takahashi, Richard J.	3/21/1996