PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
NXP B.V.	03/30/2011

RECEIVING PARTY DATA

Name:	Eliposki Remote Ltd., L.L.C.
Street Address:	2711 Centerville Rd
Internal Address:	Suite 400
City:	Wilmington
State/Country:	DELAWARE
Postal Code:	19808

PROPERTY NUMBERS Total: 18

Property Type	Number
Patent Number:	7605740
Patent Number:	7663917
Patent Number:	7181655
Patent Number:	7418650
Patent Number:	7500204
Patent Number:	7348229
Patent Number:	7635993
Patent Number:	7659154
Patent Number:	7605027
Patent Number:	7659748
Patent Number:	7640437
Patent Number:	7227422
Patent Number:	7395165
Application Number:	12125737

OP $720.00 7605740

Patent Number:	7200057
Patent Number:	7619431
Patent Number:	7333356
Patent Number:	7232983

CORRESPONDENCE DATA

Fax Number: (608)258-4258
Correspondence will be sent via US Mail when the fax attempt is unsuccessful.
Phone: 608-257-5035
Email: ptomailmadison@foley.com
Correspondent Name: Paul S. Hunter
Address Line 1: Foley & Lardner
Address Line 2: 150 E. Gilman St.
Address Line 4: Madison, WISCONSIN 53701-1497

NAME OF SUBMITTER:	Paul S. Hunter

Total Attachments: 9
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Exhibit B

ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, NXP B.V., a company formed in The Netherlands, with an office at High Tech Campus 60, 5656 AG Eindhoven, The Netherlands (**"*Assignor*"**), does hereby sell, assign, transfer, and convey unto, Eliposki Remote Ltd., L.L.C., a Delaware limited liability company, with an address at 2711 Centerville Rd, Suite 400 (**"*Assignee*"**), or its designees, all right, title, and interest that exist today and may exist in the future in and to any and all of the following (collectively, the **"*Patent Rights*"**):

(a) the provisional patent applications, patent applications and patents listed in the table below (the "***Patents***");

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
CN200680046508.9	CN	12/8/2006	Flash analog-to-digital converter Pelgrom, Marcel; Katoch, Atul; Vertregt, Maarten
7,605,740 (12/097,040)	US	10/20/2009 (12/8/2006)	Flash analog-to-digital converter Pelgrom, Marcel; Katoch, Atul; Vertregt, Maarten
CN200480016966.9	CN	6/10/2004	Non-volatile static memory cell Cuppens, R.; Diteweg, A. M. H.
DE602004015457.1 (DE602004015457.1)	DE	7/30/2008 (6/10/2004)	Non-volatile static memory cell Cuppens, Roger; Diteweg, Anthonie M.
FR1639605 (FR04736564.8)	FR	7/30/2008 (6/10/2004)	Non-volatile static memory cell Cuppens, Roger; Diteweg, Anthonie M. H.
GB1639605 (GB04736564.8)	GB	7/30/2008 (6/10/2004)	Non-volatile static memory cell Cuppens, Roger; Diteweg, Anthonie M. H.
KR10-2005-7024108	KR	6/10/2004	Non-volatile static memory cell Cuppens, Roger; Diteweg, Anthonie M. H.
7,663,917 (10/560,677)	US	2/16/2010 (6/10/2004)	Non-volatile static memory cell Cuppens, Roger; Ditewig, Anthonie Meindert Herman
7,181,655 (10/481,570)	US	2/20/2007 (6/18/2002)	Method and circuit arrangement for memory error processing Ditewig, Anthonie Meindert Herman; Cuppens, Roger; Salters, Roelof Herman Willem

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
CN200480012124.6	CN	4/26/2004	Method for temporal synchronization of clocks Ungermann, J.; Fuhrmann, P.; Zinke, M.
7,418,650 (10/555,258)	US	8/26/2008 (4/26/2004)	Method for temporal synchronization of clocks Ungermann, Jorn; Fuhrmann, Peter; Zinke, Manfred
CNZL200480016035.9 (CN200480016035.9)	CN	2/4/2009 (5/28/2004)	Real-time adaptive control for best IC performance Pineda De Gyvez, J. D. J.; Pessolano, F.; Meijer, R. I. M. P.; Rius Vazquez, J.; Rao, K. B. R.
EP04735306.5	EP	5/28/2004	Real-time adaptive control for best IC performance Pineda De Gyvez, Jose D. J.; Pessolano, Francesco; Meijer, Rinze I. M. P.; Rius Vazquez, Josep; Rao, Kiran B. R.
7,500,204 (10/559,208)	US	3/3/2009 (5/28/2004)	Real-time adaptive control for best IC performance Pineda De Gyvez, Jose De Jesus; Pessolano, Francesco; Meijer, Rinze Ida Mechtildis Peter; Rius Vazquez, Josep; Rao, Kiran Batni Raghavendra
CNZL200480037922.4 (CN200480037922.4)	CN	1/28/2009 (11/29/2004)	Method of manufacturing a semiconductor device and semiconductor device obtained with such a method Pawlak, B. J.; Duffy, R. J.
EP04799263.1	EP	11/29/2004	Method of manufacturing a semiconductor device and semiconductor device obtained with such a method Pawlak, Bartlomiej J.; Duffy, Raymond J.
7,348,229 (10/596,450)	US	3/25/2008 (11/29/2004)	Method of manufacturing a semiconductor device and semiconductor device obtained with such a method Pawlak, Bartlomiej Jan; Duffy, Raymond James
CN200580015755.8	CN	5/11/2005	Digital magnetic current sensor and logic Boeve, H. M. B.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
EP05737023.1	EP	5/11/2005	Digital magnetic current sensor and logic Boeve, Hans M. B.
7,635,993 (11/596,791)	US	12/22/2009 (5/11/2005)	Digital magnetic current sensor and logic Boeve, Hans Marc Bert
CNZL200580027415.7 (CN200580027415.7)	CN	7/29/2009 (8/1/2005)	Dual gate CMOS fabrication Muller, Markus; Stolk, Peter
EP05773563.1	EP	8/1/2005	Dual gate CMOS fabrication Muller, Markus; Stolk, Peter
7,659,154 (11/573,346)	US	2/9/2010 (8/1/2005)	Dual gate CMOS fabrication Muller, Markus; Stolk, Peter
CNZL200680014321.0 (CN200680014321.0)	CN	12/2/2009 (4/24/2006)	Method of fabricating a bipolar transistor Meunier-Beillard, Philippe; Hijzen, Erwin; Donkers, Johannes J. T. M.; Neuilly, Francois
EP06728019.8	EP	4/24/2006	Method of fabricating a bipolar transistor Neuilly, Francois; Donkers, Johannes J. T. M.; Hijzen, Erwin; Meunier-Beillard, Philippe
7,605,027 (11/913,049)	US	10/20/2009 (4/24/2006)	Method of fabricating a bipolar transistor Meunier-Beillard, Philippe; Hijzen, Erwin; Donkers, Johannes J. T. M.; Neuilly, Francois
CN200780009081.X	CN	3/13/2007	Electronic device and integrated circuit Chandra, Sunil
EP07735099.9	EP	3/13/2007	Electronic device and integrated circuit Chandra, Sunil
JP2008-558969	JP	3/13/2007	Electronic device and integrated circuit Chandra, Sunil
7,659,748 (12/293,241)	US	2/9/2010 (3/13/2007)	Electronic device and integrated circuit Chandra, Sunil
7,640,437 (10/537,517)	US	12/29/2009 (11/19/2003)	Address encryption method for flash memories Feuser, Markus; Sommer, Sabine
CNZL200380106243.3 (CN200380106243.3)	CN	8/1/2007 (12/15/2003)	Temperature compensated RC oscillator Yarborough Jr., J. M.

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
EP03768033.7	EP	12/15/2003	Temperature compensated R-C oscillator Yarborough Jr., John M.
7,227,422 (10/538,574)	US	6/5/2007 (12/15/2003)	Temperature compensated R-C oscillator Yarborough Jr., John M.
CNZL200380103944.1 (CN200380103944.1)	CN	6/25/2008 (11/14/2003)	Circuit arrangement with non-volatile memory module and method of en-/decrypting data in the non-volatile memory module Buhr, W.
EP03811456.7	EP	11/14/2003	Circuit arrangement with non-volatile memory module and method of en-/decrypting data in the non-volatile memory module Buhr, Wolfgang
JP2004-553018	JP	11/14/2003	Circuit arrangement with non-volatile memory module and method of en-/decrypting data in the non-volatile memory module Buhr, Wolfgang
7,395,165 (10/535,370)	US	7/1/2008 (11/14/2003)	Circuit arrangement with non-volatile memory module and method of en-/decrypting data in the non-volatile memory module Buhr, Wolfgang
12/125,737	US	5/22/2008	Circuit arrangement with non-volatile memory module and method for en-/decrypting data in the non-volatile memory module Buhr, Wolfgang
CNZL200480006555.1 (CN200480006555.1)	CN	11/26/2008 (3/3/2004)	Test for weak SRAM cells Pineda De Gyvez, J. D. J.; Sachdev, M.; Pavlov, A.
DE602004006848.9 (DE602004006848.9)	DE	2/7/2008 (3/3/2004)	Test for weak SRAM cells Pineda De Gyvez, Jose D.; Sachdev, Manoj; Pavlov, Andrei
FR1606824 (FR04716681.4)	FR	6/6/2007 (3/3/2004)	Test for weak SRAM cells Pineda De Gyvez, Jose D. J.; Sachdev, Manoj; Pavlov, Andrei

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
GB1606824 (GB04716681.4)	GB	6/6/2007 (3/3/2004)	Test for weak SRAM cells Pineda De Gyvez, Jose D. J.; Sachdev, Manoj; Pavlov, Andrei
KR10-2005-7016826	KR	3/3/2004	Test for weak SRAM cells Pineda De Gyvez, Jose D. J.; Sachdev, Manoj; Pavlov, Andrei
7,200,057 (10/548,340)	US	4/3/2007 (3/3/2004)	Test for weak SRAM cells Pineda De Gyvez, Jose De Jesus; Sachdev, Manoj; Pavlov, Andrei
CN200480038530.X	CN	12/20/2004	High sensitivity magnetic built-in current sensor De Wilde, Johannes; Pineda De Gyvez, Jose D. J.; De Jong, Franciscus G. M.; Huisken, Josephus A.; Boeve, Hans M. B.; Phan Le, Kim
DE602004011995.4 (DE602004011995.4)	DE	4/9/2009 (12/20/2004)	High sensitivity magnetic built-in current sensor De Wilde, Johannes; Pineda De Gyvez, Jose D.; De Jong, Franciscus G.; Huisken, Josephus A.; Boeve, Hans, M.; Phan Le, Kim
FR1706751 (FR04105805.8)	FR	2/20/2008 (12/20/2004)	High sensitivity magnetic built-in current sensor De Wilde, Johannes; Pineda De Gyvez, Jose D. J.; De Jong, Franciscus G. M.; Huisken, Josephus A.; Boeve, Hans M. B.; Phan Le, Kim
GB1706751 (GB04105805.8)	GB	2/20/2008 (12/20/2004)	high sensitivity magnetic built-in current sensor De Wilde, Johannes; Pineda De Gyvez, Jose D. J.; De Jong, Franciscus G. M.; Huisken, Josephus A.; Boeve, Hans M. B.; Phan Le, Kim
JP2006-546454	JP	12/20/2004	High sensitivity magnetic built-in current sensor De Wilde, Johannes; Pineda De Gyvez, Jose D. J.; De Jong, Franciscus G. M.; Huisken, Josephus A.; Boeve, Hans M. B.; Phan Le, Kim
KR10-2006-7012418	KR	12/20/2004	High sensitivity magnetic built-in current sensor De Wilde, Johannes; Pineda De Gyvez, Jose D. J.; De Jong, Franciscus G. M.; Huisken, Josephus A.; Boeve, Hans M. B.; Phan Le, Kim

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
SG122666 (SG200603641-2)	SG	12/20/2004	High sensitivity magnetic built-in current sensor De Wilde, Johannes; Pineda De Gyvez, Jose D. J.; De Jong, Franciscus G. M.; Huisken, Josephus A.; Boeve, Hans M. B.; Phan Le, Kim
TW093139705	TW	12/20/2004	High sensitivity magnetic built-in current sensor De Wilde, Johannes; Pineda De Gyvez, Jose D. J.; De Jong, Franciscus G. M.; Huisken, Josephus A.; Boeve, Hans M. B.; Phan Le, Kim
7,619,431 (10/596,644)	US	11/17/2009 (12/20/2004)	High sensitivity magnetic built-in current sensor De Wilde, Johannes; Pineda De Gyvez, Jose De Jesus; De Jong, Franciscus Gerardus Maria; Huisken, Josephus Antonius; Boeve, Hans Marc Bert; Phan Le, Kim
CNZL200380105655.5 (CN200380105655.5)	CN	4/29/2009 (12/3/2003)	One-time programmable memory device Reiner, J. C.
DE60329781.1 (DE60329781.1)	DE	12/3/2009 (12/3/2003)	One-time programmable memory device Reiner, Joachim Christian
FR1573747 (FR03775665.7)	FR	10/21/2009 (12/3/2003)	One-time programmable memory device Reiner, Joachim Christian
GB1573747 (GB03775665.7)	GB	10/21/2009 (12/3/2003)	One-time programmable memory device Reiner, Joachim Christian
JP2004-558946	JP	12/3/2003	One-time programmable memory device Reiner, Joachim Christian
7,333,356 (10/538,288)	US	2/19/2008 (12/3/2003)	One-time programmable memory devices Reiner, Joachim Christian
CN200380103955.X	CN	11/13/2003	Circuit arrangement with non-volatile memory module and method for registering light-attacks on the non-volatile memory module Garbe, J.C. H.; Buhr, W.
DE60326750.5 (DE60326750.5)	DE	4/30/2009 (11/13/2003)	Circuit arrangement with non-volatile memory module and method for registering light-attacks on the non-volatile memory module Garbe, Joachim Christoph Hans; Buhr, Wolfgang

Patent or Application No.	Country	Filing Date	Title of Patent and First Named Inventor
FR1565915 (FR03769828.9)	FR	3/18/2009 (11/13/2003)	Circuit arrangement with non-volatile memory module and method for registering light-attacks on the non-volatile memory module Garbe, Joachim Christoph Hans; Buhr, Wolfgang
GB1565915 (GB03769828.9)	GB	3/18/2009 (11/13/2003)	Circuit arrangement with non-volatile memory module and method for registering light-attacks on the non-volatile memory module Garbe, Joachim Christoph Hans; Buhr, Wolfgang
7,232,983 (10/536,302)	US	6/19/2007 (11/13/2003)	Circuit arrangement with non-volatile memory module and method for registering light-attacks on the non-volatile memory module Garbe, Joachim C. H.; Buhr, Wolfgang

(b) all patents and patent applications (i) to which any of the Patents directly or indirectly claims priority, (ii) for which any of the Patents directly or indirectly forms a basis for priority, and/or (iii) that were co-owned applications that incorporate by reference, or are incorporated by reference into, the Patents;

(c) all reissues, reexaminations, extensions, continuations, continuations in part, continuing prosecution applications, requests for continuing examinations, divisions, registrations of any item in any of the foregoing categories (a) and (b);

(d) all foreign patents, patent applications, and counterparts relating to any item in any of the foregoing categories (a) through (c), including, without limitation, certificates of invention, utility models, industrial design protection, design patent protection, and other governmental grants or issuances;

(e) all items in any of the foregoing in categories (b) through (d), whether or not expressly listed as Patents below and whether or not claims in any of the foregoing have been rejected, withdrawn, cancelled, or the like;

(f) inventions, invention disclosures, and discoveries described and enabled in any of the Patents and/or any item in the foregoing categories (b) through (e) that (i) are included in any claim in the Patents and/or any item in the foregoing categories (b) through (e), (ii) are subject matter capable of being reduced to a patent claim in a reissue or reexamination proceeding brought on any of the Patents and/or any item in the foregoing categories (b) through (e), and/or (iii) could have been included as an allowable claim in any

of the Patents and/or any item in the foregoing categories (b) through (e) under applicable patent laws;

(g) all rights to apply in any or all countries of the world for patents, certificates of invention, utility models, industrial design protections, design patent protections, or other governmental grants or issuances of any type related to any item in any of the foregoing categories (a) through (f), including, without limitation, under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement, or understanding;

(h) all causes of action (whether known or unknown or whether currently pending, filed, or otherwise) and other enforcement rights under, or on account of, any of the Patents and/or any item in any of the foregoing categories (b) through (g), including, without limitation, all causes of action and other enforcement rights for

(1) damages,
(2) injunctive relief, and
(3) any other remedies of any kind

for past, current, and future infringement; and

(i) all rights to collect royalties and other payments under or on account of any of the Patents and/or any item in any of the foregoing categories (b) through (h).

Assignor hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

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The terms and conditions of this Assignment of Patent Rights will inure to the benefit of Assignee, its successors, assigns, and other legal representatives and will be binding upon Assignor, its successors, assigns, and other legal representatives.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed at New Braunfels, TX on 30 March, 2011.

ASSIGNOR:

NXP B.V.

By: _____
Name: Marc Mixer
Title: Authorized Signatory
(Signature MUST be attested)

ATTESTATION OF SIGNATURE PURSUANT TO 28 U.S.C. § 1746

The undersigned witnessed the signature of Marc Mixer to the above Assignment of Patent Rights on behalf of NXP B.V. and makes the following statements:

1. I am over the age of 18 and competent to testify as to the facts in this Attestation block if called upon to do so.

2. Marc Mixer is personally known to me (or proved to me on the basis of satisfactory evidence) and appeared before me on 30 March, 2011 to execute the above Assignment of Patent Rights on behalf of NXP B.V.

3. Marc Mixer subscribed to the above Assignment of Patent Rights on behalf of NXP B.V.

I declare under penalty of perjury under the laws of the United States of America that the statements made in the three (3) numbered paragraphs immediately above are true and correct.

EXECUTED on 30 March, 2011 (date)

_____
Print Name: Joyce Brown