PATENT ASSIGNMENT

Electronic Version v1.1
Stylesheet Version v1.1

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
Cypress Semiconductor Corporation	02/15/2006

RECEIVING PARTY DATA

Name:	Netlogic Microsystems, Inc.
Street Address:	3975 Freedom Circle
City:	Santa Clara
State/Country:	CALIFORNIA
Postal Code:	95054

PROPERTY NUMBERS Total: 1

Property Type	Number
Patent Number:	7570503

OP $40.00 7570503

CORRESPONDENCE DATA

Fax Number: (408)530-9797
Correspondence will be sent via US Mail when the fax attempt is unsuccessful.
Phone: 4085309700
Email: bsako@hollp.com
Correspondent Name: Haverstock & Owens, LLP
Address Line 1: 162 N. Wolfe Road
Address Line 4: Sunnyvale, CALIFORNIA 94086

ATTORNEY DOCKET NUMBER:	NETL-03000
NAME OF SUBMITTER:	Bradley T. Sako

Total Attachments: 4
source=Provisional_Assignments_CY_to_NETL#page1.tif
source=Provisional_Assignments_CY_to_NETL#page2.tif
source=Provisional_Assignments_CY_to_NETL#page3.tif
source=Provisional_Assignments_CY_to_NETL#page4.tif

ASSIGNMENT OF PROVISIONAL PATENT APPLICATIONS

THIS ASSIGNMENT OF PATENT APPLICATIONS (this *"Assignment"*) is made as of February 15, 2006 (the *"Assignment Date"*) by Cypress Semiconductor Corporation, a Delaware corporation (the *"Assignor"*), to NetLogic Microsystems, Inc., a Delaware corporation (the *"Assignee"*).

RECITALS

A. Pursuant to the Agreement for the Purchase and Sale of Assets, dated January 25, 2006, by and between Assignor and Assignee (the ***"Purchase Agreement"***), Assignor agreed to sell, assign, transfer, convey and deliver to Assignee certain assets, including all of Assignor's right, title and interest in and to the Patent Applications (as defined below).

B. The obligation of Assignee to consummate the transactions contemplated by the Purchase Agreement is conditioned in part on the execution and delivery of this Assignment.

ASSIGNMENT

For good and valuable consideration, the receipt, adequacy and legal sufficiency of which are hereby acknowledged:

Assignor hereby sells, assigns, transfers, conveys and delivers to Assignee, its successors and assigns, (a) all worldwide right, title and interest in, to and under the patent applications listed on Schedule A to this Assignment (collectively, the ***"Patent Applications"***), including but not limited to all patent applications, patents, or similar legal protections that have been, or will be, obtained, based on any of said Patent Applications (b) all rights to obtain renewals, extensions, continuations, continuations-in-part, reissues, re-examinations, divisions, substitutes, or equivalents thereof, based on any of said Patent Applications, in the United States and all foreign countries, and (c) all past, present and future claims, counterclaims, causes of action, choses in action, rights of recovery, rights of set off, and rights of recoupment in or with respect to any of the Patent Applications.

Assignor grants the attorney of record the power to insert on this Assignment any further identification that may be necessary to comply with the rules of the United States Patent and Trademark Office, or rules of other entities, including United States or foreign governments or patent offices, for recordation of this document.

Assignor shall execute or cause to be delivered to Assignee such instruments and other documents, and shall take such other actions, as Assignee may reasonably request after the Assignment Date, that are necessary for the purpose of carrying out or evidencing the assignment of the Patent Applications pursuant to this Assignment.

IN WITNESS WHEREOF, Assignor has caused its duly authorized officer to execute this Assignment of Patent Applications as of the Assignment Date.

CYPRESS SEMICONDUCTOR CORPORATION

By: _____

Name: Brad Buss_____

Title: Chief Financial Officer_____

SCHEDULE A

PROVISIONAL PATENT APPLICATIONS

NETWORK DEVICE, CARRIER MEDIUM AND METHODS FOR INCREMENTALLY UPDATING A FORWARDING DATABASE THAT IS SPLIT INTO A BOUNDED NUMBER OF SUB-DATABASES HAVING A BOUNDED SIZE	60/458,497
ARCHITECTURE FOR ALGORITHMIC NETWORK SEARCH ENGINE WITH FIXED LATENCY, HIGH CAPACITY, AND HIGH THROUGHPUT	60/476,033
SENSE AMPLIFIER CIRCUIT FOR CONTENT ADDRESSABLE MEMORY DEVICE	60/483,418
SENSE AMPLIFIER ARCHITECTURE FOR CONTENT ADDRESSABLE MEMORY (CAM) DEVICE	60/502,833
EFFICIENT HIERARCHICAL LEARN OPERATION	60/505,382
CONTENT ADDRESSABLE MEMORY (CAM) CELL BIT LINE ARCHITECTURE	60/506,679
METHOD FOR UPDATING TCAM MASK/DATA	60/531,830
SYSTEM AND METHOD FOR DYNAMICALLY COMBINING ACCESS CONTROL LIST POLICY SEARCHING WITH TREE-BASED FORWARDING TABLE SEARCHING IN A CONTENT ADDRESSABLE MEMORY	60/531,836
IMPLEMENTING PSEUDO-TERNARY CAM FUNCTIONALITY WITH FULL-TERNARY CAM IMPLEMENTATION	60/532,401
LAYOUT FOR INTERLOCKING TCAM CELLS	60/556,628
FINDING MAXIMAL STRIPES IN DISK CACHES USING TCAM	60/612,905
PSEUDO TERNARY CAM ARRAY ROW REDUNDANCY ARCHITECTURE	60/629,694
BINARY/TERNARY DYNAMICALLY CONFIGURABLE CAM CELL	60/657,754
SINGLE ENDED WRITE MUXED TCAM CELL	60/661,745
SINGLE ENDED COLUMNWISE CONDITIONAL PREWRITE TCAM CELL	60/663,656
MEMORY OPTIMIZED PATTERN SEARCHING (MOPS)	60/665,478

WIDE WORD SUPPORT IN CAMS	60/666,875
A GLOBAL MASKING ARCHITECTURE FOR CONTENT ADDRESSABLE MEMORIES (CAM)	60/667,325
IN-LINE FALSE HIT DETECTION ARCHITECTURE FOR A CONTENT ADDRESSABLE MEMORY	60/667,343
SHARED BACK-END MSA ARCHITECTURE	60/667,587
SIGNATURE SEARCHING USING NETWORK SEARCH ENGINBES (NSES)	60/667,877
FASTER LOCAL PRIORITY ENCODER	60/678,468
DIFFERENTIAL, BITMASKABLE, ATOMIC/NON-ATOMIC TCAM CELLS	60/683,237
SOFT PRIORITY CIRCUIT AND METHOD FOR CONTENT ADDRESSABLE MEMORY (CAM) DEVICES	60/689,968
ACL'S IN TCAM	60/692,817
BLOCK MAPPING CIRCUIT AND METHOD FOR MEMORY DEVICE	60/695,280
SORTING ALGORITHMS USING CAMS	60/695,281
RANGE REPRESENTATION IN A CONTENT ADDRESSABLE MEMORY (CAM) USING AN IMPROVED ENDCODING SCHEME	60/696,128
CIRCUITS AND METHODS CONTROLLING A SEARCHABLE RANGE WITHIN NETWORK SEARCH ENGINES (NSE'S)	60/702,950
METHOD AND DEVICE FOR LIMITING CURRENT RATE CHANGES IN BLOCK SELECTABLE SEARCH ENGINE	60/705,974
SENSE AMPLIFIER CIRCUIT WITH IMPROVED ACCURACY AND RELIABILITY	60/706,275
PSEUDO TERNARY CAM USING BINARY CAM CELLS	60/719,415
MULTI-WORD PER ROW ARCHITECTURE FOR CAMS	60/722,615
FAST PARITY SCAN ENGINE	60/722,650
ROW REDUNDANCY ARCHITECTURE FOR CAMS	60/722,651
METHOD AND DEVICE FOR SCALABLE MULTIPLE MATCH EXTRACTION FROM SEARCH DATA	60/749,862
NETWORK SEARCH ENGINE (NSE) AND METHOD FOR PERFORMING INTERVAL LOCATION USING PREFIX MATCHING	60/752,645