PATENT ASSIGNMENT

Electronic Version v1.1
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SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
MOSAID Technologies Corporation	08/01/2008

RECEIVING PARTY DATA

Name:	Mosaid Technologies Incorporated
Street Address:	11 Hines Road
City:	Kanata, Ontario
State/Country:	CANADA
Postal Code:	K2K 2X1

PROPERTY NUMBERS Total: 1

Property Type	Number
Application Number:	13158862

CH $40.00 13158862

CORRESPONDENCE DATA

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ATTORNEY DOCKET NUMBER:	2037.2076-015
NAME OF SUBMITTER:	Jillian M. Kane

Total Attachments: 9
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CONFIRMATORY ASSIGNMENT OF PATENT RIGHTS

For good and valuable consideration, the receipt of which is hereby acknowledged, MOSAID Technologies Corporation, a Delaware company, with an office at Corporation Trust Center, 1209 Orange Street, Wilmington, Delaware 19801 U.S.A. (***"Assignor"***), confirms that it has sold, assigned, transferred, and conveyed unto MOSAID Technologies Incorporated, a Canadian company, with an address at 11 Hines Road, Kanata, Ontario K2K 2X1 CANADA (***"Assignee"***), or its designees, all right, title, and interest that currently exist and may exist in the future in and to any and all of the following (collectively, the ***"Patent Rights"***):

(a) the provisional patent applications, patent applications and patents listed in Exhibit A (the "Patents");

(b) all patents and patent applications to which any of the Patents directly or indirectly forms a basis of priority;

(c) all reissues, reexaminations, extensions, continuations, continuations in part, continuing prosecution applications, requests for continuing examinations, divisions, registrations of any item in any of the foregoing categories (a) and (b);

(d) all foreign patents, patent applications, and counterparts relating to any item of any of the foregoing categories (a) through (c), including, without limitation, certificates of invention, utility models, industrial design protection, design patent protection, and other governmental grants or issuances; and

(e) all items in any of the foregoing categories (b) through (d), whether or not expressly listed as Patents in Exhibit A and whether or not claims in any of the foregoing have been rejected, withdrawn, cancelled, or the like;

(f) all causes of action and remedies related to any of the Patents and/or any item in any of the foregoing categories (b) through (e) (including, without limitation, the right to sue for past, present, or future infringement, misappropriation or violation of rights related to any of the foregoing, and all rights to seek damages, injunctive relief, and any other remedies of any kind, and the right to collect royalties and other payments under or on account of any of the foregoing).

Assignor represents, warrants and covenants that:

(1) Assignor has the full power and authority, and has obtained all third party consents, approvals and/or other authorizations required to enter this Assignment of Patent Rights to Assignee; and

Assignor hereby authorizes the respective patent office or government agency in each jurisdiction to issue any and all patents, certificates of invention, utility models or other governmental grants or issuances that may be granted upon any

of the Patent Rights in the name of the Assignee, as the assignee to the entire interest therein.

IN WITNESS WHEREOF this Assignment of Patent Rights is executed at Ottawa on August 1, 2008.

ASSIGNOR:

MOSAID Technologies Corporation

By: _____

Name: Phillip Shaer

Title: Vice President, General Counsel & Corporate Secretary

STATEMENT OF WITNESS

I, ROXANNE DOROSZKIEWICZ whose full post office address is
(name of witness)

11 HINES RD, SUITE 203

OTTAWA ON K2K 2X1

was personally present and did see Phillip Shaer execute the within assignment and such assignor is personally known to me to be the person described in such document.

_____
(Signature of Witness)

Assignee hereby accepts the assignment and transfer of the Patent Rights according to the terms stipulated herein.

ASSIGNEE:

MOSAID Technologies Incorporated

By: _____

Name: Phillip Shaer

Title: Vice President, General Counsel
& Corporate Secretary

STATEMENT OF WITNESS

I, ROXANNE DOROSZKIEWICZ whose full post office address is
(name of witness)

11 HINES RD. SUITE 203

OTTAWA ON K2K 2X1

was personally present and did see Phillip Shaer execute the within assignment and such assignor is personally known to me to be the person described in such document.

_____
(Signature of Witness)

Exhibit "A"
List of Patents and Patent Applications

MOSAID Reference Number	Title	Country Name	Serial Number	Filed Date	Patent Number	Issue Date	Inventor Names
1181-07CN-000-70	Managing Power on Integrated Circuits Using Power Islands	CHINA	2004-80019586	5/7/2004			HOBERMAN, Barry, A. HILLMAN, Daniel, L. SHIELL, Jon
1181-08EP-000-70	Managing Power On Integrated Circuits Using Power Islands	EUROPE	04751547.3-2224	5/7/2004			HOBERMAN, Barry, A. HILLMAN, Daniel, L. SHIELL, Jon
1181-09IN-000-70	Managing Power on Integrated Circuits Using Power Islands	INDIA	3310/CHENP/2005	5/7/2004			HOBERMAN, Barry, A. HILLMAN, Daniel, L. SHIELL, Jon
1181-06JP-000-70	Managing Power on Integrated Circuits Using Power Islands	JAPAN	2006-532832	5/7/2004			HOBERMAN, Barry, A. HILLMAN, Daniel, L. SHIELL, Jon
1181-05KR-000-70	Managing Power on Integrated Circuits Using Power Islands	SOUTH KOREA	10-2005-7021157	5/7/2004			HOBERMAN, Barry, A. HILLMAN, Daniel, L. SHIELL, Jon
1181-04TW-000-70	Managing Power On Integrated Circuits Using Power Islands	TAIWAN	93112998	5/7/2004			HOBERMAN, Barry, A. HILLMAN, Daniel, L. SHIELL, Jon
1181-01US-0PR-70	System and Method for Managing Power In Integrated Circuits	UNITED STATES	60/468,742	5/7/2003			HOBERMAN, Barry, A.
1181-02US-000-75	Managing Power on Integrated Circuits Using Power Islands	UNITED STATES	10/840,893	5/7/2004	7,051,306	5/23/2006	HOBERMAN, Barry, A. HILLMAN, Daniel, L. SHIELL, Jon
1181-10US-0C1-70	Power Managers for an Integrated Circuit	UNITED STATES	11/336,097	1/20/2006			HOBERMAN, Barry, A. HILLMAN, Daniel, L. SHIELL, Jon
1181-11US-0C2-75	Power Managers for an Integrated Circuit	UNITED STATES	12/176,645	7/21/2008			HOBERMAN, Barry, A. HILLMAN, Daniel, L. SHIELL, Jon
1181-03PCT-00-70	Managing Power on Integrated Circuits Using Power Islands	WIPO	PCT/US04/14205	5/7/2004			HOBERMAN, Barry, A. HILLMAN, Daniel, L. SHIELL, Jon
1182-11CA-000-00	LOW LEAKAGE AND DATA RETENTION CIRCUITRY	CANADA	2,595,375	1/20/2005			HOBERMAN, Barry, A. HILLMAN, Daniel, L. WALKER, William, G. CALLAHAN, John, M. ZAMPAGLIONE, Michael, A. COLE, Andrew
1182-05CN-000-70	LOW LEAKAGE AND DATA RETENTION CIRCUITRY	CHINA	2005-80005487.1	1/20/2005			HOBERMAN, Barry, A. HILLMAN, Daniel, L. WALKER, William, G. CALLAHAN, John, M. ZAMPAGLIONE, Michael, A. COLE, Andrew

MOSAID Reference Number	Title	Country Name	Serial Number	Filed Date	Patent Number	Issue Date	Inventor Names
1182-09EPO-000-70	LOW LEAKAGE AND DATA RETENTION CIRCUITRY	EUROPE	5711776.4	1/20/2005			HOBERMAN, Barry, A. HILLMAN, Daniel, L. WALKER, William, G. CALLAHAN, John, M. ZAMPAGLIONE, Michael, A. COLE, Andrew
1182-08IN-000-70	LOW LEAKAGE AND DATA RETENTION CIRCUITRY	INDIA	5060/DELNP/2006	1/20/2005			HOBERMAN, Barry, A. HILLMAN, Daniel, L. WALKER, William, G. ZAMPAGLIONE, Michael, A. CALLAHAN, John, M. COLE, Andrew
1182-06JP-000-70	LOW LEAKAGE AND DATA RETENTION CIRCUITRY	JAPAN	2006-554101	1/20/2005			HOBERMAN, Barry, A. HILLMAN, Daniel, L. WALKER, William, G. CALLAHAN, John, M. ZAMPAGLIONE, Michael, A. COLE, Andrew
1182-07KR-000-70	Low Leakage and Data Retention Circuitry	SOUTH KOREA	10-2006-7016624	1/20/2005			HOBERMAN, Barry, A. HILLMAN, Daniel, L. WALKER, William, G. CALLAHAN, John, M. ZAMPAGLIONE, Michael, A. COLE, Andrew
1182-04TW-000-70	LOW LEAKAGE AND DATA RETENTION CIRCUITRY	TAIWAN	94104756	2/18/2005			HOBERMAN, Barry, A. HILLMAN, Daniel, L. WALKER, William, G. CALLAHAN, John, M. ZAMPAGLIONE, Michael, A. COLE, Andrew
1182-01US-0PR-70	POWER MANAGEMENT AND POWER SAVINGS IN INTEGRATED CIRCUITS	UNITED STATES	60/546,574	2/19/2004			HOBERMAN, Barry, A. HILLMAN, Daniel, L. DRORI, Joseph ZAMPAGLIONE, Michael, A. WALKER, William, G. CALLAHAN, John, M.
1182-10US-DIV-70	LOW LEAKAGE AND DATA RETENTION CIRCUITRY	UNITED STATES	11/732,181	4/2/2007	7,348,804	3/25/2008	HOBERMAN, Barry, A. HILLMAN, Daniel, L. WALKER, William, G. CALLAHAN, John, M. ZAMPAGLIONE, Michael, A. COLE, Andrew

MOSAID Reference Number	Title	Country Name	Serial Number	Filed Date	Patent Number	Issue Date	Inventor Names
1182-12US-0C1-10	LOW LEAKAGE AND DATA RETENTION CIRCUITRY	UNITED STATES	11/998,725	11/30/2007			HOBERMAN, Barry, A. HILLMAN, Daniel, L. WALKER, William, G. CALLAHAN, John, M. ZAMPAGLIONE, Michael, A. COLE, Andrew
1182-02US-000-70	LOW LEAKAGE AND DATA RETENTION CIRCUITRY	UNITED STATES	11/041,687	1/20/2005	7,227,383	6/5/2007	HOBERMAN, Barry, A. HILLMAN, Daniel, L. WALKER, William, G. CALLAHAN, John, M. ZAMPAGLIONE, Michael, A. COLE, Andrew
1182-03PCT-00-70	LOW LEAKAGE AND DATA RETENTION CIRCUITRY	WIPO	PCT/US2006/001938	1/20/2006			HOBERMAN, Barry, A. HILLMAN, Daniel, L. WALKER, William, G. CALLAHAN, John, M. ZAMPAGLIONE, Michael, A. COLE, Andrew
1183-13CA-00-00	SYSTEMS AND METHODS FOR MINIMIZING STATIC LEAKAGE OF AN INTEGRATED CIRCUIT	CANADA	2,614,125	7/5/2006			CAPLAN, Randy SCHWAKE, Steven
1183-06CN-00-70	SYSTEMS AND METHODS FOR MINIMIZING STATIC LEAKAGE OF AN INTEGRATED CIRCUIT	CHINA	2006-80026872.4	7/5/2006			CAPLAN, Randy SCHWAKE, Steven
1183-09EPO-00-10	Systems and Methods for minimizing static Leakage of an Integrated Circuit	EUROPE	5780186.2	7/5/2006			CAPLAN, Randy SCHWAKE, Steven
1183-08IL-00-70	SYSTEMS AND METHODS FOR MINIMIZING STATIC LEAKAGE OF AN INTEGRATED CIRCUIT	ISRAEL	180613	7/5/2006			CAPLAN, Randy SCHWAKE, Steven
1183-07IN-00-70	Systems and Methods For Minimizing Static Leakage Of An Integrated Circuit	INDIA	191/MUMNP/2007	7/5/2006			CAPLAN, Randy SCHWAKE, Steven
1183-04JP-00-70	SYSTEMS AND METHODS FOR MINIMIZING STATIC LEAKAGE OF AN INTEGRATED CIRCUIT	JAPAN	2007-520441	7/5/2006			CAPLAN, Randy SCHWAKE, Steven
1183-05KR-00-70	SYSTEMS AND METHODS FOR MINIMIZING STATIC LEAKAGE OF AN INTEGRATED CIRCUIT	SOUTH KOREA	10-2007-7003098	7/5/2006			CAPLAN, Randy SCHWAKE, Steven
1183-01US-0PR-70	Systems and Methods for I/O and Power Island Management and Leakage Control on Integrated Circuits	UNITED STATES	60/586,565	7/9/2004			HOBERMAN, Barry, A. COLE, Andrew CAPLAN, Randy SCHWAKE, Steven

MOSAID Reference Number	Title	Country Name	Serial Number	Filed Date	Patent Number	Issue Date	Inventor Names
1183-02US-000-10	SYSTEMS AND METHODS FOR MINIMIZING STATIC LEAKAGE OF AN INTEGRATED CIRCUIT	UNITED STATES	10/996,739	11/24/2004	7,279,956	10/9/2007	Caplan, Randy J. Schwake, Steven J.
1183-11US-CIP-10	SYSTEMS AND METHODS FOR MINIMIZING STATIC LEAKAGE OF AN INTEGRATED CIRCUIT	UNITED STATES	11/900,971	9/14/2007	7,382,178	6/3/2008	CAPLAN, Randy SCHWAKE, Steven
1183-12US-DIV-70	SYSTEMS AND METHODS FOR MINIMIZING STATIC LEAKAGE OF AN INTEGRATED CIRCUIT	UNITED STATES	11/998,762	11/30/2007			CAPLAN, Randy SCHWAKE, Steven
1183-03PCT-00-70	SYSTEMS AND METHODS FOR MINIMIZING STATIC LEAKAGE OF AN INTEGRATED CIRCUIT	WIPO	PCT/US2005/023839	7/5/2005			CAPLAN, Randy SCHWAKE, Steven
1184-08CA-000-00	PHASE-LOCKED LOOP CIRCUITRY USING CHARGE PUMPS WITH CURRENT MIRROR CIRCUITRY	CANADA	2,590,557	12/13/2005			CAPLAN, Randy HARDY, Steven, P. COLE, Andrew
1184-07CN-000-10	PHASE-LOCKED LOOP CIRCUITRY USING CHARGE PUMPS WITH CURRENT MIRROR CIRCUITRY	CHINA	2005-80048061.4	12/13/2005			CAPLAN, Randy HARDY, Steven, P. COLE, Andrew
1184-06EP-000-10	PHASE-LOCKED LOOP CIRCUITRY USING CHARGE PUMPS WITH CURRENT MIRROR CIRCUITRY	EUROPE	5854195.4	12/13/2005			CAPLAN, Randy HARDY, Steven, P. COLE, Andrew
1184-09IN-000-10	PHASE-LOCKED LOOP CIRCUITRY USING CHARGE PUMPS WITH CURRENT MIRROR CIRCUITRY	INDIA	3074/CHENP/2007	12/13/2005			CAPLAN, Randy HARDY, Steven, P. COLE, Andrew
1184-04JP-000-10	PHASE-LOCKED LOOP CIRCUITRY USING CHARGE PUMPS WITH CURRENT MIRROR CIRCUITRY	JAPAN	2007545736	12/13/2005			CAPLAN, Randy HARDY, Steven, P. COLE, Andrew
1184-05KR-000-10	PHASE-LOCKED LOOP CIRCUITRY USING CHARGE PUMPS WITH CURRENT MIRROR CIRCUITRY	SOUTH KOREA	2007-7015938	12/13/2005			CAPLAN, Randy HARDY, Steven, P. COLE, Andrew
1184-01US-0PR-70	SYSTEMS AND METHODS FOR PHASE LOCKED LOOP USING CHARGE PUMPS	UNITED STATES	60/635,849	12/13/2004			CAPLAN, Randy HARDY, Steven, P. COLE, Andrew
1184-02US-000-70	PHASE-LOCKED LOOP CIRCUITRY USING CHARGE PUMPS WITH CURRENT MIRROR CIRCUITRY	UNITED STATES	11/264,283	10/31/2005			CAPLAN, Randy HARDY, Steven, P. COLE, Andrew
1184-03PCT-000-10	PHASE-LOCKED LOOP CIRCUITRY USING CHARGE PUMPS WITH CURRENT MIRROR CIRCUITRY	WIPO	PCT/US2005/045427	12/13/2005			CAPLAN, Randy HARDY, Steven, P. COLE, Andrew
1185-05CA-000-00	Integrated Circuit With Signal Bus Formed By Cell Abutment of Logic Cells	CANADA	2,608,323	5/12/2006			HILLMAN, Daniel, L. WALKER, William, G.

MOSAID Reference Number	Title	Country Name	Serial Number	Filed Date	Patent Number	Issue Date	Inventor Names
1185-09CN-000-75	Integrated Circuit With Signal Bus Formed By Cell Abutment of Logic Cells	CHINA	2006-80020927.5	5/12/2006			HILLMAN, Daniel, L. WALKER, William, G.
1185-08EP-000-70	Integrated Circuit With Signal Bus Formed By Cell Abutment of Logic Cells	EUROPE	6770268.8	5/12/2006			HILLMAN, Daniel, L. WALKER, William, G.
1185-10IN-000-75	Integrated Circuit With Signal Bus Formed By Cell Abutment of Logic Cells	INDIA	2078/MUMNP/2007	5/12/2006			HILLMAN, Daniel, L. WALKER, William, G.
1185-06JP-000-75	Integrated Circuit With Signal Bus Formed By Cell Abutment of Logic Cells	JAPAN	2008-511396	5/12/2006			HILLMAN, Daniel, L. WALKER, William, G.
1185-07KR-000-75	Integrated Circuit With Signal Bus Formed By Cell Abutment of Logic Cells	SOUTH KOREA	2007-7029220	5/12/2006			HILLMAN, Daniel, L. WALKER, William, G.
1185-04TW-000-75	INTEGRATED CIRCUIT WITH SIGNAL BUS FORMED BY CELL ABUTMENT OF LOGIC CELLS	TAIWAN	95117110	5/16/2006			HILLMAN, Daniel, L. WALKER, William, G.
1185-01US-0PR-70	Integrated Circuit Layout with sleep transistors	UNITED STATES	60/680,888	5/13/2005			HILLMAN, Daniel, L. WALKER, William, G.
1185-02US-000-75	Integrated Circuit With Signal Bus Formed By Cell Abutment Of Logic Cells	UNITED STATES	11/433,158	5/12/2006			HILLMAN, Daniel, L. WALKER, William, G.
1185-03PCT-00-75	Integrated Circuit With Signal Bus Formed By Cell Abutment of Logic Cells	WIPO	PCT/US2006/018409	5/12/2006			HILLMAN, Daniel, L. WALKER, William, G.
1188-02TW-000-70	PHASE-LOCKED LOOP FILTER CAPACITANCE WITH A DRAG CURRENT	TAIWAN	96112073	4/4/2007			CAPLAN, Randy
1188-01US-000-75	PHASE-LOCKED LOOP FILTER CAPACITANCE WITH A DRAG CURRENT	UNITED STATES	11/400,495	4/6/2006			CAPLAN, Randy
1189-03TW-000-25	REDUCED POWER CONSUMPTION CIRCUITRY FOR MEMORY USING A REFERENCE THRESHOLD VOLTAGE	TAIWAN	96115098	4/27/2007			ZAMPAGLIONE, Michael, A. TOOHER, Michael
1189-01US-0PR-70	Reduced Power Consumption Circuitry For Memory Using A Referenced Threshold Voltage	UNITED STATES	60/796,138	4/28/2006			ZAMPAGLIONE, Michael, A. TOOHER, Michael
1189-02US-000-25	SRAM LEAKAGE REDUCTION CIRCUIT	UNITED STATES	11/741,647	4/27/2007			ZAMPAGLIONE, Michael, A. TOOHER, Michael
1189-04PCT-000-25	SRAM LEAKAGE REDUCTION CIRCUIT	WIPO	PCT/US2007/067633	4/27/2007			ZAMPAGLIONE, Michael, A. TOOHER, Michael

MOSAID Reference Number	Title	Country Name	Serial Number	Filed Date	Patent Number	Issue Date	Inventor Names
1203-02US-000-90	METHOD AND APPARATUS FOR INTEGRATED CIRCUIT DESIGN WITH A SOFTWARE TOOL	UNITED STATES	10/162,123	6/3/2002	6,766,496	7/20/2004	MCMANUS, Michael, J. RIVERA, Billie, J. TALBURT, Richard WALKER, William, G. ZAMPAGLIONE, Michael, A.
1205-02US-000-90	METHOD AND APPARATUS FOR INTEGRATED CIRCUIT DESIGN WITH LIBRARY CELLS	UNITED STATES	10/162,120	6/3/2002	7,051,308	5/23/2006	MCMANUS, Michael, J. RIVERA, Billie, J. TALBURT, Richard WALKER, William, G. ZAMPAGLIONE, Michael, A.
1252-01US-0PR-25	BALANCED PSEUDO-RANDOM BINARY SEQUENCE GENERATOR	UNITED STATES	60/912,307	4/17/2007			GALLOWAY, Brian, Jeffrey
1252-02US-000-25	BALANCED PSEUDO-RANDOM BINARY SEQUENCE GENERATOR	UNITED STATES	11/873,330	10/16/2007			GALLOWAY, Brian, Jeffrey
1253-01US-0PR-25	CIRCUIT AND METHOD FOR GLITCH CORRECTION	UNITED STATES	60/912,310	4/17/2007			GALLOWAY, Brian, Jeffrey HILLMAN, Daniel, L.
1253-02US-000-90	CIRCUIT AND METHOD FOR GLITCH CORRECTION	UNITED STATES	11/946,767	11/28/2007			GALLOWAY, Brian, Jeffrey HILLMAN, Daniel, L.